

Jaydeep P. Kulkarni

Assistant Professor of Electrical and Computer Engineering
The University of Texas at Austin

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Research Interests:

- Energy efficient integrated circuits (logic, memory, power management and hardware security)
- Applications of emerging technologies (STTRAM, RRAM, PCMs, 3DIC)
- Data-centric computing systems (compute-in-memory, neuromorphic computing)

Education:

- **Purdue University**, West Lafayette, IN
 Ph.D. Electrical & Computer Engineering, 2009
 Dissertation: Low Voltage Robust Memory Circuit Design
 Advisor: Prof. Kaushik Roy
- **Indian Institute of Science (IISc)** Bangalore, India
 M. Tech. in Electronics Design and Technology, 2004
- **College of Engineering Pune (COEP)**, University of Pune, India
 B. E. in Electronics and Telecommunication Engineering, 2002

Work Experience:

- Assistant Professor, The University of Texas at Austin, TX August'17- Present
- Senior Staff Research Scientist, Intel Labs, Hillsboro, OR May'09 – July'17
- Research Assistant, Purdue University, W. Lafayette, IN Jul'05 – Apr'09
- Graduate Intern, Circuit Research Lab, Intel, Hillsboro, OR May'08 – Aug'08
- Graduate Intern, Technology Manufacturing Group, Intel, Hillsboro, OR May'07 – Aug'07
- Design Engineer, Cypress Semiconductor, Bangalore, India Jul'04 – May'05
- Graduate Researcher, Indian Institute of Science, Bangalore, India Jul'02 – May'05
- Graduate Intern, Texas Instruments, Bangalore, India Jan'04 – May'04
- Undergraduate intern, Cirrus Logic, Pune, India Jan'01 – Apr'02

Honors and Awards:

1. AMD development chair at the University of Texas at Austin (2017-present)
2. Industrial Distinguished Lecturer for IEEE Circuits and Systems (CAS) Society (2017)
3. SRC Mahboob Khan Outstanding Industry Liaison Award (2015)
4. IEEE Transactions on VLSI Systems Best Paper Award (2015)
5. IEEE Senior Member (2015)
6. Intel Corporation- 7 Divisional Recognition Awards
7. Intel Corporation- 4 Patent Recognition Awards
8. Outstanding Doctoral Dissertation Award by Purdue University's School of ECE (2010)
9. Intel Foundation Ph.D. Fellowship Award (2008-09)
10. Two SRC Inventor Recognition Awards (2008)
11. Best paper in session Award at SRC TECHCON (2008)
12. ISLPED Design Contest Award (2008)
13. Best M.Tech Student Award, CEDT Design Medal by IISc Bangalore (2004)
14. Pune University Junior and Senior year Top10 Award (2001, 2002)
15. National Talent Search (NTS) Scholarship by the Government of India (1996-2002)

Professional Activities:

1. Associate Editor, IEEE Solid State Circuits Letters, (2018-present)
2. Associate Editor, IEEE Transactions on VLSI systems, (2015-present)
3. Member of IEEE CAS Society – VLSI systems and applications technical committee (2015-present)
4. Senior Member – IEEE, Solid State Circuits, Circuits and Systems, and Electron Device Society
5. Conference Organization –
 - General co-chair, 2018, International Symposium on Low Power Electronics Design
 - Technical program co-chair, 2017 International Symposium on Low Power Electronics Design
6. Conference Technical Program Committee Member –
 - Design Automation Conference (DAC, 2018)
 - Asian Solid State Circuits Conference (A-SSCC, 2014-present)
 - International Conference on Computer Design (ICCD, 2017)
 - International Symposium on Circuits and Systems (ISCAS, 2016)
 - International Symposium on Low Power Electronics Design (ISLPED, 2013-2016)
 - Asian Symposium on Quality Electronics Design (ASQED, 2010-13)
7. Conference Service:
 - Best paper award committee member, VLSI Design Conference, India 2018
8. Senior Member – IEEE, Solid State Circuits, Circuits and Systems, and Electron Device Society
9. Member – Association of Computing machinery (ACM)
10. Industrial Liaison/Associate –
 - Stanford University - SystemX Alliance, Non-volatile Memory Technology Research Initiative (NMTRI)

- Semiconductor Research Corporation (SRC) – Integrated Circuits and Systems Track
- NSF program on Visual Cortex on Silicon (Penn State, MIT, USC, UCSD, UCLA, Stanford, Notre Dame, Univ. of Pittsburgh, York College)
- STARnet Research - Systems On Nanoscale Information fabriCs Center (SONIC); Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN); Center for Low Energy Systems Technology (LEAST)
- Technical Champion, Intel Academic Research Office program on “Post-CMOS Circuits and Architectures” (2010-2014)

11. Reviewer:

- IEEE Journal of Solid State Circuits,
- IEEE Transactions on Circuits and Systems – I and II,
- IEEE Transactions on VLSI Systems,
- VLSI Circuit Symposium,
- IEEE Transactions on Computers,
- IEEE Transactions on Electron Devices,
- IEEE Electron Device Letters,
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- ACM Journal on Emerging Technologies in Computing

Current graduate students:

1. Sai Subrahma Nibhanupudi, Ph.D. student, University of Texas at Austin (Fall'2017-)

Graduate Advisory Committee Member:

1. Heechai Kang, Thesis Title: “Broadband Receivers Employing Pulse-Width-Modulation”, Ph.D. Student University of Texas at Austin
2. Kenneth Ramclam, Thesis Title: “Low-Power and Robust Level-Shifter with Contention Mitigation for Memory and Standalone Applications” M.S. CSE, University of South Florida, March 2015
3. Anirudh Iyengar, Thesis Title: “Domain Wall Magnets for Embedded Memory and Hardware Security”, Ph.D. CSE, University of South Florida, Expected Graduation: 2017
4. Ankit Sharma, Thesis Title: “Sub-10nm Tunnel FETs” Ph.D. ECE, Purdue University, Expected Graduation: 2018

University Service:

1. Participated in junior faculty selection process, UT Austin, Fall 2018 term

Teaching:

1. VLSI-II, Spring 2018

Talks/Tutorials:

- T1. "Energy Efficient memory design for the compute continuum and beyond" UT Austin ECE Colloquium, November 2017
- T2. "Energy Efficient memories for ultra-low power IoT applications", Silicon Labs, Austin, TX, November 2017
- T3. "Energy Efficient memory design for the compute continuum and beyond" IEEE Santa Clara Valley Circuits and Systems Society, May, 2017
- T4. "Energy Efficient Memory Circuits: From IoT to Exascale Systems and Beyond", University of Southern California, April 2016
- T5. "Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications" Tutorial at Design, Automation and Test Conference (DATE), March 2015
- T6. "Process Adaptive Sub-threshold Design", Defense Advanced Research Projects Agency(DARPA), Washington D.C., October 2008
- T7. "Write Current Reduction in MRAMs using Tiny Spiral Inductors", 2008 International Solid State Circuits Conference (ISSCC), Student Forum, February 2008,
- T8. "Process Variation Tolerant SRAM Design for Ultra-Low Voltage Applications", Indian Institute of Science, Bangalore, January 2008
- T9. "Low-Power Robust CMOS Circuits for Scaled Technologies", SRC Integrated Circuits and Systems Sciences, University of Massachusetts, Amherst, October, 2007

Patents:

- P1. A. Bonetti, **J. P. Kulkarni**, C. Tokunaga, M. Cho, P. Meinerzhagen, and M. Khellah, "Tunable level shifter replicas for functionality and delay monitoring" approved for filing by Intel corporation
- P2. **J. P. Kulkarni**, and M. Khellah, "Column multiplexed bitline technique for high density single ended sensing arrays" approved for filing by Intel corporation
- P3. M. Cho, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, and J. Tschanz "Adaptive voltage system using logic TRC and bitcell retention Vmin monitor for aging guardband reduction and lower power over the design lifetime" approved for filing by Intel corporation
- P4. A. Thaploo, **J. Kulkarni**, B. Borole, A. Appu, A. Koker, K. Sinha, W. Fu, "System, apparatus and method for reducing voltage swing on an interconnect" filed, USPTO 15/488,673
- P5. **J. P. Kulkarni**, Y. Shim, and P. Meinerzhagen, "Apparatus and method for reducing di/dt" filed USPTO 15/163,494
- P6. **J. P. Kulkarni**, Y. Shim, P. Meinerzhagen, M. Khellah "Bi-directional, multi-mode charge pump" filed USPTO 15/81445
- P7. **J. P. Kulkarni**, I. Rajwani, and E. Donkoh, "Reduced swing bitline apparatus and method" filed USPTO 15/072,278
- P8. F. Sheikh, A. Sharma, and **J. P. Kulkarni**, "Fast Fourier transform architecture" filed PCT/US2015/66963
- P9. H. Bonakdar, **J.P. Kulkarni**, "Register files including distributed capacitor circuit blocks", filed USPTO, 14/937,010

- P10. Y. Shim, **J. P. Kulkarni**, P. Meinerzhagen, and M. Khellah, "di/dt reduction technique during primary power gate wake-up", filed USPTO, 14/951,343
- P11. **J. P. Kulkarni**, "Memory device including encoded data-line multiplexer" filed USPTO 14/ 859,884
- P12. **J. P. Kulkarni**, P. Kolar, A. Sharma, S. Chatterjee, K. Subramanian, F. Sheikh, W. H. Ma, "Capacitive wordline boosting" filed USPTO 14/752464
- P13. **J. P. Kulkarni**, A. Ravi, D. Somasekhar, G. Balamurugan, S. Shekhar, T. Musah, and T.-C. Hsueh "Digitally trimmable integrated resistors using resistive memory devices" filed USPTO 14/750,670
- P14. A. Trivedi, **J. P. Kulkarni**, D. Somasekhar, M. Khellah, C. Tokunaga, J. Tschanz, "Current Steering Level Shifter" USPTO 14/569,569.
- P15. A. Trivedi, **J. P. Kulkarni**, M. Khellah, C. Tokunaga, J. Tschanz, "Delta-Vdd aware Vmin assist techniques for ultra-low voltage level shifter" USPTO 14/553,934
- P16. **J. P. Kulkarni**, A. Thaploo, I. Rajwani, K. Koo, E. Karl, M. Khellah, "Assist circuit for memory" USPTO 14/229,767
- P17. **J. P. Kulkarni**, P. Meinerzhagen, D. Somasekhar, J. Tschanz, and V. De "Apparatus for charge recovery during low power mode" PCT/US2013/077277
- P18. **J. P. Kulkarni**, B. Geuskens, J. Tschanz, V. De and M. Khellah "Methods and systems to selectively boost an operating voltage of, and controls to an 8T bit-cell array and/or other logic blocks" PCT/US2012/030627
- P19. **J. P. Kulkarni**, K. Bowman, J. Tschanz and V. De "Resilient register file circuit for dynamic variation tolerance and method of operating the same" PCT/US2011/067632
- P20. J. Nasrullah, K. Kwan, **J. P. Kulkarni** and M. Khellah "Method and systems for energy efficiency and energy efficiency and energy conservation including entry and exit latency reduction for low power states", USPTO/13333753 and PCT/US2012/066652
- P21. I. Rajwani, S. Damaraju, N. Cooray, M. Khellah and **J. P. Kulkarni** "Memory array with extended write operation" USPTO/12642444
- P22. P. Meinerzhagen, **J. P. Kulkarni**, M. Khellah, C. Dray, D. Somasekhar, J. Tschanz and V. De "Apparatus for dual purpose charge pump" US Patent 9,230,636
- P23. **J. P. Kulkarni**, M. Khellah, J. Tschanz, B. Geuskens, and V. De "Apparatus for reducing write minimum supply voltage for memory" US patent 9,153,304
- P24. A. Raychowdhury, **J. P. Kulkarni**, and J. Tschanz "Multi-supply sequential logic unit" US patent 8,901,819
- P25. **J. P. Kulkarni**, D. Somasekhar "Low voltage swing repeater" US patent 8,847,633
- P26. C. Wilkerson, A. Alameldeen, and **J. P. Kulkarni**, "Adaptive self-repairing cache" US patent 8,719,502
- P27. **J. P. Kulkarni**, D. Somasekhar, J. Tschanz and V. De "Circuits and methods for memory" US patent 8488390 and PCT/US2012/032688
- P28. **J. P. Kulkarni**, M. Khellah, B. Geuskens, A. Raychowdhury, T. Karnik and V. De "Memory write operation methods and circuits" US patent 8467263 and PCT/US2011/040458, 2011
- P29. **J. P. Kulkarni** and K. Roy "Static random access memory cell and devices using the same", US patent 7952912

P30. **J. P. Kulkarni** and K. Roy “Memory cell with built-in process variation tolerance” US patent 7672152

Book / Book Chapters:

- B1. **J. P. Kulkarni**, J. Tschanz and V. De, “Energy-Efficient Volatile Memory Circuits” in Enabling the Internet of Things - from Circuits to Networks, Editor: Prof. Massimo Alioto, Springer, New York, ISBN: 978-3-319-51480-2
- B2. **J. P. Kulkarni** and K. Roy, “Technology/Circuit Co-design for III-V FETs” pp. 423-442, in Fundamentals of III-V Semiconductor MOSFETs, Springer, New-York 2010, ISBN: 978-1-4419-1546-7

Journal Papers:

- J1. S. Motaman, S. Ghosh, and **J. Kulkarni**, “VFAB: A Novel 2-Stage STTRAM Sensing Using Voltage Feedback and Boosting” IEEE Transactions on Circuits and Systems-I (**TCAS-I**), (accepted)
- J2. S. Motaman, S. Ghosh, and **J. Kulkarni**; “Impact of Process Variation on Self-Reference Sensing Scheme and Adaptive Current Modulation for Robust STTRAM Sensing” ACM Journal on Emerging Technologies in Computing Systems (JETC), pp. 1-17, Vol. 14, issue-1, November 2017
- J3. **J. P. Kulkarni**, J. Keane, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, “5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology” IEEE Journal of Solid State Circuits (**JSSC**) (special issue on ISSCC 2016), pp. 229-239, Vol. 52, No. 1, January 2017
- J4. M. Cho, S. Kim, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, V. De, “Post-Silicon Voltage Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating” accepted to IEEE Journal of Solid State Circuits (**JSSC**), (special issue on ISSCC 2016), pp. 50 – 63, Vol. 52, No. 1, January 2017
- J5. S. Srinivasa, A. Aziz, N. Shukla, X. Li, J. Sampson, S. Datta, J. P. Kulkarni, V. Narayanan, and S. Gupta, “Correlated Material Enhanced SRAMs with Robust Low Power Operation” IEEE Transactions on Electron Devices (**TED**), pp. 4744- 4752 Vol. 63, No. 12, December 2016
- J6. A. Sharma, A. A. Goud, J. P. Kulkarni, and K. Roy, “Source-underlapped GaSb-InAs TFETs with applications to Gain Cell Embedded DRAMs” IEEE Transactions on Electron Devices (**TED**), pp. 2563-2569, Vol 63, No. 6, June 2016
- J7. **J. P. Kulkarni**, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De, “A 409 GOPS/W Adaptive & Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin & Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature & Aging, IEEE Journal of Solid State Circuits (**JSSC**), pp. 117-129, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015
- J8. S. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. Ryan, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, and V. De, “Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally Controlled Fully Integrated Voltage Regulator” IEEE Journal of Solid State Circuits (**JSSC**), pp. 18-30, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015
- J9. R. Jain, B. Geuskens, M. Khellah, S. Kim, **J. Kulkarni**, J. Tschanz and V. De, “A 0.45-1V Fully Reconfigurable Switched Capacitor step down DC-DC converter with High Density MIM Capacitor in 22nm Tri-gate CMOS” IEEE Journal of Solid State Circuits (**JSSC**), pp. 1-11, vol. 49, No. 4, April 2014
- J10. R. Pandey, V. Saripalli, **J. P. Kulkarni**, S. Datta, “Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability”, IEEE Electron Device Letters (**EDL**), pp. 393-395, Vol 35, No. 3, March 2014

- J11. S. Gupta, **J.P. Kulkarni**, and K. Roy, "Tri-Mode Independent Gate FinFET based SRAM with Pass Gate Feedback: Technology-Circuit Co-design for Enhanced Cell Stability", IEEE Transactions on Electron Devices (**TED**), pp. 3696-3704, vol. 60, No. 11, November 2013
- J12. A. R. Alameldeen, N.S. Kim, S. M. Khan, H. R. Ghasemi, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, "Improving memory reliability power and performance using mixed cell designs" Intel Technology Journal (**ITJ**), pp. 36-53, vol. 17, issue 1, 2013
- J13. S. Gupta, **J.P. Kulkarni**, S. Datta and K. Roy, "Process-Variation Tolerant Heterojunction Intra-band Tunnel (HIBT) FETs for Low Voltage SRAMs", IEEE Transactions on Electron Devices (**TED**), pp. 3533-3542, vol. 59, No. 12, December 2012
- J14. **J. P. Kulkarni** and K. Roy, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design" IEEE Transactions on VLSI systems (**TVLSI**), pp. 319-332, vol. 20, No. 2, February 2012 (**2015 IEEE TVLSI best paper award, Top-25 most downloaded TVLSI manuscript for the year 2012**)
- J15. **J. P. Kulkarni**, A. Goel, P. Ndai and K. Roy, "Read-Disturb-Free, Differential Sensing 1R/1W Port 8T Bitcell Array" IEEE Transactions on VLSI systems (**TVLSI**), pp. 1727-1730, Vol. 19, Issue: 9, September 2011
- J16. M. Meterelliyoz, P. Song, F. Stellari, **J. P. Kulkarni** and K. Roy, "Characterization of Random Process Variations using Ultra Low Power High Sensitivity, Bias Free Sub-threshold Process Sensor" IEEE Transactions on Circuits and Systems-I (**TCAS-I**), pp. 1838-1847, Vol. 57, Issue:8, August 2010
- J17. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits" IEEE Transactions on Magnetics (**TMAG**), pp. 1898-1901, vol. 46, No. 6, June 2010
- J18. M. Meterelliyoz, **J. P. Kulkarni** and K. Roy, "Analysis of SRAM and eDRAM Cache Memories under Spatial Temperature Variations" IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (**TCAD**), pp. 2-13, Vol. 29, Issue 1, January 2010
- J19. **J. P. Kulkarni** and K. Roy, "Technology Circuit Co-design for Ultra-Fast InSb Quantum Well Transistors", IEEE Transactions on Electron Devices (**TED**), pp. 2537-2545, Vol. 55, October 2008
- J20. Q. Cao, H.-S. Kim, N. Pimparkar, **J. P. Kulkarni**, C. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers, "Medium Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates" pp. 495-500, **Nature**, vol. 454, 24th July 2008
- J21. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Robust Schmitt Trigger based Sub-threshold SRAM" IEEE Journal of Solid State Circuits (**JSSC**), pp. 2304-2313, Vol. 42, No. 10, October 2007

Conference Papers:

- C1. P. Meinerzhagen, C. Tokunaga, A. Malavasi, V. Vaidya, **J. Kulkarni**, C. Augustine, M. Cho, S. Kim, G. Matthew, R. Jain, K. Ravichandran, M. Khellah, J. Tschanz, and V. De, "Improving energy/performance of a 14nm graphics technology (GT) processor using fast fine-grain DVFS with hybrid DLDO/SCVR, execution unit micro-turbo, retentive sleep, and Vmin reduction" International Solid State Circuits Conference, February 2018 (accepted)
- C2. **J. P. Kulkarni**, C. Tokunaga, M. Cho, M. M. Khellah, J. W. Tschanz, and V. K. De "F_{MAX} / V_{MIN} and noise margin impacts of aging on domino read, static write, and retention of 8T 1R1W SRAM arrays in 22nm high-k/metal-gate tri-gate CMOS" VLSI Circuit Symposium (**VLSI Symposium**), pp. 116-117, June 2017
- C3. **J. P. Kulkarni**, C. Tokunaga, C. Augustine, M. Khellah, J. Tschanz and V. De, "Adaptive and resilient high-performance memory design for dynamic variation tolerance" VLSI Test Symposium, April 2017 (**Invited paper**)

- C4. J. Keane, **J. Kulkarni**, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, "5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology" International Solid State Circuits Conference (**ISSCC**), pp. 308-309, Feb. 2016
- C5. M. Cho, S. Kim, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, V. De, "Post-Silicon Voltage Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating" International Solid State Circuits Conference (**ISSCC**) pp. 152-153, February 2016
- C6. **J. P. Kulkarni**, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De, "A 409 GOPS/W Adaptive & Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin & Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature & Aging" International Solid State Circuits Conference (**ISSCC**), pp. 82-83, February 2015
- C7. S. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. Ryan, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, and V. De, "Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally-Controlled Hybrid LDO/Switched-Capacitor VR with Fast Droop Mitigation" International Solid State Circuits Conference (**ISSCC**), pp. 154-155, February 2015
- C8. S. Motaman, S. Ghosh, and **J. Kulkarni**, "A Novel Slope Detection Technique for Robust STTRAM Sensing" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 7-12, July 2015
- C9. C. Tokunaga, J. Ryan, C. Augustine, **J. Kulkarni**, Y. Shih, S. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. Khellah, J. Tschanz, V. De, "A 22nm Graphics Execution Core with Wide Voltage Range and 40% Higher Peak GFLOPS/W via Adaptive Clocking, Selective Boosting, and State-Retentive Sleep" International Solid State Circuits Conference (**ISSCC**), pp. 108-109, February 2014
- C10. **J.P. Kulkarni**, M. Khellah, J. Tschanz, B. Geuskens, R. Jain, S. Kim and V. De, "Dual-Vcc 8T-bitcell SRAM Array in 22nm Tri-gate CMOS for energy efficient operation across wide dynamic voltage range" VLSI Circuit Symposium (**VLSI Symp**), pp. C126-C127, June 2013, (**Conference highlight paper**)
- C11. R. Jain, B. Geuskens, M. Khellah, S. Kim, **J. Kulkarni**, J. Tschanz and V. De, "A 0.45-1V Fully Reconfigurable Switched Capacitor step down DC-DC converter with High Density MIM Capacitor in 22nm Tri-gate CMOS" VLSI Circuit Symposium (**VLSI Symp**), pp. C174-C175, June 2013 (**Conference highlight paper**)
- C12. S. M. Khan, A. R. Alameldeen, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, "Improving Multi-Core Performance Using Mixed-Cell Cache Architecture", International Symposium on High Performance Computer Architecture (**HPCA**), pp. 229-230, February 2013
- C13. **J. Kulkarni**, B. Geuskens, T. Karnik, M. Khellah, J. Tschanz and V. De, "Capacitive-Coupling Wordline Boosting with Self-Induced V_{CC} Collapse for Write V_{MIN} Reduction in 22-nm 8T SRAM" International Solid State Circuits Conference (**ISSCC**), pp. 234-235, February 2012
- C14. M. Nicolaidis, L. Anghel, N. Zergainoh, Y. Zorian T. Karnik, J. Tschanz, **J. Kulkarni**, K. Bowman, M. Khellah, A. Raychowdhury, C. Tokunaga, S-L Lu, and V. De, "Designing Reliable Processor Cores" Design Automation and Test in Europe (**DATE**), March 2012 (invited paper)
- C15. S. Gupta, **J.P. Kulkarni**, S. Datta and K. Roy, "Dopant Straggle-free Heterojunction Intra-band Tunneling (HIBT) FETs with Abrupt Source/Drain Junctions, Low Drain-induced Barrier Lowering/Thinning and Reduced Variation in OFF current" 2012 Device Research Conference (**DRC**), June 2012

- C16. V. Saripalli, S. Datta, V. Narayanan, and **J.P. Kulkarni**, "Variation-Tolerant Ultra low-power Hetero-junction Tunnel FET SRAM Design" 7th International Symposium on Nanoscale Architectures (**NANOARCH**), pp. 45-52, June 2011
- C17. B. Geuskens, M. Khellah, **J. Kulkarni**, T. Karnik and V. De "Opportunities for PMOS Read and Write Ports in Low Voltage Dual-Port 8T Bit-Cell Arrays" Custom Integrated Circuits Conference (**CICC**), pp. 1-4, September 2010
- C18. A. Raychowdhury, B. Geuskens, **J. Kulkarni**, J. Tschanz, K. Bowman, T. Karnik, S.-L. Lu, V. De and M. Khellah, "PVT & Aging Adaptive Word-Line Boosting for 8T SRAM Power reduction" International Solid State Circuits Conference (**ISSCC**), pp. 352-353, February 2010
- C19. M. Meterelliyoz, A. Goel, **J. P. Kulkarni** and K. Roy, "Accurate Characterization of Random Process Variations Using a Robust Low-Voltage High-Sensitivity Sensor Featuring Replica-Bias Circuit" International Solid State Circuits Conference (**ISSCC**), pp. 186-187, February 2010
- C20. J. Tschanz, K. Bowman, M. Khellah, C. Wilkerson, B. Geuskens, D. Somasekhar, A. Raychowdhury, **J. Kulkarni**, C. Tokunaga, S.-L. Lu, T. Karnik, V. De, "Resilient Design in Scaled CMOS for Energy Efficiency" Asia Pacific Design Automation Conference (**ASP-DAC**), pp. 625-625, January 2010 (Invited paper)
- C21. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits" International Magnetism Conference (**INTERMAG**), January 2010
- C22. K. Roy, **J. Kulkarni** and M.E. Hwang, "Low Voltage Process Adaptive Logic and Memory Arrays for Ultra-low Power Sensor Nodes" 8th IEEE **Sensors** Conference, pp. 185-188, October 2009 (Invited paper)
- C23. A. Goel, P. Ndai, **J. P. Kulkarni** and K. Roy, "Read/Access-Preferred (REAP) SRAM – Architecture-Aware Bit Cell Design for Improved Yield and Lower V_{min} " Custom Integrated Circuits Conference (**CICC**), September 2009
- C24. K. Roy, **J.P. Kulkarni**, S. Gupta, "Device/Circuit Interactions at 22nm Technology node" Design Automation Conference (**DAC**), pp.97-102, July 2009
- C25. M. Meterolliyez, P. Song, F. Stellari, **J. P. Kulkarni** and K. Roy, "A High Sensitivity Process Variation Sensor utilizing Sub-threshold operation" Custom Integrated Circuits conference (**CICC**), pp. 125-128, September 2008
- C26. **J. P. Kulkarni** and K. Roy, "Process Variation Tolerant SRAM Design for Ultra Low Voltage Applications" **SRC TECHCON**, November 2008 (Best paper in session Award)
- C27. K. Roy, **J.P. Kulkarni** and M.E. Hwang, "Process Adaptive Digital Sub-threshold Logic and Memory" 16th International Conference on Very Large Scale Integration (**VLSI-SOC**), pp. 42-45, October 2008 (Invited paper)
- C28. **J. P. Kulkarni**, K. Kim, S. Park and K. Roy, "Process Variation Tolerant SRAM Array for Ultra Low Voltage Applications" Design Automation Conference (**DAC**), pp. 108-113, June 2008
- C29. K. Roy, **J.P. Kulkarni**, M.E. Hwang, A. Raychowdhury and K. Kim, "Process Variation Tolerant Digital Sub-threshold Design" 33rd Annual Government Microcircuit Applications and critical Technology Conference (**GOMACTech**), March 2008
- C30. K. Roy, **J.P. Kulkarni** and M.E. Hwang, "Process Tolerant Ultra-Low Voltage Digital Sub-threshold Design" 8th topical meeting on silicon monolithic integrated circuits in RF systems, (**SIRF**), pp.42-45 January 2008 (Invited paper)
- C31. M. Meterolliyez, **J. P. Kulkarni** and K. Roy, "Thermal Analysis of 8-T SRAM for Nano-scaled Technologies" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 123-128, August 2008

- C32. **J. P. Kulkarni**, M. Meterolliyev, K. Roy and J. Murthy, "Nano-scaled SRAM Thermal Stability Analysis using Hierarchical Compact Thermal Models" **iTHERM**, pp. 999-1005, May 2008
- C33. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Fully Differential Robust Schmitt Trigger based Sub-threshold SRAM" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 171-176, August 2007
- C34. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Fully Differential Robust Schmitt Trigger based Sub-threshold SRAM" **SRC TECHCON** 2007
- C35. **J. P. Kulkarni** and K. Roy "A High Performance Scalable Multiplexed Keeper Technique" 2007 International Symposium on Quality Electronics Design (**ISQED**), pp. 545-549, March 2007
- C36. **J. P. Kulkarni** and N. Bhat, "Effect of Poly-Si Gate Depletion on Tuning Range of MOS Varactors" Device Research Conference (**DRC**), pp. 81-82, June 2006
- C37. **J. P. Kulkarni** and N. Bhat, "Process Technique for Improving Tuning range in Varactors using Poly-Silicon Depletion effect" Asia Pacific Microwave Conference (**APMC**), December 2004
- C38. **J. P. Kulkarni** and N. Bhat, "Process Technique for Improving Tuning range in MOS Varactors" Proceedings of the IEEE **INDICON**, pp. 534-537, 2004
- C39. S. Kibey, **J. P. Kulkarni** and P. Sarode "A fast LSF search algorithm based on inter-frame correlation in G.723.1" EURASIP Journal of Applied Signal Processing, Vol. 11, July 2004
- C40. A. Pugalia, **J. P. Kulkarni**, N. Bhargava and N. Bhat "Single pocket Halo Sensitivity in 100nm Analog Transistor Design" Intl. Workshop on Physics of Semiconductor Devices (**IWPSD**), pp. 611-613, December 2003