A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM

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***Abstract*—We propose a novel Schmitt Trigger (ST) based differential 10-transistor SRAM (Static Random Access Memory) bitcell suitable for subthreshold operation. The proposed Schmitt trigger based bitcell achieves 1.56× higher read static noise margin (SNM) (V_{DD} = 400 mV) compared to the conventional 6T cell. The robust Schmitt trigger based memory cell exhibits built-in process variation tolerance that gives tight SNM distribution across the process corners. It utilizes differential operation and hence does not require any architectural changes from the present 6T architecture. At iso-area and iso-read-failure probability the proposed memory bitcell operates at a lower (175 mV) V_{DD} with 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 6T cell. Simulation results show that the proposed memory bitcell retains data at a supply voltage of 150 mV. Functional SRAM with the proposed memory bitcell is demonstrated at 160 mV in 0.13 μm CMOS technology.**

***Index Terms*—Low power SRAM, low voltage SRAM, process variations, Schmitt trigger, subthreshold SRAM.**

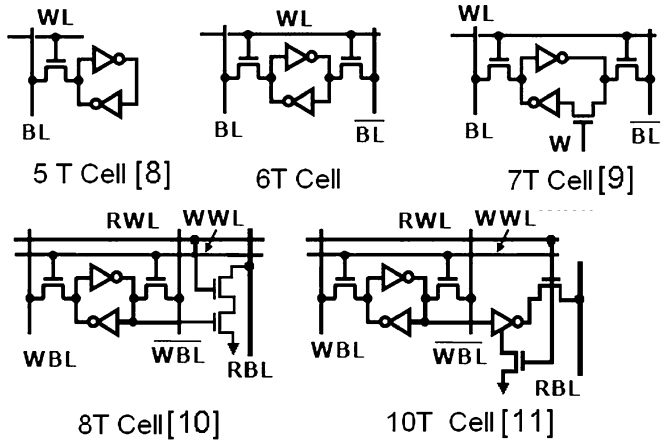

Fig. 1. Various SRAM bitcells [8]–[11].

I. Introduction

AGGRESSIVE scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance. Leakage current increases with the scaling of the device dimensions. Increased integration density along with the increased leakage necessities ultralow-power operation in the present power constrained design environment. The power requirement for battery-operated devices such as cell phones and medical devices is even more stringent. Reducing the supply voltage reduces the dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of low-power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [1]. However, as the supply voltage is reduced, the sensitivity of the circuit parameters to process variations increases [2]. Process variations limit the circuit operation in the subthreshold region, particularly the memories [2], [3]. Embedded cache memories are expected to occupy 90% of the total die area of a system-on-a-chip (SoC) [2]. Nanoscaled SRAM bitcells having minimum-sized transistors are vulnerable to inter-die as well as intra-die process variations. Intra-die process variations include random dopant fluctuation (RDF) and line edge roughness (LER), etc. This may result in a threshold voltage mismatch between the adjacent transistors in a memory cell [4]. Coupled with inter-die and intra-die process variations, lower supply voltage operation results in various memory failures, i.e., read failure, hold failure, access time failure, and write failure [4]. Memory failure probability is predicted to be higher in the future technology nodes [5]. Adaptive circuit techniques such as source biasing, and dynamic V_{DD} have been proposed to improve the process variation tolerance [6]. Self-calibration techniques to achieve low-voltage operation while keeping the failure probability under control have also been proposed [7]. The 6-transistor (6T) cell which uses a cross-coupled inverter pair is the *de facto* memory bitcell used in the current SRAM designs. Different types of SRAM bitcells have been proposed to improve the memory failure probability at a given supply voltage (Fig. 1). 6T and 7T bitcells utilize differential read operation while 5T, 8T, and 10T bitcells employ the single-ended reading scheme. The 8T and 10T cells use an extra sensing circuit for reading the cell contents, achieving improved read stability. A detailed comparison of various SRAM bitcells is shown in Table I. Recently, a memory cell with single-ended read operation and operating at 103 mV supply voltage has been reported [12].

For a stable SRAM bitcell operating at lower supply voltages, the stability of the inverter pair should be improved. None of the aforementioned bitcells has a mechanism to improve the stability of the inverter pair under process variations. We propose a Schmitt trigger based differential bitcell having built-in feedback mechanism for improved process variation tolerance.

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TABLE I
COMPARISON OF VARIOUS SRAM BITCELLS

Sr. No.	5T [8]	6T	7T[9]	8T[10]	10T[11]
Read	Single Ended	Differential	Differential	Single Ended	Single Ended
#WL	1	1	1	2	2
#BL	1	2	2	3	3
Area	0.8	1	--	1.3	1.66
#PMOS	2	2	2	2	3
#NMOS in Read Path	2	2	2 or 3	2	3

In particular:

1) We have proposed a novel Schmitt trigger based, differential, 10-transistor SRAM bitcell with built-in feedback mechanism. It requires no architectural change compared to the 6T cell architecture. It can be used as a drop-in replacement for present 6T based designs.
2) We have demonstrated that with respect to 6T cell, the proposed Schmitt trigger based bitcell gives better read stability, better write-ability, improved process variation tolerance, lower read failure probability, low-voltage/low-power operation, and improved data retention capability at ultralow voltage.
3) We have fabricated a test chip in 0.13 μm logic process technology and validated the proposed technique. An SRAM array containing the proposed memory bitcell is functional at 160 mV of supply voltage.

To maintain the clarity of the discussion, the "10T cell" is referred as the memory cell reported in [11]. The proposed Schmitt Trigger (ST) based 10T memory cell is referred as the "ST bitcell" hereafter. The rest of this paper is organized as follows. In Section II, the proposed ST bitcell operation is described. In Section III, comparison is made among 6T/8T/10T/ST bitcells for various SRAM metrics. Measurement results are discussed in Section IV. Section V concludes the paper.

II. SCHMITT TRIGGER BASED 10-TRANSISTOR SRAM BITCELL

The proposed ST 10-transistor SRAM cell focuses on making the basic inverter pair of the memory cell robust. At very low voltages, the cross-coupled inverter pair stability is of concern. To improve the inverter characteristics, Schmitt trigger configuration is used. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition [13]. This adaptation is achieved with the help of a feedback mechanism. One possible implementation of a Schmitt trigger is shown in Fig. 2(a). This structure is used to form the inverter of our memory bitcell. The basic Schmitt trigger requires six transistors instead of two transistors to form an inverter. Thus, it would need 14 transistors in total to form an SRAM cell, which would result in large area penalty. Since PMOS transistors are used as weak pull-ups to hold the "1" state, a feedback mechanism in the PMOS pull-up branch is not used.

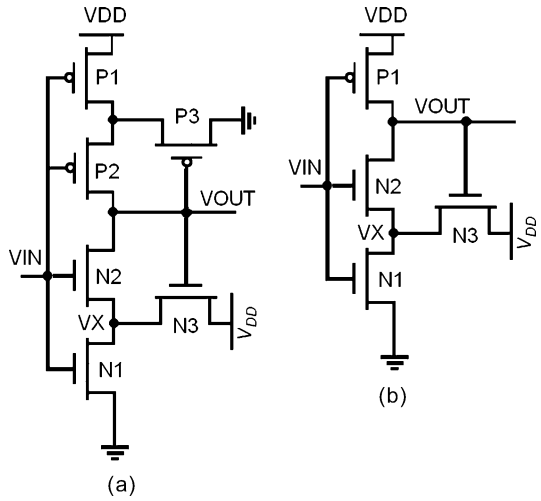

Fig. 2. (a) Schmitt trigger. (b) Modified Schmitt trigger.

Feedback mechanism is used only in the pull-down path. The modified Schmitt trigger schematic is shown in Fig. 2(b).

A. Schmitt Trigger Based 10-Transistor SRAM Bitcell

The complete schematic for the proposed ST bitcell is shown in Fig. 3(a). Transistors PL-NL1-NL2-NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. AXL and AXR are the access transistors. The positive feedback from NFL/NFR adaptively changes the switching threshold of the inverter depending on the direction of input transition. During a read operation (with say $V_{\rm L} = 0$ and $V_{\rm R} = V_{\rm DD}$), due to voltage divider action between the access transistor and the pull-down NMOS, the voltage of $V_{\rm L}$ node rises. If this voltage is higher than the switching threshold (trip point) of the other inverter, the contents of the cell can be flipped, resulting in a read failure event [4]. In order to avoid a read failure, the feedback mechanism should increase the switching threshold of the inverter PR-NR1-NR2. Transistors NFR and NR2 raise the voltage at node $V_{\rm NR}$ and increase the switching threshold of the inverter storing "1". Thus, Schmitt trigger action is used to preserve the logic "1" state of the memory cell. The proposed ST bitcell utilizes differential operation, giving better noise immunity [13]. It requires no architectural change compared to the conventional

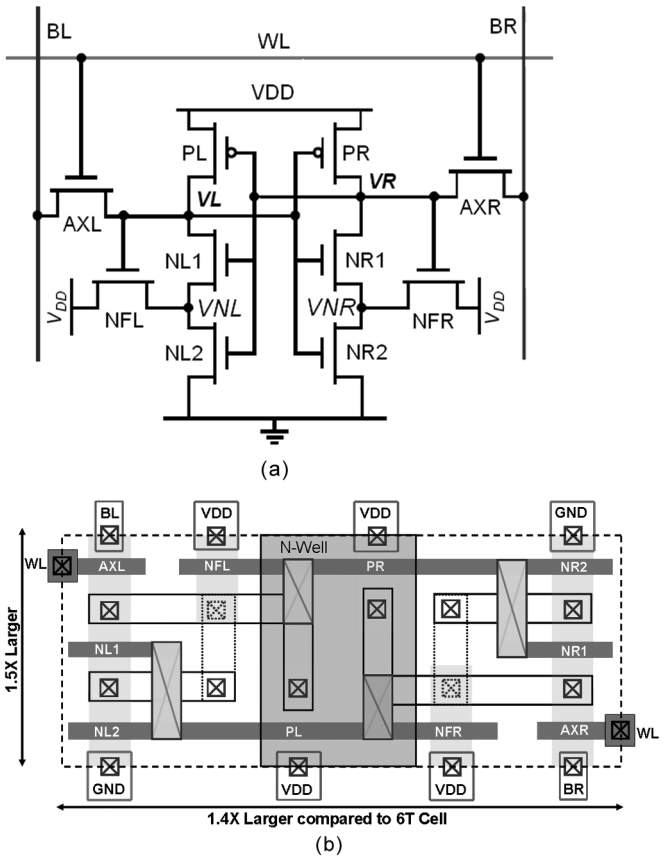

Fig. 3. (a) Schmitt trigger based 10-transistor SRAM bitcell. (b) Schmitt trigger based SRAM bitcell layout.

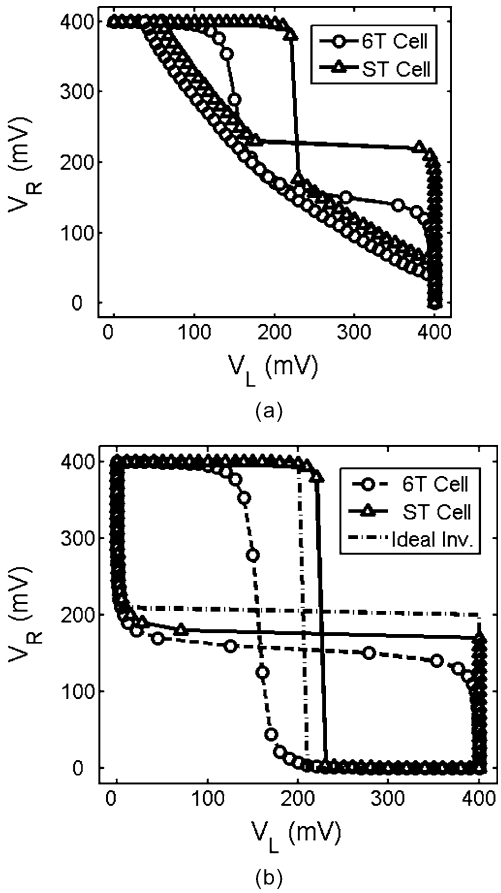

Fig. 4. Inverter characteristics. $V_{\rm DD}$ = 400 mV. (a) Read mode. (b) Hold mode.

6T cell architecture and hence can be used as a drop-in replacement for the present 6T based designs.

The proposed ST bitcell has two PMOS transistors and eight NMOS transistors. Pull-up transistors PL and PR share the same N-well. As the number of PMOS transistors is the same as the 6T cell, the N-well area consumed by ST bitcell could be same as the conventional 6T cell. Fig. 3(b) shows one possible "thin cell" layout for the proposed ST bitcell. The conventional 6T cell requires four columns of active regions, whereas the proposed ST bitcell requires six columns of the active region. The extra columns of the active region have minimum width. Horizontal dimension is increased by ∼40% compared to the 6T cell. Since the read path has three NMOS transistors in series, it results in 50% increase in vertical dimension. Thus, the proposed ST bitcell consumes $\sim 2.1\times$ larger area compared to nominal 6T cell. $V_{\rm DD}$, $V_{\rm GND}$, BL, BR, and WL contacts are shared between neighboring cells.

III. Simulation Results

HSPICE simulations are done using 0.13 μm logic process technology. Typical NMOS (PMOS) $V_{\rm T}$ is 350 mV (300 mV). The 6T/8T/10T and the proposed ST bitcells are compared for various SRAM metrics. For the 6T cell, the transistor widths $\rm W_{PU}/W_{AX}/W_{PD}$ are 160nm/240nm/320nm, respectively. For the ST bitcell, extra transistors NFL/NL2 are of minimum width (160 nm) while the other transistors have the same dimensions as those of the 6T cell.

A. Read Stability

For improving the cell stability, the proposed ST bitcell focuses on making the inverter pair robust. Feedback transistors NFL/NFR increase the inverter switching threshold whenever the node storing "1" is discharged to the "0" state. Thus, cell asymmetry changes based on the direction of the node voltage transition. Fig. 4(b) shows the inverter characteristics indicating the cell asymmetry. When $V_{\rm L}$ is increased from 0 to $V_{\rm DD}$, the other node $(V_{\rm R})$ makes a transition from $V_{\rm DD}$ to 0. During this time, the feedback mechanism due to NFR-NR2 raises the node voltage $V_{\rm NR}$ and tries to maintain the logic "1" state of the $V_{\rm R}$ node. This gives near-ideal inverter characteristics essential for robust memory cell operation. The static noise margin (SNM) is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [14]. The ST bitcell has 1.56× improvement in the read SNM, compared to the conventional 6T counterpart, shown in Fig. 4(a) ($V_{\rm DD}$ = 400 mV).

Since the proposed ST bitcell consumes more area ($\sim 2\times$) compared to the 6T cell, it is worthwhile to compare these cells under "iso-area" condition. For iso-area condition, the cell ratio $(\rm W_{PD}/W_{AX})$ in the 6T cell is increased so as to have same area as that of the ST bitcell. Under iso-area condition, the minimum-sized ST bitcell gives 1.52× improvement in read SNM over the 6T cell ($V_{\rm DD}$ = 400 mV), shown in Fig. 5. At higher supply voltages (i.e., in super-threshold regime), the drain current varies

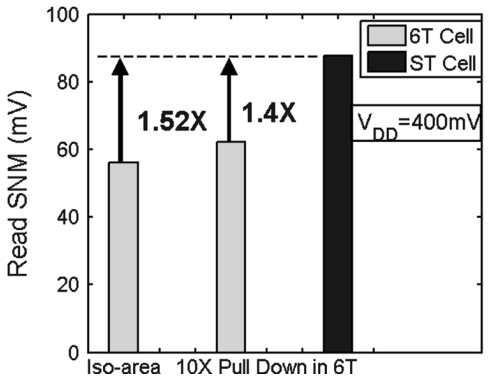

Fig. 5. Read SNM, iso-area comparison.

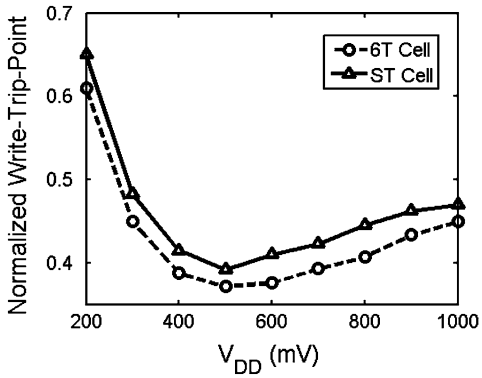

Fig. 6. Normalized write-trip-point versus $V_{\rm DD}$.

linearly with the gate voltage. Transistor upsizing increases the SNM considerably. However, in the subthreshold regime, drain current depends exponentially on the gate voltage. Any device upsizing will result in marginal change in the drain current. Thus, in the subthreshold region, SNM is relatively independent of the device sizing [15]. Even with $10\times$ increased cell ratio $(\mathrm{W_{PD}/W_{AX}})$ in the 6T cell, the proposed minimum-area ST bitcell shows $1.4\times$ improvement in the read SNM, shown in Fig. 5. This shows that for a stable SRAM cell operating at a lower supply voltage, a feedback mechanism can be more effective than simple transistor upsizing as in a conventional 6T cell.

B. Write-ability

Write-ability of a bitcell gives an indication of how easy or difficult it is to write to the cell. Write-trip-point defines the maximum bitline voltage $(V_{\rm BL}^{\rm MAX})$ needed to flip the cell content [16]. The higher the bitline voltage, the easier it is to write to the cell. Normalized write-trip-point is defined as

$$\text{Normalized Write-Trip-Point} = \left[\frac{V_{\rm BL}^{\rm MAX}}{V_{\rm DD}}\right].$$

Initially consider $V_{\rm L}$ = "0" and $V_{\rm R}$ = "1". In order to write a "0" to node $V_{\rm R}$, BR is pulled down to ground, BL is kept at $V_{\rm DD}$, and wordline is turned ON. The voltage at node $V_{\rm R}$ is determined by the size of the pull-up transistor (PR) and the access transistor (AXR). The other node $V_{\rm L}$ is transitioning from "0" state to "1" state. During this transition, the feedback transistor (NFL) is OFF. This results in the reduced pull-down transistor strength at node $V_{\rm L}$ due to stacked (series connected NL1–NL2) NMOS transistors. Compared to the 6T cell, the effective strength of pull-down transistor is reduced in the ST bitcell during $1 \rightarrow 0$ input transition. Hence, the node storing "0" $(V_{\rm L})$ is flipped at a much higher voltage, giving a higher write-trip-point compared to the 6T cell shown in Fig. 6. Unlike the conventional 6T cell, the ST bitcell gives better read stability as well as better write-ability. Schmitt trigger action gives better read stability while reduced pull-down strength (series connected NMOS) and absence of feedback during $1 \rightarrow 0$ input transition enables the ST bitcell to achieve better write-ability than the 6T cell.

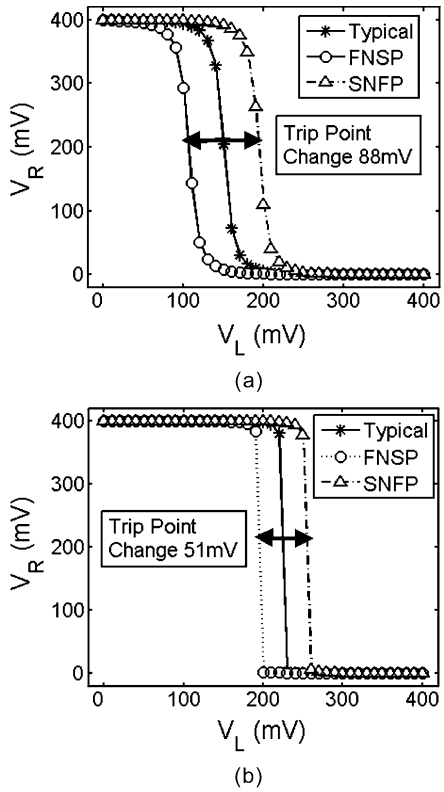

Fig. 7. Switching threshold comparison for $0 \rightarrow 1$ input transition. (a) 6T bitcell. (b) ST bitcell.

C. Process Variation Tolerance

The proposed ST bitcell has a built-in process variation tolerance. Fig. 7 shows the inverter voltage transfer characteristics (during a $0 \rightarrow 1$ input transition) for a standard 6T cell and the proposed ST bitcell for typical and skewed process corners. (FNSP = Fast NMOS and Slow PMOS; SNFP = Slow NMOS and Fast PMOS). As $V_{\rm L}$ varies from $V_{\rm GND}$ to $V_{\rm DD}$ the feedback transistor NFR raises the node voltage $V_{\rm NR}$ above $V_{\rm GND}$. It increases the switching threshold when $V_{\rm R}$ is transitioning from "1" state to "0" state. This results in sharp inverter characteristics shown in Fig. 7(b). In a Fast NMOS process corner, threshold voltage of NMOS (NFR) would reduce. This would increase the intermediate node voltage $(V_{\rm NR})$ closer towards $V_{\rm DD}$ and would increase the switching threshold of the inverter compared to the 6T cell. Similarly for

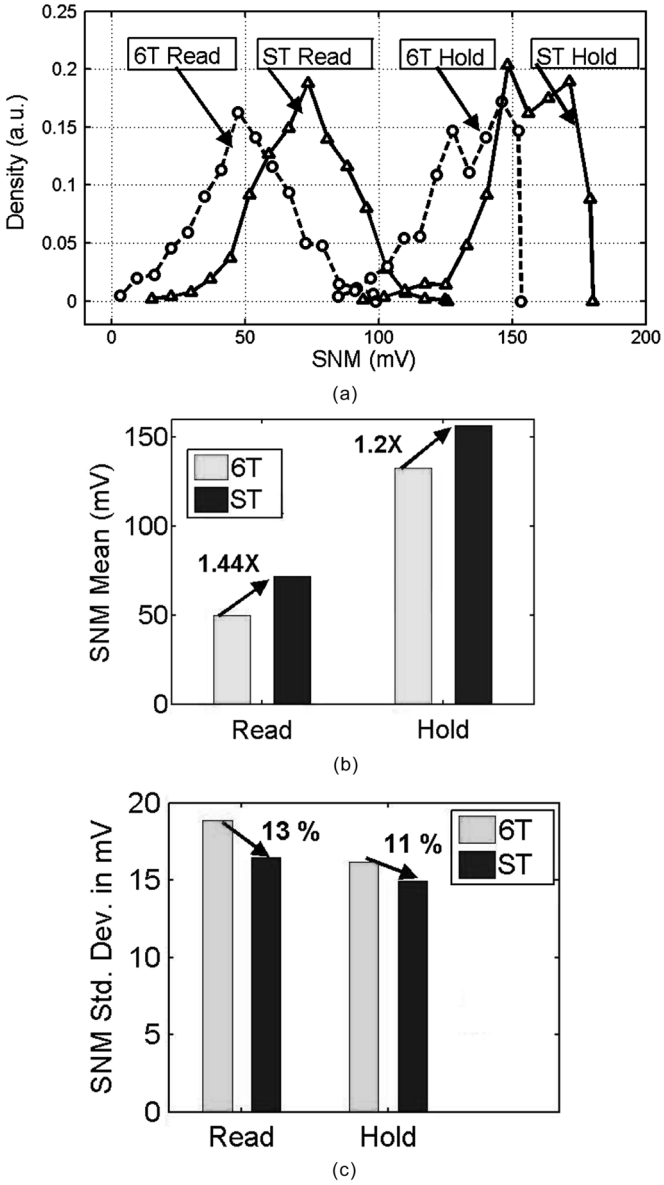

Fig. 8. SNM comparisons, Monte Carlo simulation. (a) Read/hold SNM distribution. (b) Mean SNM value. (c) Std. deviation in SNM.

a slow NMOS corner, NMOS (NFR) $V_{\rm T}$ would increase and switching threshold would be reduced compared to the 6T cell. The variation in switching threshold is 51 mV in the ST bitcell compared to 88 mV in the 6T cell indicating improved process variation tolerance (Fig. 7).

In order to evaluate the effectiveness of the ST bitcell under process variations, Monte Carlo simulations ($V_{\rm DD} = 400$ mV) are done for read and hold case. It is observed that the proposed ST bitcell gives higher mean read (hold) SNM 1.44× (1.22×) compared to the 6T cell shown in Fig. 8. Further, standard deviation in read (hold) SNM is reduced by 13% (11%) compared to the standard 6T cell ($V_{\rm DD} = 400$ mV).

D. Read Failure Probability

Supply voltage is reduced gradually from the nominal value of 1.0 V to the point where memory cell contents are about to flip or reach a metastable point. For estimating the minimum $V_{\rm DD}$ required during read operation, 25 000 Monte Carlo simulations are done. The distribution of minimum $V_{\rm DD}$ required to avoid a read failure is shown in Fig. 9. The tail of the matched distribution is shown in the inset. The proposed ST bitcell requires 24% lower average $V_{\rm DD}$ with 39% reduced standard deviation than the 6T cell. Based on the minimum $V_{\rm DD}$ distributions, cumulative distributive functions (CDF) are calculated and the minimum $V_{\rm DD}$ required for a given read failure probability is estimated. It is observed that, at iso-read-failure probability, the ST bitcell operates at a lower voltage than the conventional 6T cell. Minimum $V_{\rm DD}$ versus the read failure probability is shown in Fig. 10. Due to reduced $V_{\rm DD}$, the ST bitcell consumes lower leakage power compared to the 6T cell despite four extra transistors. As the access transistor size in the ST bitcell is the same as the 6T cell, the bit-line diffusion capacitance and word-line gate capacitance is unchanged. This reduces read/write dynamic power dissipation quadratically ($C_{\rm L}V_{\rm DD}^2{\rm f}$) with reduced $V_{\rm DD}$. Note that the difference in minimum $V_{\rm DD}$ increases as the read failure probability decreases.

Again, Monte Carlo simulations are done for a read operation under iso-area condition. The minimum $V_{\rm DD}$ required to avoid a read failure at iso-area and iso-read-failure probability (for this example 10^{-6}) show that, the proposed ST bitcell operates at 175 mV lower supply voltage than the 6T cell. The ST bitcell operating at a lower supply voltage gives 18% saving in the leakage power and 50% savings in the dynamic power (at read failure probability of 10^{-6}) shown in Fig. 11.

E. Scalability

Using predictive technology models, the proposed ST bitcell is compared with the 6T cell to verify the effectiveness of our technique in scaled technologies [17]. The ST bitcell consistently predicts better read and hold SNM compared to the 6T cell in scaled technologies. For 32 nm technology, using predictive models, the ST bitcell predicts 1.53× improvement in read SNM compared to its 6T counterpart ($V_{\rm DD} = 400$ mV) shown in Fig. 12 [17], [18]. Thus, the proposed ST bitcell can be scalable into future technologies. As technology scales, with increased process variations, the memory cell failure probability would worsen at lower supply voltages. In such a scenario, the proposed ST bitcell with built-in feedback mechanism could be useful for low $V_{\rm DD}$ operation.

F. Ultralow-Voltage Operation

During the standby mode, the supply voltage of a memory array is reduced to minimize the leakage power. However, the supply voltage cannot be reduced arbitrarily as memory bitcells would not be able to hold the contents of the cell. This voltage is termed data retention voltage (DRV) [19]. The 6T/8T/10T/ST bitcells are compared for Hold SNM at low supply voltages. As 6T, 8T, and 10T cells use the same inverter pair, they would show almost the same characteristics in hold mode. Fig. 13 shows the inverter characteristics for 6T/8T/10T and the proposed ST bitcells at ultralow $V_{\rm DD}$ (150 mV). It is clearly seen that the proposed ST bitcell exhibits superior transfer characteristics to 6T/8T/10T cells. In 0.13 μm technology, the hold SNM for 6T/8T/10T cells is 18 mV, while the proposed ST bitcell exhibits 42 mV hold SNM (2.3× better) [Fig. 13(a)]. Similarly, for

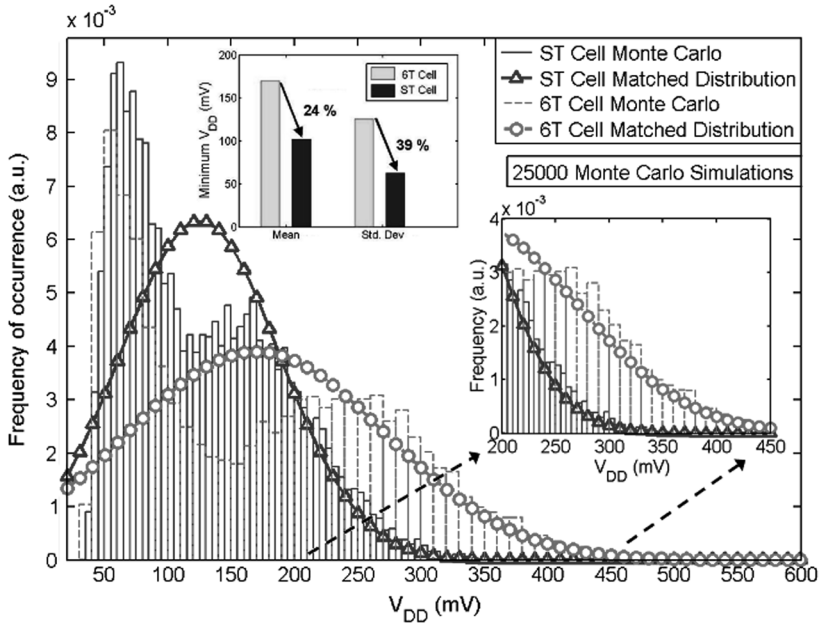

Fig. 9. Minimum $V_{\rm DD}$ comparison, MC simulation.

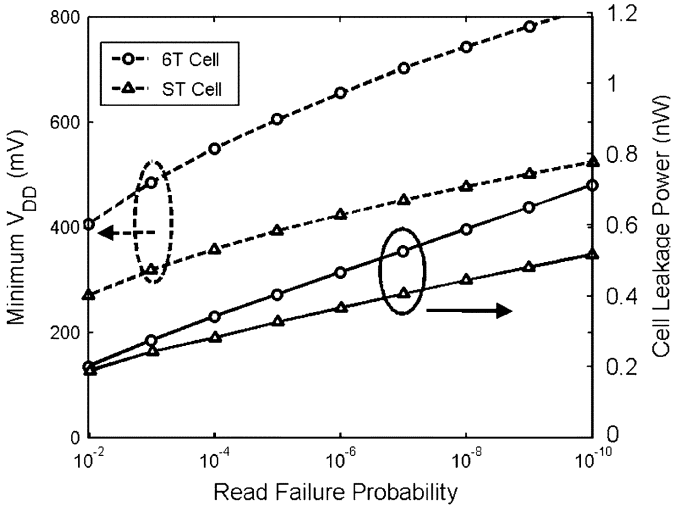

Fig. 10. Leakage power and minimum $V_{\rm DD}$ versus read failure probability.

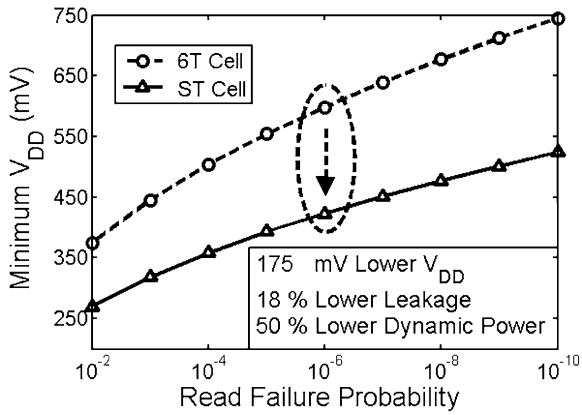

Fig. 11. Iso-area, iso-failure probability comparison.

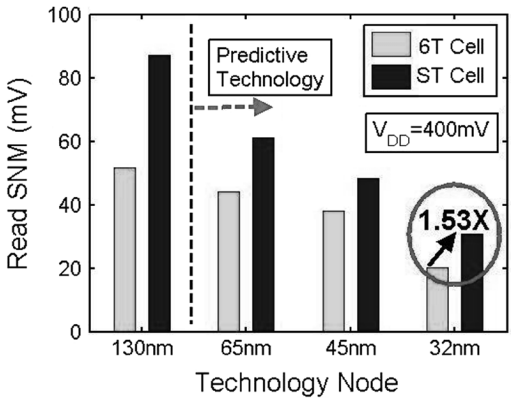

Fig. 12. Read SNM comparison for scaled technologies.

32 nm technology node, the proposed ST bitcell predicts $>2\times$ improvement in the hold SNM at $V_{\rm DD} = 150$ mV compared to the 6T cell [Fig. 13(b)].

Thus, the proposed ST bitcell could be useful for ultralow-voltage data retention in future nanoscaled technologies. The Monte Carlo simulations for the hold SNM are done at 150 mV $V_{\rm DD}$ (25 000 simulations). The hold SNM distribution for various cells is shown in Fig. 14. At 150 mV of $V_{\rm DD}$, the 6T/8T/10T cells no longer exhibit a Gaussian distribution, but a uniform distribution. Also, the hold failure probability is very high with many cells having hold SNM close to zero, indicating possible data flipping. The proposed ST bitcell results in better hold SNM, close to $V_{\rm DD}$/4. The SNM distribution for the proposed ST bitcell is skewed towards the higher values. Due to built-in process variation tolerance (one NMOS (NFL/NFR) opposing another NMOS (NL1/NR1)) the distribution is tight. Also notice that the hold failure probability in the ST bitcell is very low compared with 6T/8T/10T cells.

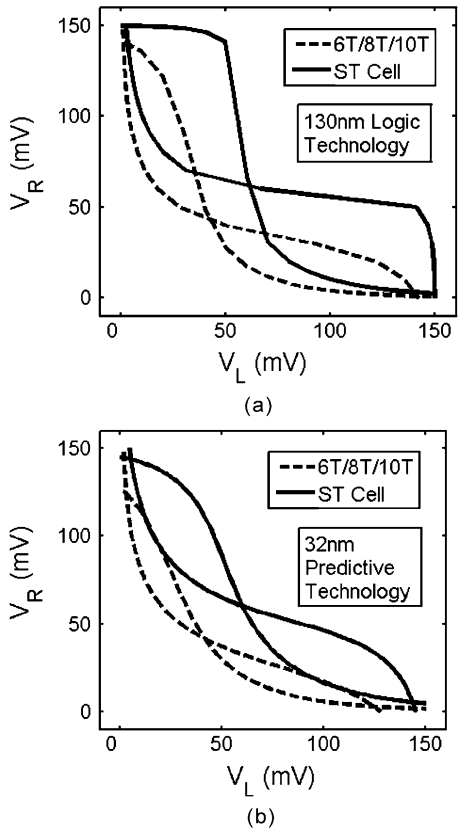

Fig. 13. Hold SNM comparison. $V_{\rm DD} = 150$ mV. (a) 130 nm technology. (b) 32 nm technology.

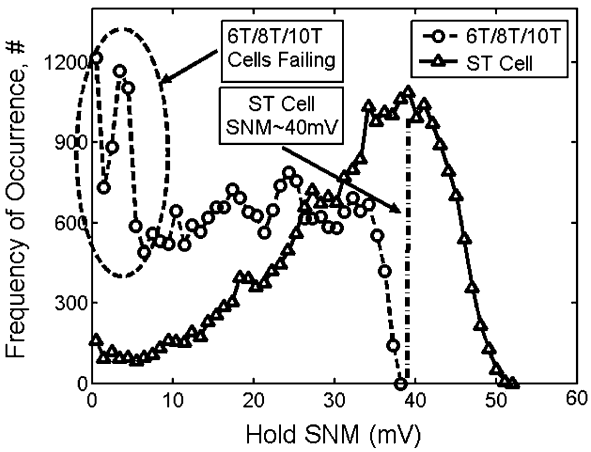

Fig. 14. Hold SNM, Monte Carlo simulation. $V_{\rm DD} = 150$ mV.

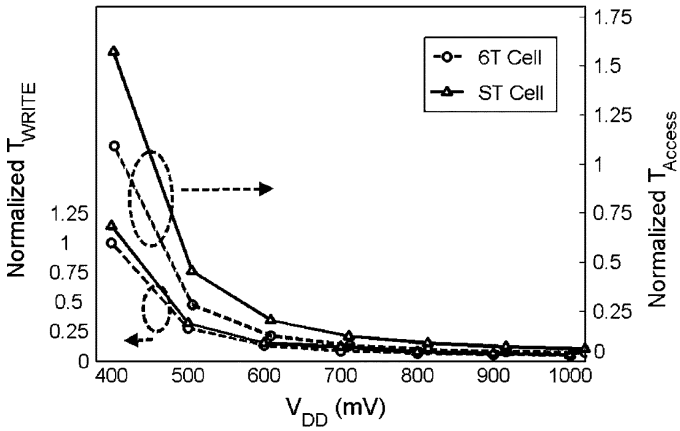

Fig. 15. Write time, access time versus $V_{\rm DD}$. The delay values are normalized to $T_{\rm WRITE}$ value ($V_{\rm DD} = 400$ mV).

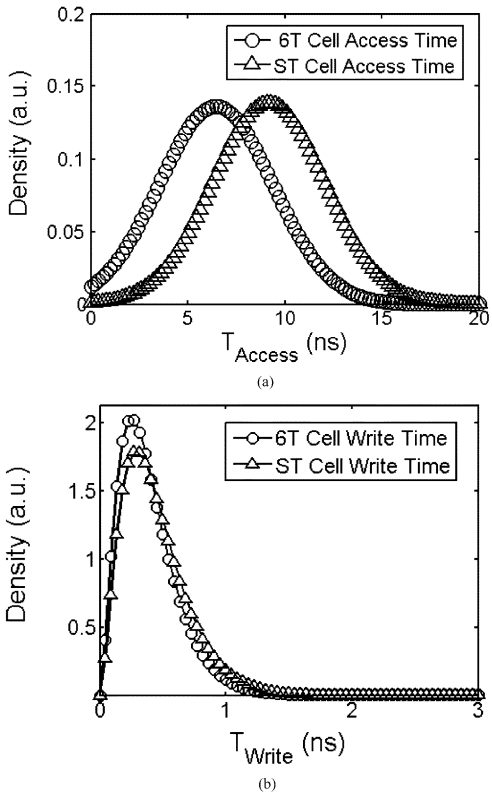

Fig. 16. $T_{\rm ACCESS}/T_{\rm WRITE}$ Monte Carlo simulation ($V_{\rm DD} = 400$ mV). (a) $T_{\rm ACCESS}$ distribution. (b) $T_{\rm WRITE}$ distribution.

This analysis points out the importance of the stability of cross-coupled inverter pair for robust SRAM bitcells operating at ultralow voltages.

G. Access Time/Write Time

Fig. 15 shows the write/access time variations versus $V_{\rm DD}$. Access time $(T_{\rm ACCESS})$ is estimated as the time required for developing 50 mV bitline differential voltage after the wordline is turned ON during a read operation. The ST bitcell incurs 60% longer access time than the 6T cell due to series connected NMOS transistors in the pull-down path ($c_{\rm BL} = 100$ fF, $V_{\rm DD} = 400$ mV). Write time $(T_{\rm WRITE})$ is estimated as the time required to flip the cell contents after the wordline is turned ON, during a write operation. In the write mode, due to increased node capacitance, the ST bitcell exhibits 14% longer write time ($V_{\rm DD} = 400$ mV) than the 6T cell. It is observed that near the subthreshold region, the ST bitcell requires ~ 100 mV higher supply voltage than the 6T cell to produce the same access/write time. For $V_{\rm DD}$ higher than 500 mV, the delay penalty is marginal.

Fig. 16 shows the Monte Carlo simulation results (5000 runs) for access time $(T_{\rm ACCESS})$ and write time $(T_{\rm WRITE})$ ($c_{\rm BL} = 100$ fF, $V_{\rm DD} = 400$ mV). $T_{\rm ACCESS}$ exhibits a Gaussian

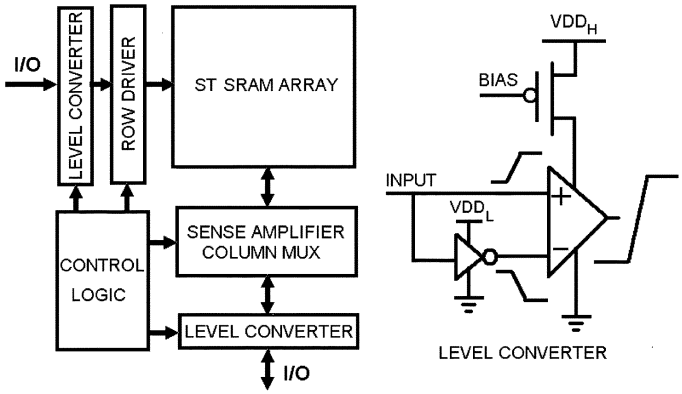

Fig. 17. SRAM architecture, level converter.

distribution while T_{WRITE} shows a non-central F distribution shown in Fig. 16 [4]. For the read case, the ST bitcell shows 42% higher average T_{ACCESS} (due to three series connected NMOS) than the 6T cell. Similarly for the write case, the ST bitcell incurs 14% higher average T_{WRITE} than the 6T cell (due to increased node capacitance).

IV. Measurement Results

A test chip containing 256×16 cells (4 kb) SRAM array has been fabricated using 0.13 μm CMOS technology. Fig. 17 shows the implemented SRAM architecture with the level conversion stage at I/O. A level shifter converts low V_{DD} data (400 mV) to high V_{DD} data (1.2 V) to drive the package capacitance ($\sim$10–20 pF). The I/O buffers operating at lower voltage would require wide transistors to drive such load. The level converter consists of an operational amplifier (opamp) operating in open-loop configuration and is driven by the complementary input signals (Fig. 17). In addition, buffers are implemented to bypass the level conversion stage in order to monitor various internal signals operating at low supply voltages. External control signals are provided to select either the level converter stage or the buffer chain. For SNM measurements, separate isolated 6T/ST memory bitcells with each transistor having 10 fingers are fabricated. The width of each finger is kept the same as the width of a bitcell transistor used in the SRAM array. As threshold voltage (V_{T}) depends on the width of the transistor, the finger structure would generate transistors having same V_{T} as that used in the SRAM array. The transfer characteristics of a memory bitcell depends on "relative sizes" (or relative current driving capabilities) of the transistors. Increasing the number of fingers of all transistors equally would not change the transfer characteristics and hence would not alter SNM values. Guard rings and dummy transistors are used in the finger structure layout in order to minimize the effect of process bias. For isolated cell layout, several dummy NMOS transistors acting as capacitors with source/drain/substrate connected to ground and gate connected to the higher metal layers are used. These dummy NMOS are used for gate oxide protection (Antenna rule). Fig. 18 shows the SRAM layout and the chip micrograph.

Fig. 19 shows the measured butterfly curves ($V_{\mathrm{DD}} = 400$ mV) for the read and hold case. The proposed ST bitcell shows improved inverter characteristics compared to the 6T cell as

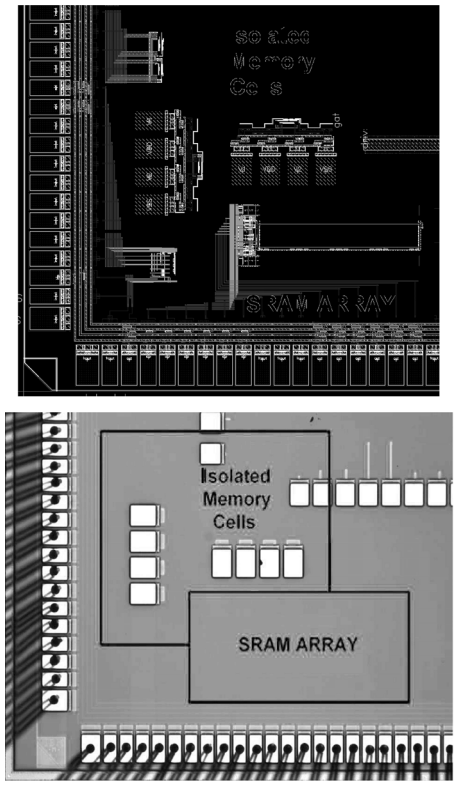

Fig. 18. SRAM layout and chip micrograph.

seen in the hold case. Thus, the proposed ST bitcell consistently gives higher read and hold SNM for different supply voltages, as shown in Fig. 20(a). The measured SNM results match well with the simulation results. The write-trip-point is measured by first writing "1" to a node and then lowering the corresponding bitline voltage from V_{DD} to the point where the contents of the memory cell are flipped (i.e., write-trip-point). The corresponding bitline voltage is normalized to V_{DD}. It is observed that the write-trip-point in the ST bitcell is higher than 6T cell shown in Fig. 20(b). Thus, the proposed ST bitcell clearly demonstrates improved read stability as well as improved write-ability than the 6T cell. Array leakage power and the maximum frequency of operation are measured for various supply voltages. At 400 mV, the SRAM operates at 620 kHz consuming 0.146 μW. This includes the bias current of op-amps used in the level converter. Fig. 21 shows the variation of measured maximum frequency of operation and leakage power for different supply voltages. Maximum frequency and leakage power values are normalized to 400 mV V_{DD} values. Bias voltage for the opamp used in the level conversion stage is adjusted as the supply voltage is changed. Supply voltage is reduced gradually to verify the SRAM array functionality. Various rows in two different test chips are checked for the correct read operation. The proposed ST bitcell array is functional at 160 mV shown in Fig. 22. The data waveforms are captured by enabling the buffer chain in the I/O buffer. The level converter stage is bypassed in this case. The top waveform in Fig. 22 shows the monitored wordline signal and the bottom waveform shows the observed data bits at the output pin. There is a significant delay ($\sim$25 ms) between the wordline signal

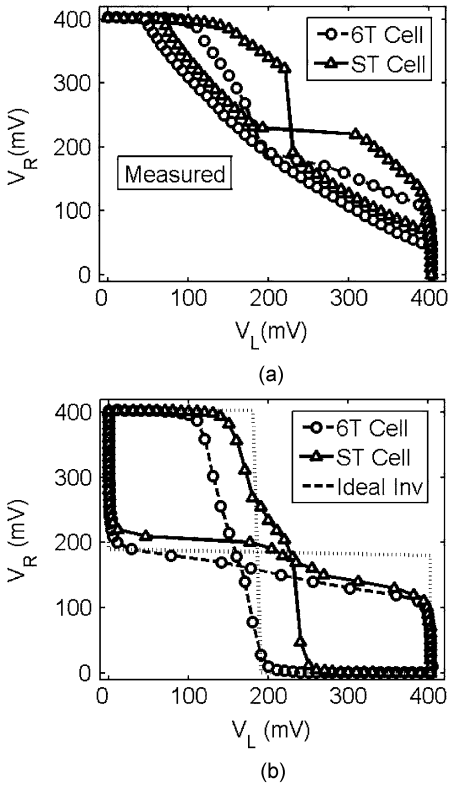

Fig. 19. Read and hold SNM measurement. $V_{\rm DD} = 400$ mV. (a) Read mode. (b) Hold mode.

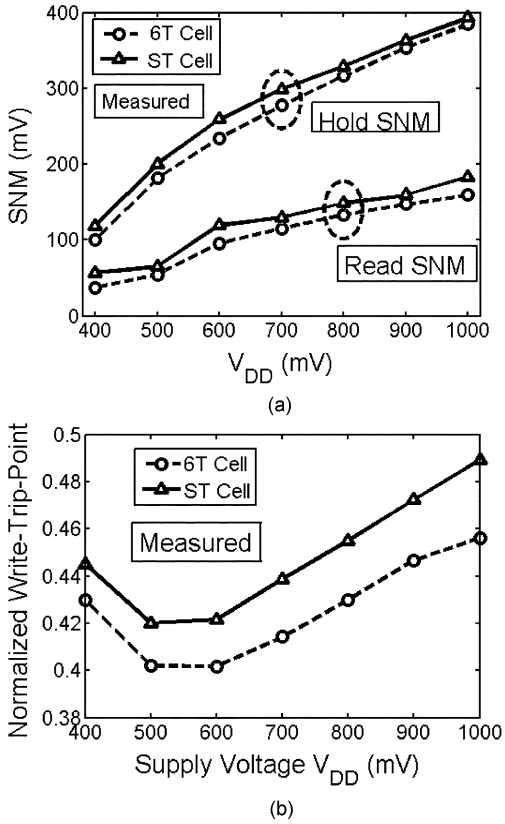

Fig. 20. Measured read, hold SNM and normalized write-trip-point versus $V_{\rm DD}$. (a) Read/hold SNM. (b) Normalized write-trip-point.

and the output data bit signal. We believe that it is due to eight inverter pairs having thick-oxide high $V_{\rm T}$ transistors used in the I/O buffer, package/pin capacitance and the oscilloscope input capacitance (∼20 pF in total).

V. Conclusion

We proposed a Schmitt trigger based differential, robust, 10-transistor SRAM bitcell suitable for subthreshold operation. The proposed ST bitcell achieves higher read SNM (1.56×) compared to the conventional 6T cell ($V_{\rm DD} = 400$ mV). The robust memory cell exhibits built-in process variation tolerance that gives a tight SNM distribution across the process corners. It incorporates differential operation and hence it does not require any architectural changes from the present 6T architecture. At iso-area and iso-read-failure probability, the proposed ST bitcell operates at a lower $V_{\rm DD}$ with lower leakage and reduced read/write power. Simulation results show that the ST bitcell can retain the data at low supply voltage (150 mV). An SRAM array functional at 160 mV supply voltage is demonstrated using 0.13 μm CMOS technology.

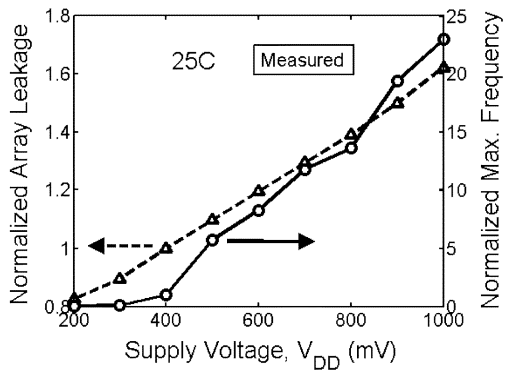

Fig. 21. Measured leakage power and maximum frequency of operation versus $V_{\rm DD}$.

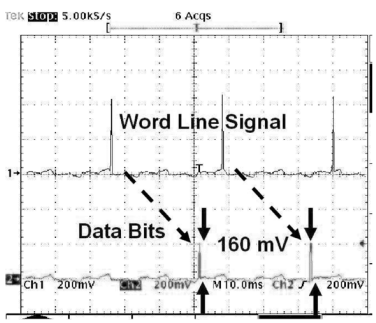

Fig. 22. 160 mV functional SRAM; wordline and data bits waveform. The x-axis (time) unit is in ms, indicating a delay between the internal wordline signal and the output data bits.

Appendix
Schmitt Trigger Operation in Subthreshold Region

To estimate the switching threshold (V_{M+}) during a $0 \rightarrow 1$ input transition, the feedback transistor is assumed to be ON with the gate connected to $V_{\rm DD}$, as shown in Fig. 23. The feedback

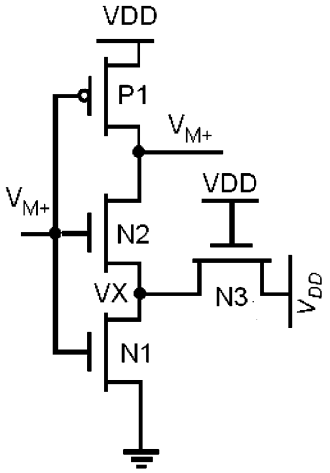

Fig. 23. $0 \rightarrow 1$ input transition equivalent circuit.

transistor N3 increases the intermediate node voltage V_X whenever output is at $V_{\rm DD}$. The drain current in the subthreshold region is given by

$$I = \beta I_o \exp\left(\frac{-V_T}{mkT/q}\right) \cdot \exp\left(\frac{V_{\rm GS}}{mkT/q}\right) \cdot \left(1 - e^{-V_{\rm DS}/(kT/q)}\right)$$
$$V_{\rm T} = V_{\rm TO} - \eta V_{\rm DS} \quad (1)$$

where $\beta =$ transistor W/L ratio, $I_o =$ process-specific current at $V_{\rm GS} = V_{\rm T0}$ for a transistor with W/L $= 1$, T is the temperature in Kelvin, m is the body effect coefficient $= (1 + C_{\rm si}/C_{\rm ox})$, and $\eta =$ drain induced barrier lowering (DIBL) coefficient.

If we define

$$A = \beta I_o \exp\left(\frac{-V_{T0}}{mkT/q}\right)$$

the drain current (I) can be written as

$$I = A \cdot \exp\left(\frac{V_{\rm GS} + \eta V_{\rm DS}}{mkT/q}\right) \cdot \left(1 - e^{-V_{\rm DS}/(kT/q)}\right). \quad (2)$$

Further, for $V_{\rm DS} > 100$ mV $(\sim 4kT/q)$, the term $(1 - e^{-V_{\rm DS}/(kT/q)})$ can be ignored ($< 2\%$ error at 300 K). Thus, the simplified current expression in the subthreshold region as mentioned in (2) becomes

$$I = A \cdot \exp\left(\frac{V_{\rm GS} + \eta V_{\rm DS}}{mkT/q}\right). \quad (3)$$

Using the equivalent circuit shown in Fig. 23, the switching threshold (V_{M+}) during a $0 \rightarrow 1$ input transition is estimated as follows.

At node $V_{\rm OUT}$, $I_{\rm P1} = I_{N2}$

$$A_{P1} \cdot \exp\left(\frac{(V_{\rm DD} - V_{M+}) + \eta_{P1}(V_{\rm DD} - V_{M+})}{m_{P1}kT/q}\right) = A_{N2} \cdot \exp\left(\frac{(V_{M+} - V_X) + \eta_{N2}(V_{M+} - V_X)}{m_{N2}kT/q}\right)$$
$$\therefore \frac{kT}{q} \ln\left(\frac{A_{P1}}{A_{N2}}\right) = \left(\frac{(1+\eta_{N2})(V_{M+} - V_X)}{m_{N2}}\right) - \left(\frac{(1+\eta_{P1})(V_{\rm DD} - V_{M+})}{m_{P1}}\right)$$
$$\therefore V_X = \left(1 + \frac{m_{N2}(1+\eta_{P1})}{m_{P1}(1+\eta_{N2})}\right) V_{M+} - \left(\frac{m_{N2}(1+\eta_{P1})}{m_{P1}(1+\eta_{N2})}\right) V_{\rm DD} - \left(\frac{kT}{q}\right) \cdot \ln\left(\frac{A_{P1}}{A_{N2}}\right) \cdot \left(\frac{m_{N2}}{1+\eta_{N2}}\right). \quad (4)$$

Let

$$\left(\frac{kT}{q}\right) \cdot \ln\left(\frac{A_{P1}}{A_{N2}}\right) \cdot \left(\frac{m_{N2}}{1+\eta_{N2}}\right) = \alpha$$
$$V_X = \left(\frac{1 + m_{N2}(1+\eta_{P1})}{m_{P1}(1+\eta_{N2})}\right) V_{M+} - \left(\frac{m_{N2}(1+\eta_{P1})}{m_{P1}(1+\eta_{N2})}\right) V_{\rm DD} - \alpha. \quad (5)$$

If we assume $m_{P1} = m_{N2}$ and $\eta_{P1} = \eta_{N2}$, then V_X can be written as

$$V_X = 2V_{M+} - V_{\rm DD} - \alpha. \quad (5a)$$

At node V_X, $I_{N2} + I_{N3} = I_{N1}$

$$A_{N2} \cdot \exp\left(\frac{(V_{M+} - V_X) + \eta_{N2}(V_{M+} - V_X)}{m_{N2}kT/q}\right) + A_{N3} \cdot \exp\left(\frac{(V_{\rm DD} - V_X) + \eta_{N3}(V_{\rm DD} - V_X)}{m_{N3}kT/q}\right) = A_{N1} \cdot \exp\left(\frac{V_{M+} + \eta_{N1}V_X}{m_{N1}kT/q}\right) \quad (6)$$

we assume $m_N = m_{N2} = m_{N3} = m_N$ and $\eta_{N1} = \eta_{N2} = \eta_{N3} = \eta_N$. Substituting the value of V_X from (5a)

$$A_{N2} \cdot \exp\left(\frac{(1+\eta_N) \cdot (V_{\rm DD} - V_{M+} + \alpha)}{m_N kT/q}\right) + A_{N3} \cdot \exp\left(\frac{(1+\eta_N) \cdot (2V_{\rm DD} - 2V_{M+} + \alpha)}{m_N kT/q}\right) = A_{N1} \cdot \exp\left(\frac{(1+2\eta_N)V_{M+} - \eta_N (V_{\rm DD} + \alpha)}{m_N kT/q}\right). \quad (7)$$

Equation (7) can be solved numerically to obtain V_{M+}. It can be observed that factors A_{N1}, A_{N2}, A_{N3} depend on NMOS process conditions and fairly track each other across the process corners. For example, at fast NMOS process corner, fast N1 and N3 track fast N2 transistor characteristics. Therefore, Schmitt trigger action does give improved robustness against process variations even in subthreshold regime (Fig. 7). In addition, the switching threshold (V_{M+}) is raised using feedback, as shown in Fig. 7(b).

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