A Read-Disturb-Free, Differential Sensing 1R/1W Port, 8T Bitcell Array

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***Abstract*—We propose a read-disturb-free, 1-read/1-write port, 8-transistor (8T) bitcell utilizing differential sensing. The conflicting design requirement of read versus write operation in a conventional 6T SRAM bitcell is eliminated using separate read/write access transistors. A distributed read-access transistor shared across the bitcells of every row enables read-disturb-free differential sensing operation with eight transistors per bitcell. Write-access transistors are upsized to form a diffusion-notch-free layout which would result in improved manufacturability. 1R/1W port nature of the proposed 8T bitcell makes it an attractive choice for the high speed, dense register file (RF) designs. Bitcell failure measurements on 20 test-chips fabricated in 90-nm CMOS technology demonstrate that the proposed differential 8T bitcell shows 220 mV lower read-$V_{\min}$, 40 mV lower hold-$V_{\min}$, 25 mV higher weak-write voltage compared to the iso-area 6T bitcell at iso-performance. At 600 mV, the proposed 8T bitcell array operates up to 67.2 MHz.**

***Index Terms*—Differential sensing, low voltage static random access memory (SRAM), 1R/1W port SRAM, process tolerance, 8-transistor (8T) bitcell.**

I. Introduction

Static random access memory (SRAM) occupies a significant portion of the total-die area and it is predicted that nearly 90% of the total die area would be occupied by on-chip cache memory in future nano-scale technologies [1]. Conventional 6-transitor (6T) SRAM bitcells utilize minimum sized transistors to achieve high density. Minimum sized devices are prone to significant threshold voltage variations due to random dopant placement and gate edge roughness [1], [2]. Threshold voltage mismatch in SRAM transistors results in asymmetrical bitcell characteristics affecting the bitcell stability [3]. This poses significant challenges in lowering the minimum operating supply voltage (referred as $V_{\min}$) of SRAM caches. With increased process variations and lower $V_{\min}$ constraint, it is becoming extremely difficult to balance the read-stability and the write-ability requirements of a 6-transistor (6T) bitcell by delicate transistor sizing. Various process/circuit assist techniques and bitcell topologies have been explored to lower SRAM $V_{\min}$ [4]. However in this work, we focus on bitcell topology for achieving low voltage operation. We believe that read/write assist techniques can be applied for further $V_{\min}$ reduction.

In order to decouple read and write design requirements, bitcells with varying number of transistors (6T–10T) are also proposed [2]. Key feature of some of these bitcells is to separate read and write operation by employing separate read/write ports. In order to achieve read-disturb free operation, single ended 1R/1W port 8T bitcell has been proposed [5]. The read stability and the write-ability can be optimized independently by optimizing the respective access transistor size. Single ended 1R/1W port 8T bitcell utilizes large signal sensing featuring domino-style hierarchical bitlines. Large signal sensing and hierarchical bitline organization results in poor array efficiency and higher power consumption [4]. Differential dual-ported 8T bitcells use separate read and write access transistors. However read operation in such dual ported bitcell still results in disturbing the bitcell node voltages. In this work, we propose a read-disturb-free, differential sensing 1R/1W port 8T SRAM bitcell incorporating a distributed shared read-access transistor. The rest of the paper is organized as follows. Section II presents the proposed 8T bitcell. Section III compares the proposed 8T bitcell with the conventional 6T and single ended 8T bitcell. Measurement results are presented in Section V. Section VI concludes this paper.

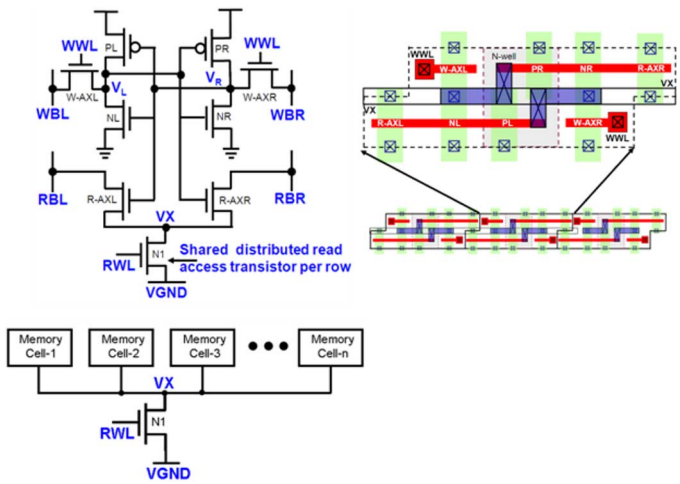

Fig. 1. Proposed read-disturb-free, 1R/1W port, differential sensing 8T bitcell schematics and layout with distributed shared read-access transistor.

II. Proposed 1R/1W 8T Port Differential 8T Bitcell

The proposed 8T bitcell schematic is shown in Fig. 1. Read-disturb-free, 1R/1W port functionality is achieved by adding a differential read port to the conventional 6T SRAM bitcell. The differential sensing with read-disturb-free mechanism requires 10 transistors to form the bitcell [2]. However, the read-access transistors can be shared to form one transistor as reported earlier in the "single-port" 9T bitcell [6]. In the proposed 1R/1W port 8T bitcell, the read-access transistor (shown as N1 in Fig. 1) is shared across the bitcells of each row. Thus, the proposed scheme contains only 8 transistors per bitcell unlike the earlier 9T bitcell in which RWL access transistor is used for every bitcell. Moreover, the proposed 8T bitcell has dual port functionality unlike the single port functionality in earlier reported 9T bitcell [6]. Dual port functionality in the proposed 8T bitcell is useful for register file (RF) designs requiring phase based back-to-back read/write operations.

Read/Write Stability: In the conventional 6T SRAM bitcell access transistor and the pull-down transistor strengths need to be balanced for maintaining the read-stability across wide range of supply and process variations [7]. Addition of separate read port in the proposed 8T bitcell results in read-disturb free operation improving the read-stability. The read-stability in the proposed 8T bitcell is same as the hold-mode stability. Separate write port in the proposed 8T bitcell allows upsizing write-access transistor widths (W-AXL, W-AXR in Fig. 1) compared to the pull-up pMOS thereby improving the writeability.

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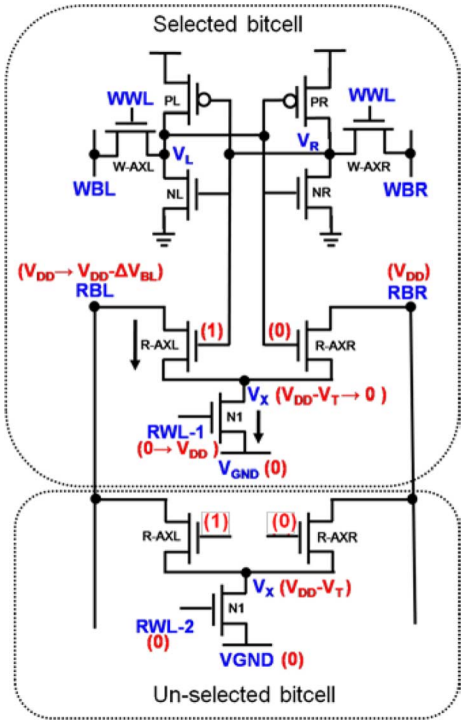


Fig. 2. Shared read access transistor with unselected bitcell on the same column.

Diffusion-Notch Free Layout: In a conventional 6T bitcell, for improving read-stability pull-down nMOS width is generally larger than the access transistor width, forming a diffusion notch. Variations in diffusion notches can impact yield, bitcell size, bit density and array $V_{\min}$ [4]. Uniform diffusion tracks give better manufacturability—a must for future nano-scale technologies.Upsizing write-access transistors result in diffusion-notch free layout in the proposed 8T bitcell. Fig. 1 shows the diffusion-notch-free thin cell layout for the proposed 8T bitcell along with the adjacent bitcells. Each of the proposed 8T bitcells requires six diffusion tracks with one of the diffusion tracks is shared with the adjacent bitcell. Thus, the proposed 8T bitcell on an average requires five diffusion tracks (conventional 6T thin-cell layout requires four diffusion tracks). Fig. 1 shows only diffusion-to-M1 contacts. Read bitlines would use separate M2 lines. Shared read access transistor is distributed after every 16 bitcells. Extra diffusion track and the distributed read access transistor increases the proposed 8T bitcell area by 28% (including shared read-access transistor) compared to the minimum sized 6T bitcell. Sharing the read access transistor (N1) along a row results in low area overhead compared to the earlier 9T bitcell.

Charge Sharing: Since the read-access transistor (N1) is placed in the bottom of the read port (see Fig. 2), the intermediate node V_X of every bitcell is weakly connected to the read bitline (RBL), as one of read port devices (R-AXL or R-AXL) will be ON depending on the bitcell data (see Fig. 2). Hence the charge sharing issue between RBL and the V_X node of the unselected cells on the same column needs to be considered. During the precharge phase, V_X node of every bitcell is precharged to $V_{CC} - V_T$. When a particular RWL is asserted, one of the RBL would start discharging (see Fig. 2). Charge sharing between RBL and V_X nodes would occur if RBL discharges below $V_{CC} - V_T$. For small signal sensing with bitline differential (ΔV_{BL}) requirement $\sim$ 50–100 mV, RBL will not drop below $V_{CC} - V_T$. Hence charge sharing due to V_X node of unselected cells would not affect the bitline differential/read delay.

TABLE I
DEVICE SIZE FOR BITCELL FAILURE PROBABILITY ESTIMATION

	PU	PD	W-AX	R-AX
6T Mincell	100nm	200nm	100nm	---
6T Iso-area bitcell	100nm	600nm	100nm	---
Single Ended 8T bitcell	100nm	200nm	200nm	300nm
Proposed Diff. 8T bitcell	100nm	200nm	200nm	100nm

Half-Select Stability: The proposed 8T bitcell incorporates upsized write- access transistors to improve the writeability. Hence the bitcells on unselected column will experience read-disturbs. Although it is possible to optimize the bitcell to achieve read-stability under such half-select conditions, the read-stability advantage due to separate read-port would be lost [5]. Hence, to avoid the half-select condition, the proposed 1R/1W port 8T bitcell array should be floor-planned such that all bits in the same word are spatially adjacent as suggested in [5].

Access-Time Overhead: The shared read-access transistor in the proposed 8T bitcell can reduce the read current due to additional capacitance at the shared intermediate node (V_X). However, this access-time overhead can be mitigated by upsizing the read-access transistor (N1) or using a small charge-pump for every row to boost RWL voltage as reported in [2].

Leakage Reduction With VGND: As read access transistor (N1) in the proposed 8T bitcell is shared across the bitcells of the same row, the read bitline leakage (during the standby mode) can be reduced by raising the source voltage (VGND node in Fig. 1). By raising VGND potential, the leakage current through the read access transistor (N1) is reduced due to increased threshold voltage (body effect) as well as negative gate-source voltage. Note that VGND node is different than VSS node of the cross coupled inverter pair (source of NL and NR in Fig. 1) and hence altering VGND voltage will not affect the hold mode stability of the bitcell.

III. COMPARISON WITH 6T AND SINGLE ENDED 8T BITCELL

In this section, we present the comparison between the 6T mincell, 6T iso-area bitcell, single ended 8T bitcell, and the proposed differential 8T bitcell. Monte Carlo simulations are performed using 65 nm industrial CMOS process technology models across all process corners (temperature = 300 K). Failure probability is estimated assuming Gaussian V_T distribution [2]. Minimum geometry 6T bitcell (referred as 6T mincell) device widths are 100/100/200 nm for pull-up/access/pull-down transistors, respectively. For improving the read-stability in iso-area 6T bitcell, pull-down device is increased by 3X following the layout design rules as reported in [8]. For single ended and the proposed 8T bitcell write-access transistors are upsized to 200 nm to form diffusion-notch free layout. Table I lists the detailed device sizing employed to compare the bitcell topologies. Note that, for iso-area analysis, we use iso-channel-length for all transistors. Although channel length can be adjusted separately for each device, setting SRAM transistor channel lengths to any arbitrary value may not be feasible in nano-scale technologies due to limitations in the lithography process.

Read static noise margin (R-SNM) is used to quantify the read-stability of the SRAM bitcells. As shown in inset (Fig. 3), read-failure probability (P_{read}) is estimated as

$$P_{\text{read}} = \text{Prob.}(\text{R}-\text{SNM} < V_{\text{thermal}}).$$

If R-SNM is lower than the thermal voltage, then it is treated as a read-failure. Note that any other suitable threshold criterion can be

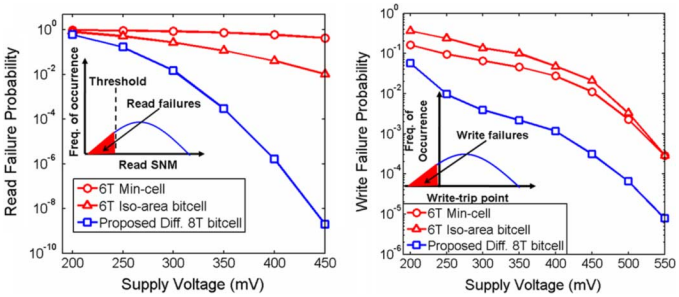


Fig. 3. Read and hold-failure probability comparison: 6T bitcell versus proposed 8T bitcell.

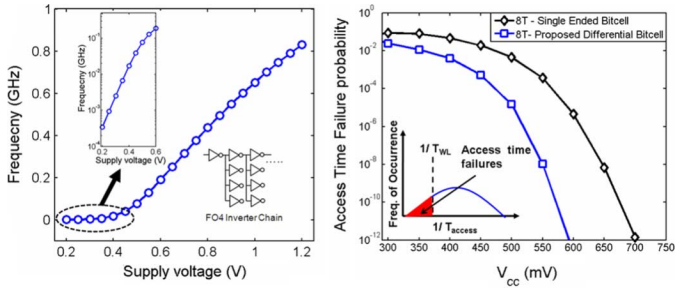


Fig. 4. Access-time failure probability comparison: single ended 8T versus proposed differential 8T bitcell.

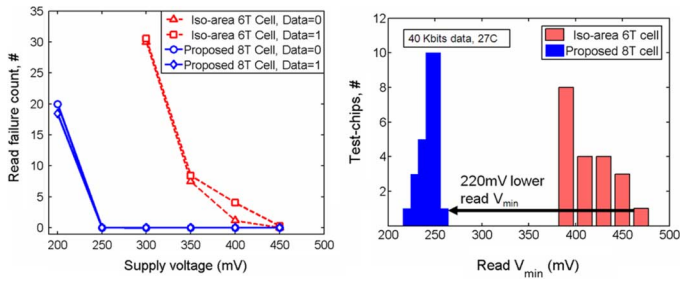


Fig. 5. Measured read-failures (average of 20 test-chips) and measured read-$V_{\min}$ distribution.

used. Read-disturb free operation in the proposed 8T bitcell significantly gives lower read failure probability compared to the iso-area 6T bitcell (see Fig. 3). Similar to the read stability case, hold-failure probability (P_{hold}) is estimated by computing the hold-SNM.

$$P_{\text{hold}} = \text{Prob.}\,(\text{hold SNM} < V_{\text{thermal}}).$$

As P/N ratio of the cross coupled inverter pair is higher in the proposed 8T bitcell compared to the iso-area 6T bitcell, it results in symmetrical inverter characteristics and hence lower hold-failure probability. 6T mincell and the proposed 8T bitcell has same P/N ratio for the cross coupled inverter pair resulting in similar hold-failure characteristics. However, hold-failure probabilities are marginally different due to leakage currents through differently sized access transistors. Single ended 8T bitcell also employ read-disturb-free operation. Hence read/hold-stability in both 8T bitcells is same as the hold-mode stability.

Write-ability of a bitcell gives an indication of how easy or difficult it is to write to the cell. Write-trip-point is defined as the bitline voltage needed to flip the cell content [9]. As shown in inset (Fig. 3), write-failure probability (P_{write}) is calculated as

$$P_{\text{write}} = \text{Prob.}\,(\text{write}-\text{trip}-\text{point} < 0\ \text{mV}).$$

Due to upsized write-access transistors, the proposed 8T bitcell gives lower write-failure probability compared to the 6T mincell as well as iso-area 6T bitcell (see Fig. 4). For the single ended 8T bitcell, write-access device is upsized to achieve diffusion-notch-free layout. Hence both 8T bitcells would show similar write-failure characteristics.

For access-time failures, it is shown that instead of T_{access}; the inverse of T_{access} gives normal distribution [10]. Hence, access-time failure probability ($P_{\text{access\_time}}$) is calculated as

$$P_{\text{access time}} = \text{Prob.}\,(1/\text{T}_{\text{access}} < 1/T_{\text{WL}}).$$

For the differential sensing, access-time (T_{access}) is estimated as the time required to produce a prespecified bitline differential ($\Delta V_{\text{BL}} = 50$ mV) for correct sense amplifier operation. As bitline differential depends on the word-line pulse-width, it is necessary to obtain voltage-frequency characteristics across different voltages. Fig. 4 shows the variation of clock frequency with the supply voltage. In this case, the delay of 20 minimum sized FO4 (Fan out of 4) inverters is assumed to be one clock period. SRAM array cycle time is one clock period in which word-line is activated in the first phase and sense amplifier is activated in the next phase. For the proposed differential 8T bitcell, 128 bitcells/column is used to estimate the access-time. Delay from WL turn-ON to 50 mV bitline differential is termed as the access-time. The read-port transistor and the shared read-access transistor width in the proposed 8T bitcell are sized to yield the same read-current as that of the iso-area 6T bitcell. Hence the proposed 8T bitcell would show similar access-time characteristics compared to the 6T bitcell. For the single-ended 8T bitcells case, 128 bits are organized as 8 local-bitline (LBL) stages (with 16 bits/LBL) driving the global-bitline (GBL) stage. Delay from read WL turn-ON to GBL evaluation is termed as the access-time. It is found that, differential sensing 8T bitcell shows improved access-time characteristics compared to the single ended sensing 8T (see Fig. 4).

IV. Measurement Results

A test-chip containing 2 kb iso-area 6T bitcell and the proposed 8T bitcell arrays was fabricated using 90-nm CMOS technology. SRAM array was organized as 256 rows × 8 columns. To achieve robust design margins at low voltage fully synchronous design style was adopted. Built-in test circuit to measure the failure count was also implemented [11]. Fig. 5 shows the measured single bit read-failures for data $= 0$ and data $= 1$ for the proposed differential 8T bitcell and iso-area 6T bitcell averaged over 20 test-chip measurements. For the 6T iso-area bitcell, hold-failures were observed below 300 mV. Hence to distinguish read-failures from the hold-failures, read-failure measurements in the 6T bitcell were performed only up to 300 mV. Due to read-disturb free operation, the proposed 8T bitcell shows significantly reduced read-failures. In the proposed 8T bitcell, as read-stability and hold-stability are same, the read-failures below 250 mV are essentially hold-failures. Read-$V_{\min}$ was determined when the first read-failure was observed. The proposed 8T bitcell showed 220 mV lower read $V_{\min}$ compared to the iso-area 6T bitcell (40 kb data, room temperature). Also, the spread in read-$V_{\min}$ distribution was reduced for the proposed 8T bitcell.

Hold-failures were measured by following a similar procedure as the read-failure measurements. Fig. 6 shows measured hold-failures averaged over 20 test-chips (40 kb, Data$= 0$ and Data $= 1$) at room temperature for the proposed 8T bitcell and the iso-area 6T bitcell. In order to achieve improved read-stability for iso-area 6T bitcell, pull-down transistors are upsized. This lowers the switching threshold of the cross coupled inverters resulting in increased hold-failures in the iso-area 6T bitcell. On the other hand, the proposed 8T bitcell has higher P/N ratio, resulting symmetrical inverter characteristics reducing the hold-failures. Hold-$V_{\min}$ was estimated as the highest supply voltage where first hold-failure was observed (see Fig. 6). The proposed 8T bitcell

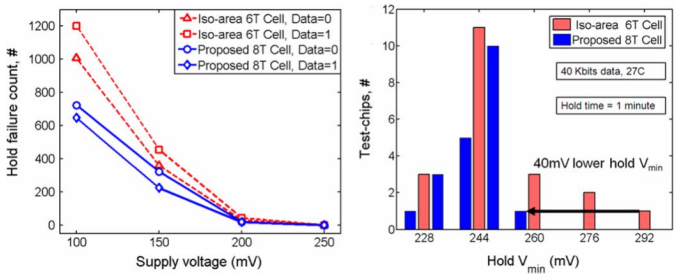


Fig. 6. Measured hold-failures (average of 20 test-chips and measured hold-$V_{\min}$ distribution.

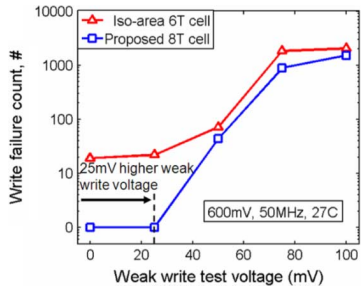


Fig. 7. Measured write-failures versus weak write test voltage.

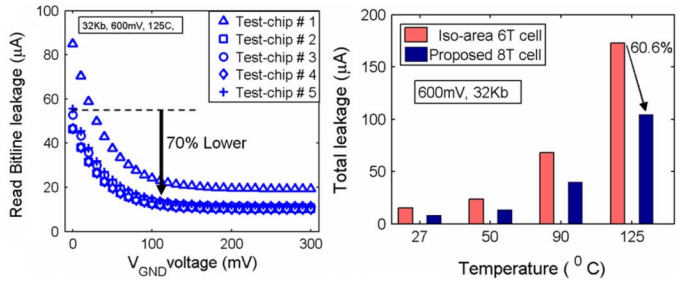


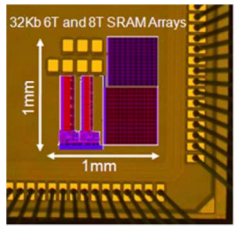
Fig. 8. Measured read bitline leakage current and total leakage current (average of five test-chips).

showed 40 mV lower hold-$V_{\min}$ as well as lower spread in hold-$V_{\min}$ compared to the iso-area 6T bitcell (40 kb data).

Write-failures were measured following weak-write-test methodology [9]. The write-trip-point of the bitcell was estimated as the maximum bitline voltage necessary to flip the bitcell data. Higher write-trip-point indicates better writeability. Fig. 7 shows measured room temperature write-failures at 600 mV/50 MHz. The 6T iso-area bitcell showed finite number of write-failures even with weak-write voltage of "0." On the other hand, the proposed 8T bitcell could tolerate 25 mV higher weak-write voltage before first write-failure occurred. Larger write-access transistor size in the proposed 8T bitcell resulted in improved write-ability compared to the corresponding iso-area 6T bitcell.

Access-time failure measurements were performed at higher supply voltage (600 mV) in order to distinguish it from read-failure measurements. Operating frequency was increased gradually (up to maximum logic analyzer frequency of 67.2 MHz) and access-time failures were observed. Since the read port transistors in the proposed 8T bitcell have same size as that of the iso-area 6T bitcell, both bitcells showed similar access-time failures.

The leakage current was measured by a direct probe measurement from 32 kb iso-area 6T bitcell and the proposed 8T bitcell arrays. VGND node voltage was controlled with an external supply. It was observed that raising the VGND node voltage to 100 mV reduces read bitline current in the proposed 8T bitcell by 70% (average of five test-chips, Fig. 8). Further, the proposed 8T bitcell showed 60% lower total-leakage compared to iso-area 6T counterpart (at 600 mV, 125C). Higher leakage current in the iso-area 6T bitcell is due to upsized pull-down transistors (NL, NR). Fig. 9 shows the 90 nm test-chip die photo and the chip measurement summary. The test-chip contained nearly 600 K transistors and occupied 1 mm^2 die area.



Technology	90nm, 8-metal, CMOS
Transistor count	600 K
Die area	1 mm X 1mm
Measured Read V_{min}	480 mV (6T iso-area) / 260mV (8T)
Measured Hold V_{min}	300 mV (6T iso-area) / 260mV (8T)
Maximum Frequency	67.2MHz (6T/8T, V_{DD} = 600mV, 25C)
Measured Leakage Current	182μA (6T iso-area)/ 114μA (8T) (32Kb, 600mV, 125C)

Fig. 9. Annotated die photograph and chip measurement summary.

V. Conclusion

Read-disturb-free, differential sensing, 1R/1W port, 8T bitcell is proposed. The conflicting design requirement of read versus write operation in a conventional 6T SRAM bitcell is eliminated using separate read/write access transistors. A distributed read-access transistor shared across the bitcells of every row enables read-disturb-free differential sensing operation while consuming 8 transistors per bitcell. Due to its read-disturb-free and dual port functionality it can also be used in Register File designs requiring phase based back-to-back read/write operations. Measurement results on a 90-nm CMOS test-chip with the proposed 8T bitcell demonstrated lower read/hold $V_{\min}$, better writeability and lower leakage compared to the iso-area 6T bitcell at iso-performance.

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