Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design

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***Abstract*—We analyze Schmitt-Trigger (ST)-based differential-sensing static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. The proposed ST bitcells incorporate a built-in feedback mechanism, achieving process variation tolerance—a must for future nano-scaled technology nodes. A detailed comparison of different bitcells under iso-area condition shows that the ST-2 bitcell can operate at lower supply voltages. Measurement results on ten test-chips fabricated in 130-nm CMOS technology show that the proposed ST-2 bitcell gives 1.6× higher read static noise margin, 2 × higher write-trip-point and 120-mV lower read-V_{min} compared to the iso-area 6T bitcell.**

***Index Terms*—Low-voltage SRAM, process tolerance, Schmitt-Trigger (ST), V_{min}.**

I. Introduction

PORTABLE electronic devices have extremely low power requirement to maximize the battery lifetime. Various device-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write-failure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2].

In a given process technology, the maximum supply voltage (referred to as V_{max}) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits. V_{max} is reducing with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as V_{min}), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, V_{min} is increasing, and this closes the gap between V_{max} and V_{min} [5]. Hence, to enable SRAM bitcell operation across a wide voltage range, V_{min} has to be further lowered. Various design solutions such as read-write assist techniques and bitcell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bitlines, bitcell VSS node, and bitcell VCC node) [5]. In this case, SRAM V_{min} can be lowered without adding extra transistors to the six–transistor (6T) bitcell. Various bitcell topologies are also proposed to enable low-voltage operation. In this work, we focus only on various bitcell configurations. We believe that read-write assist circuits can be applied to these bitcell configurations for further V_{min} reduction.

The remainder of this paper is organized as follows. Section II describes various previously published SRAM bitcells. Section III briefly presents the Schmitt-Trigger (ST)-based SRAM bitcells. Section IV shows the detailed V_{min} comparison of various bitcell topologies. Section V presents the measurement results. Section VI summarizes the low-voltage SRAM design discussion.

II. Previous SRAM Bitcell Research

Several SRAM bitcells have been proposed having different design goals such as bit density, bitcell area, low voltage operation and architectural timing specifications. Fig. 1 lists the SRAM bitcells having four to ten transistors [6]–[27]. In the four–transistor (4T) loadless bitcell, pMOS devices act as access transistors [6]. The design requirement is such that pMOS OFF-state current should be more than the pull-down nMOS transistor leakage current for maintaining data "1" reliably. With increasing process variations and exponential dependence of the subthreshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging.

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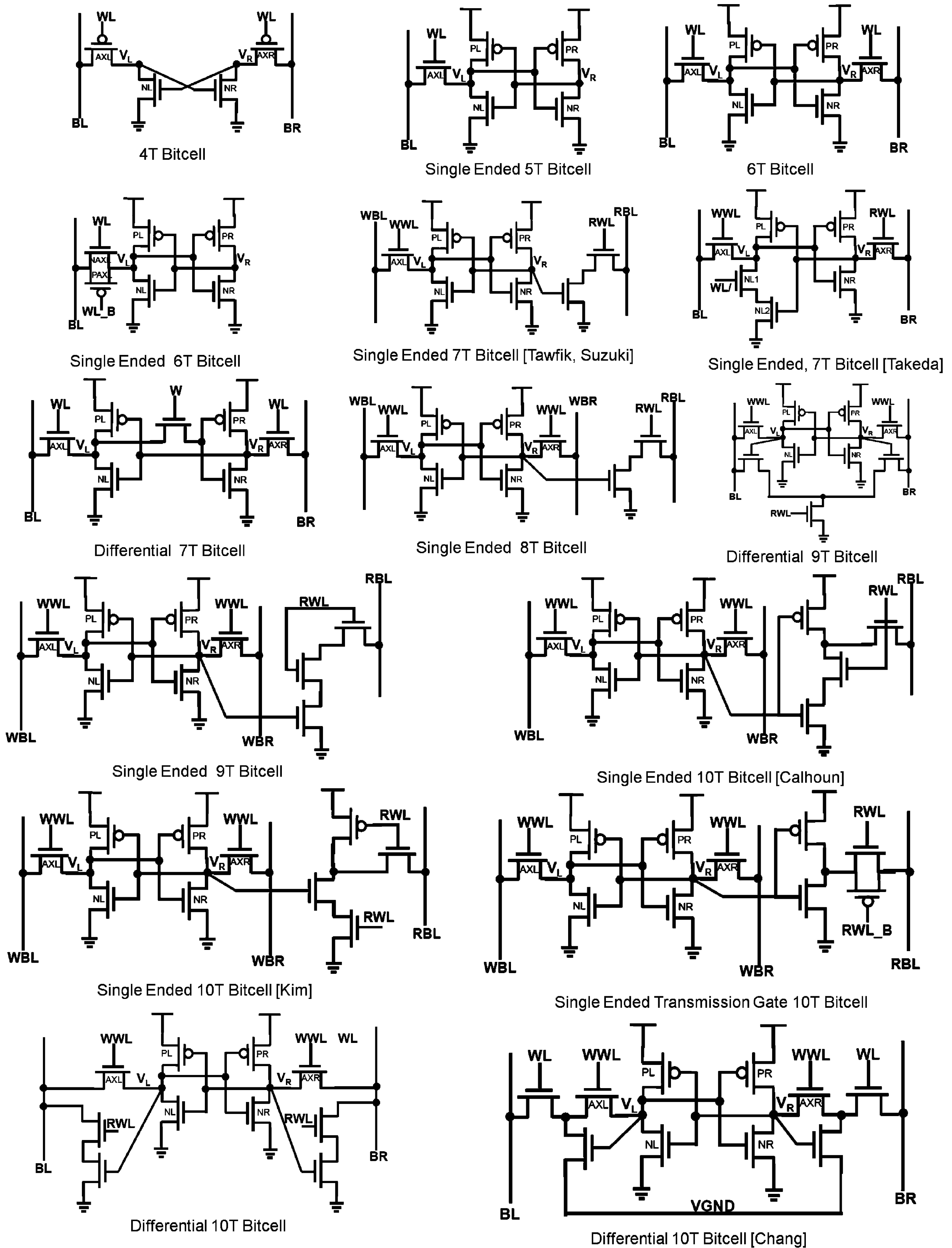


Fig. 1. Published SRAM bitcell configurations [6]–[24].

5T bitcell consists of asymmetric cross coupled inverters with a single bitline [7]. Separate bitline precharge voltages are used for read and write operations. The intermediate read bitline precharge voltage requires a dc–dc converter. Tracking the read precharge voltage across PVT corners would require additional design margins in bitcell sizing and may limit its ap-

plicability. A 6T bitcell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two nMOS access transistors. The 6T bitcell is the "*de facto*" memory bitcell used in the present SRAM designs. A single-ended 6T bitcell uses a full transmission gate at one side [8]. Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters. The single-ended 7T bitcell proposed separately by Tawfik *et al.* and Suzuki consists of single-ended write operation and a separate read port [9], [10]. Single-ended write operation in this 7T bitcell needs either asymmetrical inverter characteristics or differential VSS/VCC bias. Takeda *et al.* have proposed another single-ended 7T bitcell in which an extra transistor is added in the pull-down path of one of the inverters [11]. During read mode, the extra transistor is turned OFF, isolating the corresponding storage node from VSS. This results in read-disturb-free operation. In a differential 7T bitcell, the feedback between the two inverters is cut off during the write operation [12]. Successful write operation necessitates skewed inverter sizing, resulting in asymmetrical noise margins. In a single-ended 8T bitcell, extra transistors are added to the conventional 6T bitcell to separate read and write operation [13]–[17]. Liu and Kursun have proposed a 9T bitcell with differential read-disturb-free operation [18]. In a single-ended 9T bitcell, separate read port is used to decouple read and write operation which is similar to the single-ended 8T bitcell. Stacked read access transistors are used to reduce the bitline leakage [19], [20]. Recently, differential 8T bitcells utilizing RWL/WWL cross-point array and data-dependent VCC have also been reported [21], [22]. Single-ended 10T bitcells are similar to the single-ended 8T bitcell except for the read port configurations. Additional transistors are used to control the read bitline leakage [23], [24]. Noguchi *et al.* have proposed a single-ended transmission-gate 10T bitcell [25]. The bitcell contents are buffered using an inverter and then transferred to the read bitline whenever the bitcell is accessed. Use of the transmission gate eliminates domino-style read-bitline sensing. Thus, read bitline does not require precharge and keeper transistor. Also, if the the accessed data are unchanged, read-bitline toggling is avoided. A differential 10T bitcell with two separate ports for read-disturb- free operation has also been reported [25]. Chang *et al.* have proposed a read-disturb-free differential 10T bitcell which is suitable for bit-interleaved architecture [26]. A similar 10T cell with column-assist technique is also reported. [27]. However, series-connected write access transistors degrade the write-ability of the bitcell and needs write-assist circuits such as word-line boosting for a successful write operation.

In all of the previously reported bitcells, the basic element for the data storage is a cross-coupled inverter pair. Extra transistors are added to decouple the read and write operations. None of the previously reported bitcells incorporate process variation tolerance for improving the stability of the cross coupled inverter pair of an SRAM bitcell operating at ultralow supply voltage. For successful SRAM operation under PVT variations, the stability of the cross-coupled inverter is important. Traditionally, device sizing has been adopted to mitigate the effect of process variations. However, device sizing is not effective in improving the bitcell stability at very low supply voltage [28].

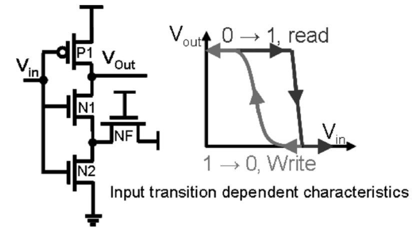


Fig. 2. Conceptual ST schematics: the gate connection of the feedback transistor is connected to the VCC to show the feedback mechanism during $0 \rightarrow 1$ input transition.

Hence, we need a different design approach for successful low voltage SRAM design in nanoscaled technologies. In this work we propose Schmitt Trigger based SRAM bitcell having built-in feedback mechanism that exhibits the process variation tolerance. This robust process tolerance can be an essential attribute for SRAM scaling into future nanoscaled technology nodes.

III. Schmitt Trigger (ST) SRAM Bitcells

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition [29]. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in Fig. 2. During $0 \rightarrow 1$ input transition, the feedback transistor (NF) tries to preserve the logic "1" at output (V_{out}) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a $0 \rightarrow 1$ input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

For the $1 \rightarrow 0$ input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. Two novel bitcell designs are proposed. The first ST-based SRAM bitcell has been presented in our earlier work [30]. Another ST-based SRAM bitcell which further improves the bitcell stability has been reported in [31]. To maintain the clarity of the discussion, the ST bitcell in [30] is termed the "ST-1" bitcell while the other ST bitcell in [31] is termed the "ST-2" bitcell.

A. *ST-1 Bitcell*

Fig. 3 shows the schematics of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-line (WL), and two bitlines (BL/BR). Transistors PL-NL1-NL2-NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the $0 \rightarrow 1$ input transition giving the ST action. Detailed operation of the ST-1 bitcell can be found in [30].

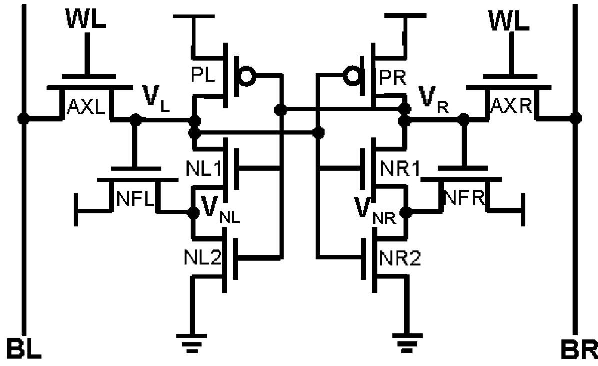
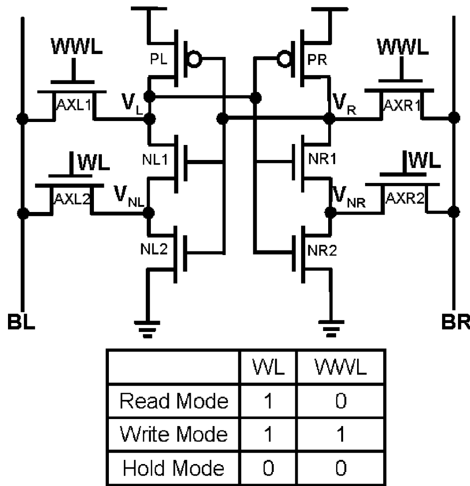


Fig. 3. ST-1 bitcell schematics.



	WL	WWL
Read Mode	1	0
Write Mode	1	1
Hold Mode	0	0

Fig. 4. ST-2 bitcell schematics.

B. ST-2 Bitcell

Fig. 4 shows the schematics of the ST-2 bitcell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bitlines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bitcell, feedback is provided by separate control signal (WL) unlike the ST-1 bitcell, where in feedback is provided by the internal nodes. In the ST-1 bitcell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Detailed operation of the ST-2 bitcell is explained in our earlier work [31].

IV. SRAM Bitcell $V_{\min}$ Analysis

A. Iso-Area Bitcells

The ST bitcells consumes approximately $2\times$ area compared with the 6T mincell [30], [31]. Hence, in order to estimate the minimum supply voltage $V_{\min}$, it is only fair to compare the bitcells under iso-area condition. Fig. 5 shows the thin-cell illustrative layout of the 6T mincell and the proposed ST-2 bitcell. In a thin-cell layout approach, the vertical dimension is determined by the poly pitch while lateral dimension is determined by the device sizing. In general, the SRAM bitcell area is dominated by the contact and the diffusion spacing. Careful examination of various industrial minimum–sized 6T bitcell layouts reveal that only 30%–35% of the lateral dimension contributes to the device widths while remaining lateral dimension is used for the contact and diffusion spacing [32], [33]. Note that, the channel lengths of SRAM transistors may not be set to arbitrary value in a scaled process due to lithography limitations. Increasing the channel length increases bitcell area along the bitline direction. This would increase the bitline capacitance and hence the bitline power consumption. Since bitline power is the dominant component of the overall power consumption, the vertical dimension along the bitline is unchanged (= 2 poly-pitch) for the bitcell upsizing. Any upsizing is realized in the lateral direction by increasing the device widths along the word-line. This would increase word-line capacitance and hence word-line switching power. However, only one word-line in the subarray is active during a read/write operation. Hence, this approach of bitcell upsizing would result in minimal increase in power dissipation. Monte Carlo simulations are performed using 65-nm industrial process technology models which include systematic as well as random process variations. Bitcell failure probability is estimated assuming Gaussian distribution of the threshold voltage [3].

1) 6T Iso-Area Bitcell: In this work, we use 6T mincell device widths of 100, 100, and 200 nm for pull-up/access/pull-down transistors, respectively. We can upsize the 6T mincell in various ways. If the bitcell is upsized to be more read-stable, it would affect its write-ability and *vice versa*. Hence, all transistors in the 6T mincell are upsized uniformly to improve the read-stability and write-ability simultaneously. As seen in Fig. 5, increasing device widths linearly increases the bitcell area sublinearly. For $2\times$ larger area, the 6T mincell device widths need to be upsized by $4\times$. The bitcell area is estimated following the layout rules in [33].

2) 8T Iso-Area Bitcell: Fig. 6 shows the single-ended sensing 8T bitcell organization [34]. Local bitline (LBL) containing 8/16/32 bitcells is evaluated using the read-merge logic (NAND gate in Fig. 6). A second stage of Global bitline (GBL) combines multiple LBL stages. For the LBL stage, to maintain the dynamic node voltage, a weak pMOS device called a keeper is used. The keeper device supplies the leakage current of the pull-down path. As keeper device opposes discharging of the LBL node, a tradeoff exists between the LBL evaluation delay and the noise immunity. Due to large signal sensing and delay/noise tradeoff at the local bitline node, hierarchical bitline sensing is used. Thus, due to segmented bitline and the associated read-merge logic, single-ended 8T bitcell array efficiency is 30–50% [5], [35]. On the other hand, present 6T bitcell designs utilize differential sensing mechanism resulting in 65%–75% array efficiency [36]–[39]. Due to a difference in the array efficiency, the 8T iso-area bitcell $V_{\min}$ should be evaluated at iso-subarray area condition. Table I shows the split-up of the total subarray area containing 6T/8T/ST bitcells. Bitcell areas are normalized to 6T mincell area.

8T (ST) bitcell area is 30% (100%) larger than the 6T mincell [13]–[17], [30], [31]. The array efficiency for single-ended

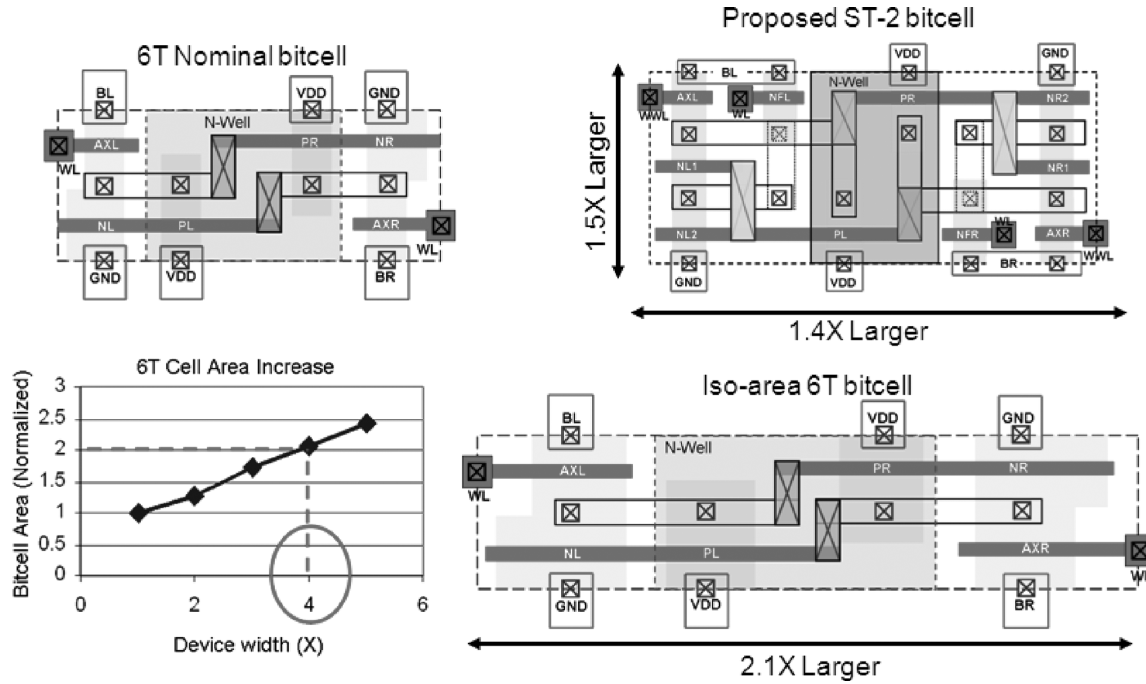


Fig. 5. 6T bitcell upsizing approach: area versus device widths.

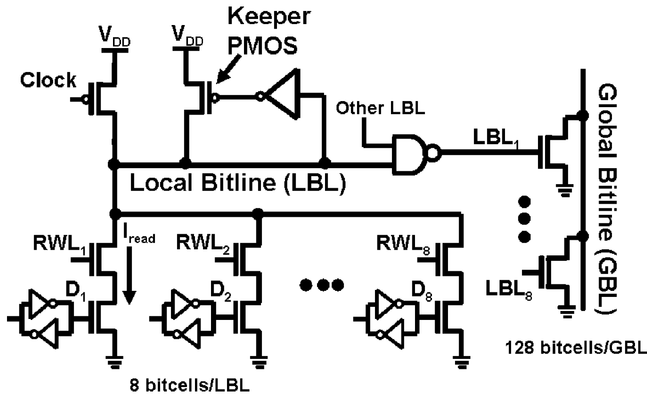


Fig. 6. 8T SRAM: hierarchical bitline sensing mechanism.

TABLE I
SUBARRAY AREA ANALYSIS OF 6T/8T/ST BITCELL

	6T mincell	8T bitcell	ST bitcells
Bitcell area	1X	1.3X	2X
No. of bitcells	N	N	N
Total bitcell area	NX	1.3NX	2NX
Array efficiency	70%	50%	70%
Peripheral circuits area	0.43NX	1.3NX	0.86NX
Total Sub-array area	1.43NX	2.6NX	2.86NX

and the differential sensing is assumed to be 50% and 70% respectively. As shown in Table I, for iso-area condition 8T bitcell can be upsized by $(2.86\mathrm{Nx} - 1.3\mathrm{Nx})/\mathrm{Nx} = 1.56$. As 8T bitcell has read-disturb-free operation, any additional area increase can be used for upsizing the write access transistors to improve the write-$\mathrm{V_{min}}$. Therefore, for iso-area 8T bitcell, the write-access transistors are upsized by 3 × compared to the 6T mincell case (Fig. 7).

3) 10T Iso-Area Bitcell: A 10T bitcell with additional read ports sutilize differential sensing without disturbing the bitcell nodes during a read operation [25]. The 10T bitcell proposed by Chang *et al.* is another differential sensing bitcell without any read-disturbs [26]. These bitcells together are referred to as "differential 10T bitcells" hereafter. For iso-area comparison, any additional area is used to upsize the write-access transistors. The differential 10T bitcell with two separate read ports consumes $\sim 1.66\times$ larger area compared with the 6T mincell. Therefore, for iso-area condition, the write access transistors in this bitcell are upsized by 2 × to give the same area as that of the ST bitcells (Fig. 8). Single-ended sensing 10T bitcells occupy 1.6 × area compared with the 6T mincell area [23], [24]. Single-ended 10T bitcells utilize read-disturb free operation. Hence, any additional area is used to increase the write-access transistor by 2 × for iso-area comparison. Table II lists device sizing for various bitcell topologies used for $\mathrm{V_{min}}$ analysis.

B. Read-Failure Probability

Read static noise margin (SNM) is used to quantify the read-stability of the SRAM bitcells. The SNM is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [40]. Read-failure probability ($\mathrm{P_{read\text{-}fail}}$) is estimated as

$$\mathrm{P_{read\text{-}fail}} = Prob.(\text{read SNM} < kT).$$

If read SNM is lower than the thermal voltage ($kT = 26$ mV at 300 K), the bitcell contents can be flipped due to thermal noise. Note that any other suitable threshold criteria can be used in estimating read-failure probability. Read-$\mathrm{V_{min}}$ is determined at the 6-sigma read-failure probability (i.e., $\mathrm{P_{read\text{-}fail}} = 1\mathrm{e}-9$).

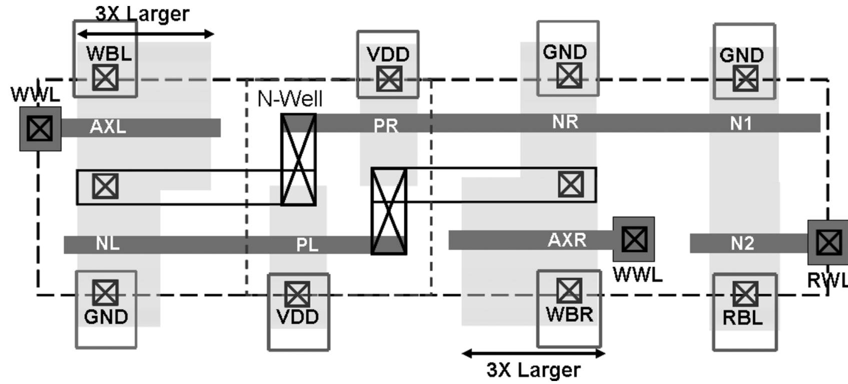


Fig. 7. Iso-area 8T thin-cell layout.

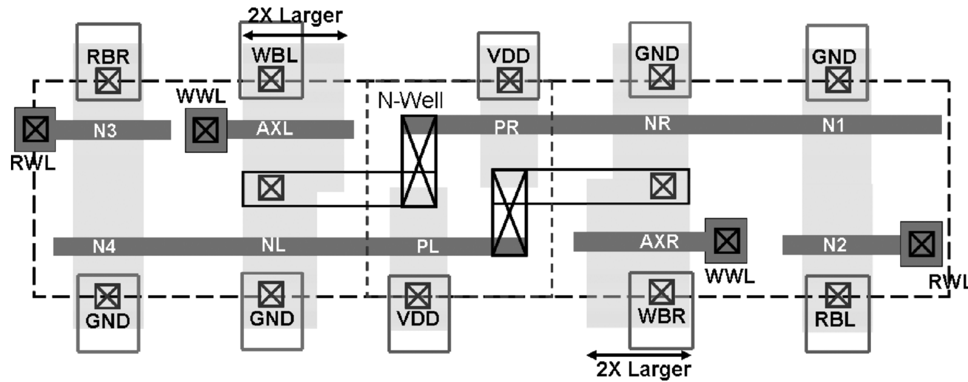


Fig. 8. Iso-area differential 10T cell layout.

TABLE II
DEVICE SIZING FOR VARIOUS BITCELL TOPOLOGIES

Sr. No.	Bitcell Topology	NL1/NR1	NL2 /NR2	PL/ PR	AXL/AXR	NFL/NFR	N1/N2	N3/N4
1	6T Mincell (1X Area)	200	-	100	100	-	-	-
2	6T bitcell (2X upsized)	400	-	200	200	-	-	-
3	6T bitcell (3X upsized)	600	-	300	300	-	-	-
4	6T bitcell (4X upsized, Iso-area)	800	-	400	400	-	-	-
5	6T bitcell (8X upsized)	1600	-	800	800	-	-	-
6	6T bitcell (12X upsized)	2400	-	1200	1200	-	-	-
7	8T Mincell	200	-	100	100	-	100	-
8	8T bitcell (Iso-subarray-area)	200	-	100	300	-	100	-
9	10T Diff. mincell	200	-	100	100	-	100	100
10	10T Diff. bitcell (Iso-area)	200	-	100	200	-	100	100
11	10T Diff. bitcell (Iso-area) [26]	200	-	100	200	-	100	100
12	Schmitt Trigger-1 (ST-1) bitcell	200	200	100	200	200	-	-
13	Schmitt Trigger-2 (ST-2) bitcell	200	200	100	200	200	-	-

Fig. 9 plots read-failure probability versus supply voltage for various 6T bitcell sizing. It is found that built-in process tolerance in the ST-2 bitcell gives lower read-failure probability compared with the iso-area 6T bitcell. For 8T and 10T bitcells, read-stability is same as the hold-mode stability as bitcell nodes are not disturbed during the read operation. As the cross-coupled inverter size in the 8T/10T bitcell is same as that for the 6T mincell, it would show similar hold-failure probability as shown in Fig. 10. Thus, read-failure probability in 8T/10T bitcell is lower than the ST bitcells. Lower read-failure probability would translate into lower read-$V_{\min}$ in 8T/10T bitcell compared with the ST bitcells.

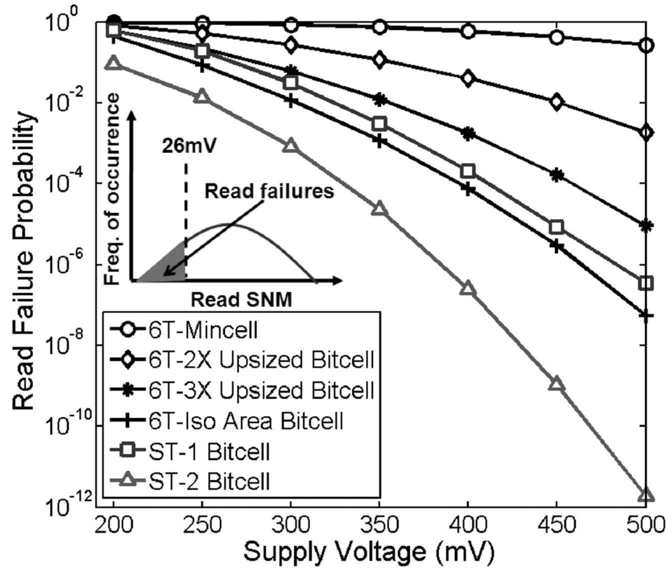


Fig. 9. 6T versus ST bitcell: read-failure probability comparison.

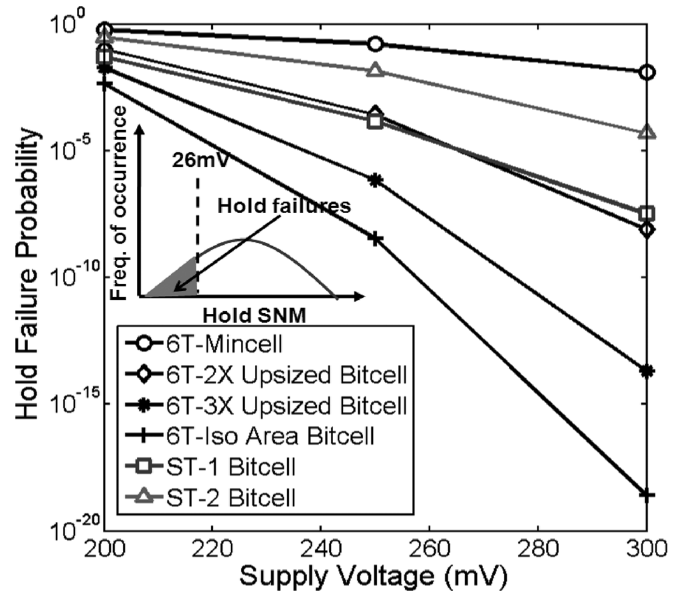


Fig. 10. 6T versus ST bitcell: hold-failure probability comparison.

C. Hold-Failure Probability

Similar to the read stability case, hold-stability is estimated by computing the hold SNM. Fig. 10 shows the hold-failure probability variation versus supply voltage for 6T and ST bitcells. As shown in inset, hold-failure probability ($P_{\text{hold-fail}}$) is estimated as

$$P_{\text{hold-fail}} = Prob.(\text{hold SNM} < kT).$$

Hold-$V_{\min}$ is determined at the 6-sigma hold failure probability (i.e., $P_{\text{hold-fail}} = 1e-9$). It is observed that upsizing 6T device dimensions give robust inverter characteristics. This gives lower hold-failure probability and lower hold-$V_{\min}$ compared to the minimum sized ST-1 and ST-2 bitcells. As explained above, the cross-coupled inverter pair size in 8T /10T bitcell and 6T mincell are same, it would result in similar hold-failure probabilities. As shown in Fig. 10, ST bitcells show lower hold-failure probability compared with the 6T mincell. Hence, ST bitcells would yield lower hold-$V_{\min}$ compared with the 8T/10T bitcell.

Note that ST-1 bitcells having internal node-based feedback give improved hold-failure characteristics compared with the ST-2 bitcell. For the ST-2 bitcell, WL and WWL control signals are OFF during the hold-mode (Fig. 4).

D. Write-Failure Probability

Write-ability of a bitcell gives an indication of how easy or difficult it is to write to the bitcell. Write-trip-point defines the maximum 0-side bitline voltage needed to flip the cell content [41]. The higher the 0-side bitline write-trip-point voltage, the easier it is to write to the cell. Fig. 11 shows the write-failure probability variation versus supply voltage. As shown in inset, write-failure probability ($P_{\text{write-fail}}$) is calculated as

$$P_{\text{write-fail}} = \text{Prob.}(\text{write-trip-point} < 0\text{ mV}).$$

Write-$V_{\min}$ is determined at the 6-sigma write-failure probability (i.e., $P_{\text{write-fail}} = 1e-9$). In case of ST-1 and ST-2 bitcell, absence of a feedback mechanism and series-connected pull-down nMOS transistors result in higher write-trip point compared with the 6T bitcell. Consequently, the proposed ST bitcells give lower write-$V_{\min}$ compared with the 6T bitcell. For ST-2 bitcell, WL and WWL control signals are asserted, resulting in lower write-failures compared with the ST-1 bitcell. Fig. 12 shows the comparison of write-failure probability for 8T and ST bitcells under iso-area condition. Upsizing the write-access transistor in 8T bitcell improves its write-ability. However, ST bitcells with series connected pull-down transistors give lower write-failure probability and lower write-$V_{\min}$ compared to 8T bitcell. Single-ended 10T bitcells would result in write-$V_{\min}$ similar to the 8T bitcell. Fig. 13 shows the write-failure probability comparison of the differential 10T bitcells and the ST bitcells under iso-area condition. The proposed ST-2 bitcell gives the lowest write-failure probability and hence the

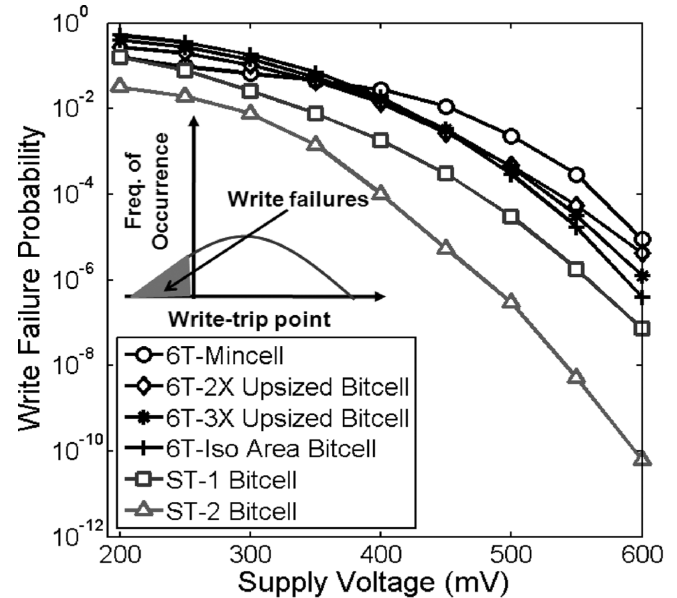


Fig. 11. 6T versus ST bitcell: write-failure probability comparison.

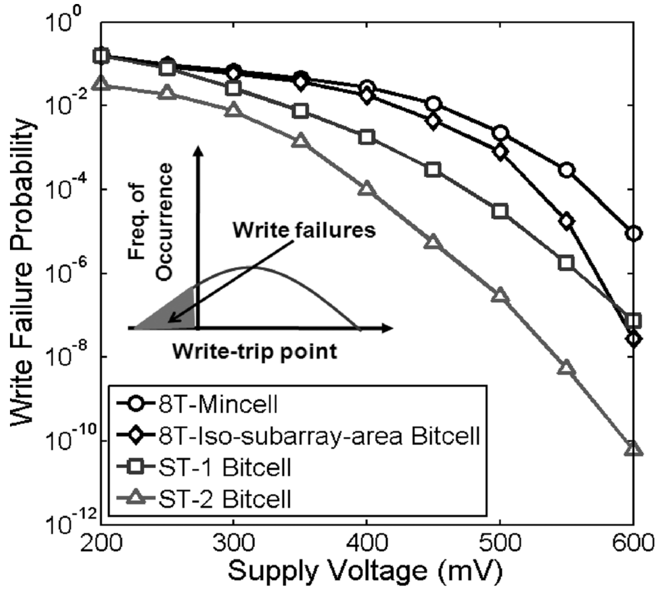


Fig. 12. 8T versus ST bitcell: write-failure probability comparison.

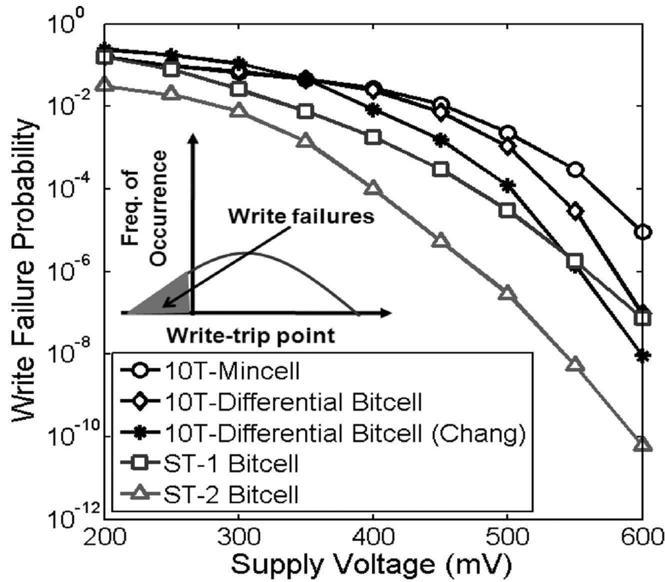


Fig. 13. 10T versus ST bitcell: write failure probability comparison.

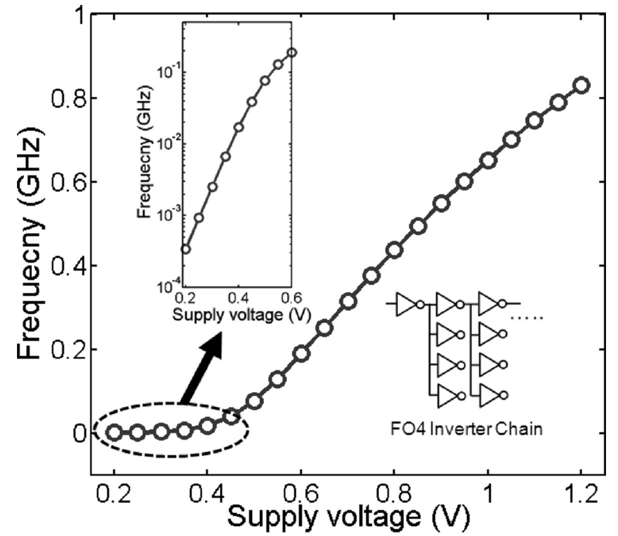


Fig. 14. Clock frequency variation with supply voltage.

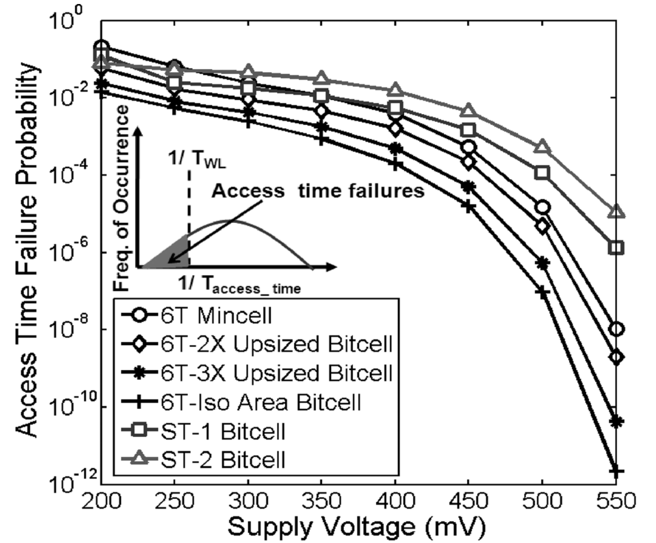


Fig. 15. 6T versus ST bitcell: access-time failure probability comparison.

lowest write-$\mathrm{V_{min}}$ compared with the differential 10T bitcells. The differential 10T bitcell proposed by Chang *et al.* contains two series-connected write-access transistors which degrades the write-ability of the bitcell.

E. Access-Time Failure Probability

Access-time ($\mathrm{T_{access}}$) is defined as the time required to produce a prespecified voltage difference ($\Delta \mathrm{V_{BL}} \approx 50\,\mathrm{mV}$) between two bitlines. If this bitline differential is less than the sense amplifier input offset voltage, sense amplifier's output may not resolve correctly resulting in incorrect data value. For a given supply voltage, the access-time failure depends on array organization viz. bitcell read-current, bitline capacitance (number of bitcells/column), word-line pulse-width, bitline leakage, column multiplexer series resistance and sense amplifier offset voltage. As the bitline differential depends on the word-line pulse-width, it is essential to obtain the variation of clock frequency with the supply voltage scaling (Fig. 14). In this case, the delay of 20 minimum-sized FO4 (fan out of 4) inverters is assumed to be one clock period. The SRAM cycle time is one clock period in which the word-line is activated in the first phase and the sense amplifier is activated in the next phase. One hundred twenty-eight bitcells are assumed on a column. Data pattern for the worst case bitline leakage is used (i. e. minimum bitline differential). It has been shown that, instead of $\mathrm{T_{access}}$, the inverse of $\mathrm{T_{access}}$ gives normal distribution [42]. Hence, access-time failure probability ($\mathrm{P_{access_time\text{-}fail}}$) is calculated as

$$\mathrm{P_{access_time\text{-}fail}} = \mathrm{Prob.}\left(\frac{1}{\mathrm{T_{access}}} < \frac{1}{\mathrm{T_{WL}}}\right)$$

where $\mathrm{T_{WL}}$ = word-line pulse-width.

Access-$\mathrm{V_{min}}$ is determined at the 6-sigma access time failure probability (i.e., $\mathrm{P_{access_time\text{-}fail}} = 1\mathrm{e}-9$). Fig. 15 shows the

TABLE III
Vmin COMPARISON OF VARIOUS BITCELL TOPOLOGIES

Sr. No.	Bitcell Topology	Read Vmin (mV)	Write Vmin (mV)	Hold Vmin (mV)	Access-time Vmin (mV)	Normalized Area	Vmin (mV)
1	6T Mincell (1X Area)	1000	750	452	561	1	1000
2	6T bitcell (2X upsized)	724	724	307	553	1.33	724
3	6T bitcell (3X upsized)	608	691	268	533	1.67	691
4	6T bitcell (4X upsized, Iso-area)	540	665	252	521	2	665
5	6T bitcell (8X upsized)	398	609	216	510	3.33	609
6	6T bitcell (12X upsized)	340	584	208	504	4.66	584
7	8T Mincell	452	750	452	662	1.33	750
8	8T bitcell (Iso-subarray-area)	452	620	452	662	2	662
9	10T Diff. mincell	452	750	452	573	1.67	750
10	10T Diff. bitcell (Iso-area)	452	650	452	573	2	650
11	10T Diff. bitcell (Iso-area) [26]	452	616	452	573	2	616
12	Schmitt Trigger-1 (ST-1) bitcell	586	650	319	600	2	650
13	Schmitt Trigger-2 (ST-2) bitcell	450	567	360	617	2	617

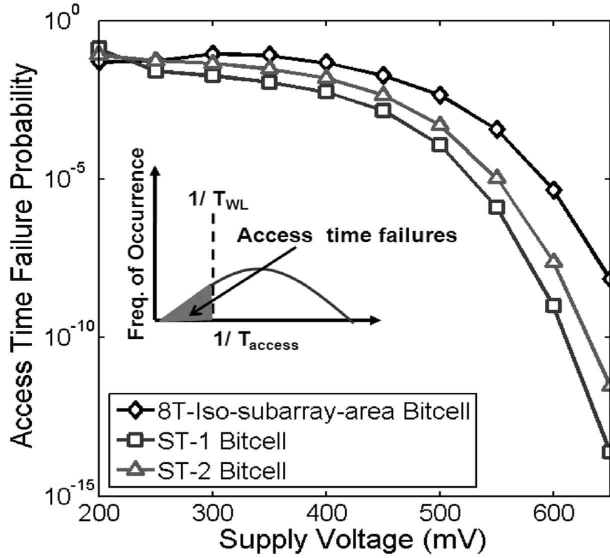


Fig. 16. 8T versus ST bitcell: access-time failure probability comparison.

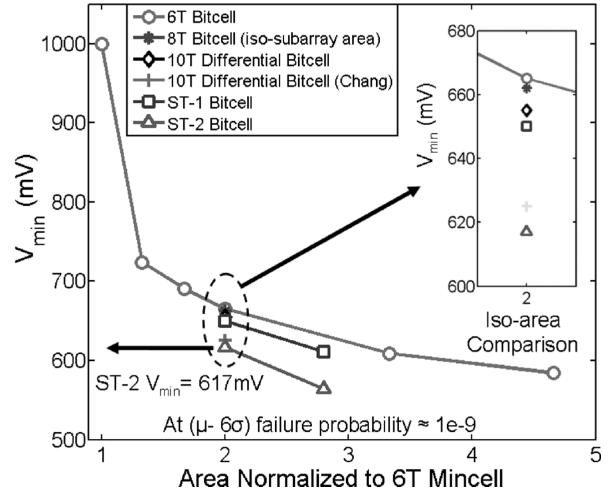


Fig. 17. Iso-area $\mathrm{V_{min}}$ comparison of 6T/8T/10T/ST bitcells.

access-time failure probability variation versus supply voltage for 6T and ST bitcells. It is found that upsized 6T bitcells give higher read-current compared with ST-1 and ST-2 bitcells, resulting in lower access-time failure probability and lower access-$\mathrm{V_{min}}$. ST-2 bitcell gives higher read current compared with the ST-1 bitcell. However, ST-1 bitcell shows better access-time failure probability due to lower bitline capacitance compared with the ST-2 bitcell case. For the 8T bitcell, 128 bitcells are arranged as shown in Fig. 6. The delay from RWL turn-ON to global bitline (GBL) evaluation is termed as the access-time. Fig. 16 shows the access-time failure probability comparison of the 8T bitcell and ST bitcells. At iso-area condition, differential sensing ST bitcells show improved access time compared to the single-ended sensing 8T bitcell. This analysis indicates that differential sensing can give higher performance compared to the single-ended sensing, as observed in [43]. Single-ended 10T bitcells would show access-time characteristics similar to 8T bitcells. For the differential 10T bitcell, the read access transistors are sized to have same read current as that of the 6T bitcell, it would result in similar access-time failure characteristics (Fig. 15).

F. Iso-Area $\mathrm{V_{min}}$ *Comparison*

Table III compares the estimated $\mathrm{V_{min}}$ for various bitcell topologies. Fig. 17 shows $\mathrm{V_{min}}$ comparison of 6T/8T/10T/ST bitcells under iso-area condition. $\mathrm{V_{min}}$ of a bitcell is determined at 6-sigma failure probability ($1e-9$). $\mathrm{V_{min}}$ is calculated as

$$\mathrm{V_{min}} = \mathrm{Max.[Read\text{-}V_{min}, Hold\text{-}V_{min}, Write\text{-}V_{min}, Access\text{-}V_{min}]}.$$

As seen in Fig. 17, the ST-2 bitcell shows the lowest $\mathrm{V_{min}}$ of 617 mV. Built-in feedback mechanism in ST-2 bitcell improves the read-stability. In addition, higher write-trip-point in

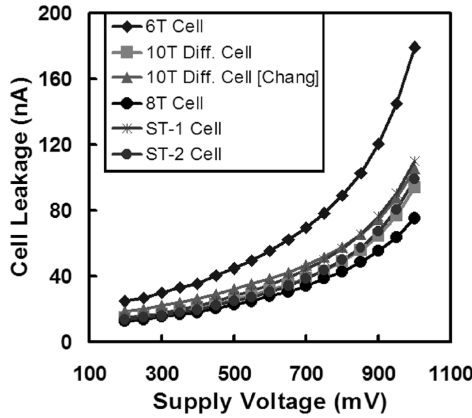


Fig. 18. Iso-area bitcell leakage current comparison.

ST-2 bitcell improves the write-ability. In spite of the read-disturb-free operation in 8T and 10T bitcells, their V_{min} is limited by the write operation. For this technology, 6T mincell transistor widths need to be upsized by $8\times$ (bitcell area increased by $3.3\times$) to achieve V_{min} same as the ST-2 bitcell. Note that the upsized ST bitcells show further V_{min} reduction. In this bitcell V_{min} analysis, we do not account the effect of various read/write assist techniques [5]. We believe that these techniques can be applied to the bitcell topologies for further V_{min} reduction.

G. Leakage Current Comparison

Leakage current is an important parameter in the bitcell design. Fig. 18 shows bitcell leakage comparison of 6T/8T/10T/ST bitcells under iso-area condition in 65 nm technology. ($\mathrm{Temp} = 110\,^{\circ}\mathrm{C}$, typical corner). It is found that iso-area 6T bitcell due to $4\times$ upsized transistors consumes $\sim 1.5\times$ higher leakage as compared with the ST bitcells. 10T differential and ST bitcells show comparable leakage current. Further, the ST-2 bitcell consumes lower leakage than the ST-1 bitcell. This is because, in the ST-2 bitcell, both feedback transistors are OFF in the hold mode unlike the ST-1 bitcell in which only one of the feedback transistors is OFF.

V. Measurement Results

A test-chip with 2Kb SRAM array containing 6T and ST-2 bitcells has been fabricated in 130-nm CMOS technology. For DC measurements, separate isolated 6T/ST-2 bitcells with each transistor having ten fingers were fabricated. Guard rings and dummy fingers (transistors) were implemented for the isolated cell layout in order to minimize the effect of process bias on the finger structures.

The finger structure would result in transistors having threshold voltage (V_T) same as that of the transistor used in the bitcell array. Thus, isolated-cell SNM measurement would be equivalent to the actual SRAM array bitcells. In order to characterize the memory failure statistics, built-in self-test circuit was designed [44]. SRAM tester circuit is described in our earlier work [31]. Measurements were done on ten different test-chips to fully characterize both 6T and ST bitcell. Fig. 19 shows the captured voltage transfer characteristics during the read and the hold mode in which the X and Y axes represent the voltages at the storage nodes. This graph clearly shows that

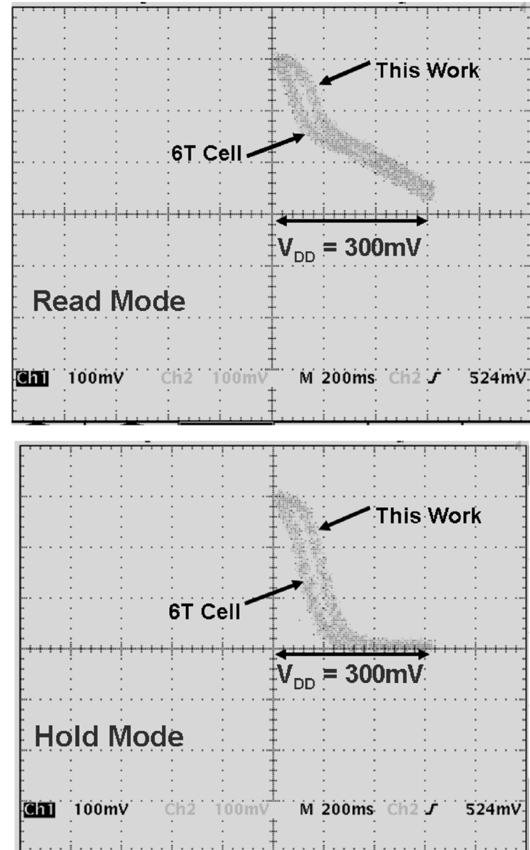


Fig. 19. Captured read and hold mode characteristics at 300 mV.

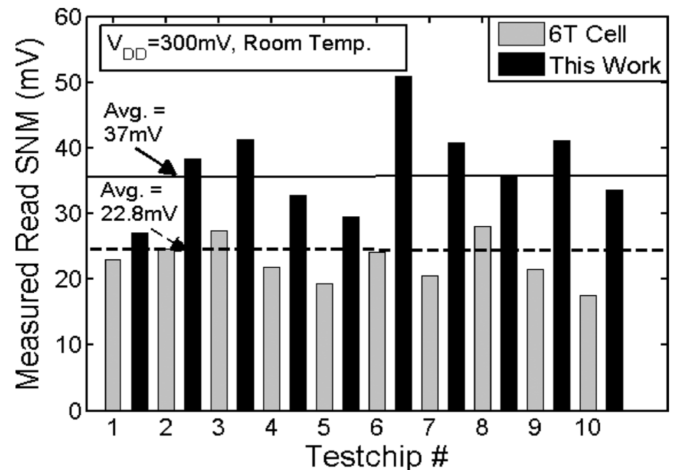


Fig. 20. Read SNM measurement with ten test-chips.

the proposed ST-2 bitcell exhibits improved read/hold mode characteristics compared to the conventional 6T bitcell.

Read-SNM measurements on 10 test-chips show that the proposed ST-2 bitcell on an average gives 58% higher read-SNM compared with 6T bitcell as shown in Fig. 20 ($V_{CC} = 300\,\mathrm{mV}$). The hold-SNM for 6T and ST-2 bitcell is found to be almost same (Fig. 21). The improvement in ST-2 bitcell read-SNM is consistent across different supply voltages as shown in Fig. 22.

The write-trip-point was determined by performing the weak-write-test [45]. Measured results show that the ST-2 bitcell gives $\sim 2\times$ higher write-trip-point compared to the 6T

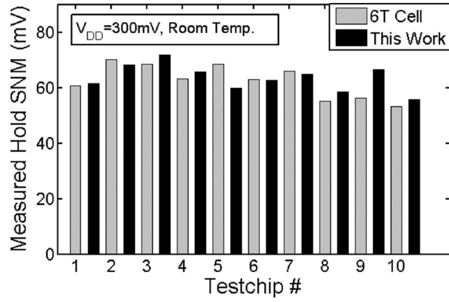


Fig. 21. Hold SNM measurement with ten test-chips.

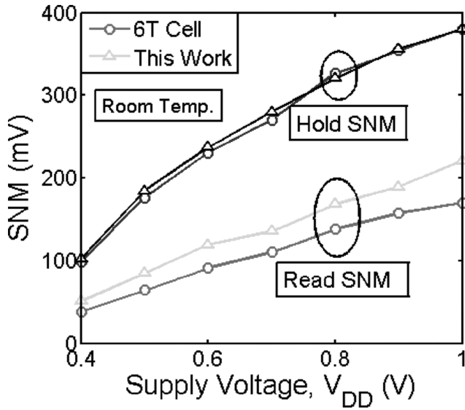


Fig. 22. Measured read/hold SNM versus VCC.

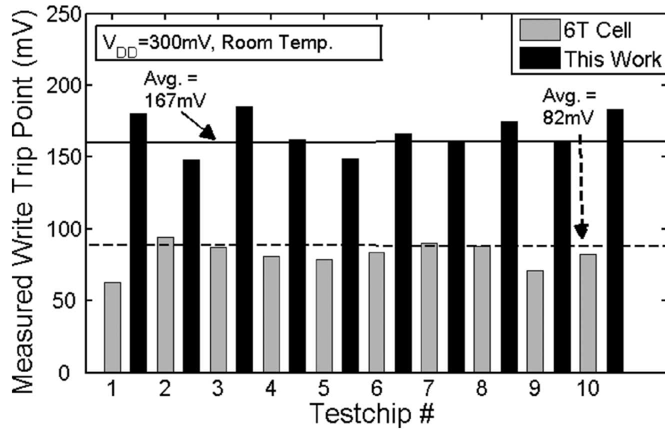


Fig. 23. Write-trip-point measurement with ten test-chips.

bitcell ($V_{CC} = 300$ mV, Fig. 23) which is consistent across wide range of supply voltage (Fig. 24).

Using the on chip tester circuit, ten test-chips were characterized for failure statistics. Supply voltage was reduced gradually and read failures were counted using the built-in counter. The clock frequency was kept low to avoid access-time failures.

Read-V_{min} was determined as the highest supply voltage where the first read failure occurred. As shown in Fig. 25, the proposed ST-2 bitcell with built-in feedback mechanism achieves 120 mV lower read-V_{min} compared to the standard 6T bitcell. Also, it is found that the weak-write-test (WWT) voltage is higher in the ST-2 bitcell compared to the 6T bitcell. At 300 mV, the operating frequency is 270 kHz with leakage

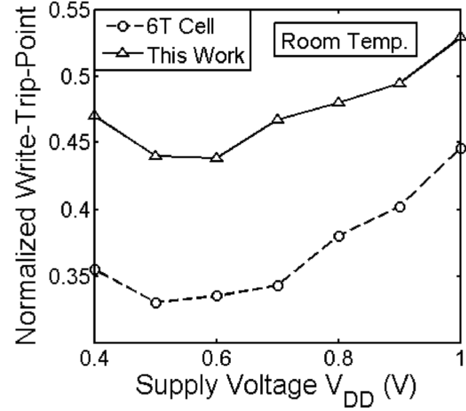


Fig. 24. Measured write-trip-point versus VCC for one test-chip.

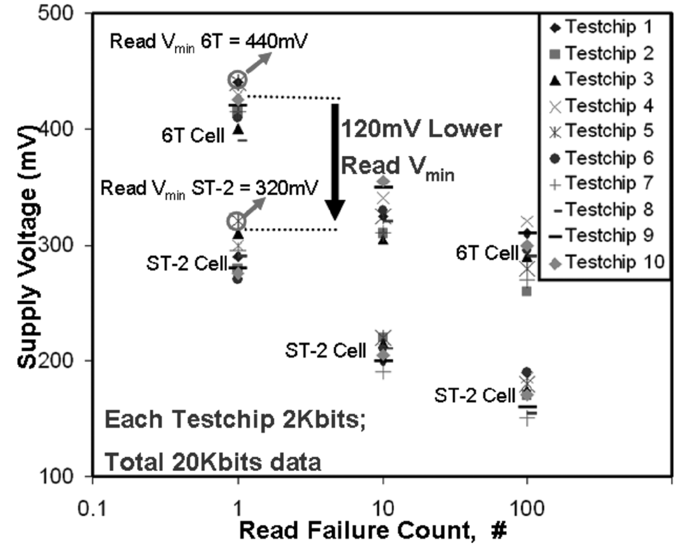


Fig. 25. Measured read failure statistics for ten test-chips.

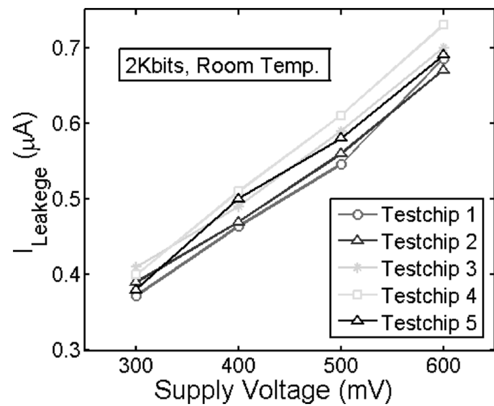


Fig. 26. Measured leakage current versus VCC for five test-chips.

power consumption of 0.11 μW (Fig. 26). Supply voltage was reduced gradually to determine the correct read functionality. The best case read-V_{CC} for the proposed ST-2 bitcell was 150 mV at 500 Hz (Fig. 27).

Fig. 28 shows the die photograph and the test-chip measurement summary. Fig. 29 shows the possible application space for the proposed ST-2 bitcell. Since the ST bitcells consume $2\times$

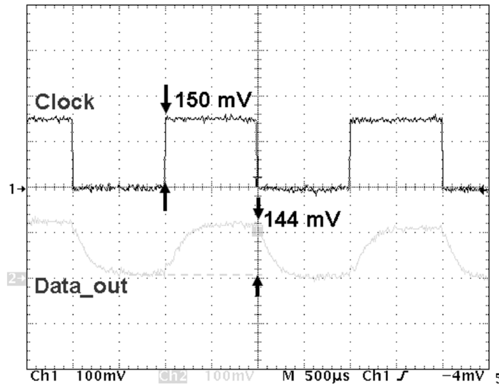
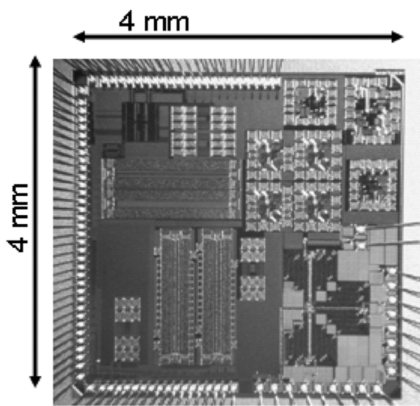


Fig. 27. ST-2 bitcell read operation at 150 mV/500 Hz.



Technology	0.13µm, 8-metal, CMOS
# Transistors	104 K
Silicon area	1.063 mm^2
Read V_{min}	320mV (20Kbits, Room Temp.)
Best case read V_{DD}	150mV (@ 500Hz, Room Temp.)
Frequency	270KHz (V_{DD} = 300mV, ΔV_{BL} = V_{DD} /2)
Leakage current	0.372µA (2Kbits, 300mV, Room Temp.)

Fig. 28. Die photograph and chip measurement summary.

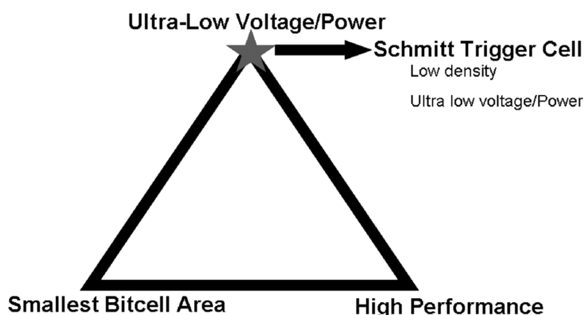


Fig. 29. ST SRAM bitcells: application space.

larger area compared with the 6T mincell, at iso-area, the upsized 6T bitcell has better performance compared with the ST bitcells (Fig. 15). However, due to built-in process tolerance, the proposed ST bitcells can potentially be useful in applications requiring ultra low voltage. Recently, Wilkerson *et al.* have proposed the use of ST-1 bitcell for tag-arrays to achieve low voltage cache operation [46].

VI. Conclusion

Lowering the supply voltage is an effective way to achieve ultra-low-power operation. In this work, we evaluated ST-based SRAM bitcells suitable for ultra-low-voltage applications. The built-in feedback mechanism in the proposed ST bitcell can be effective for process-tolerant, low-voltage SRAM operation in future nanoscaled technologies. Monte Carlo simulations in 65-nm technology predict lower $\mathrm{V_{min}}$ for the proposed ST-2 bitcell under the iso-area condition. Measurement results with a 130-nm test-chip clearly demonstrate the effectiveness of the proposed ST-2 bitcell for successful ultralow-voltage operation.

A. Future Work

In this paper, 6T/8T/10T/ST SRAM bitcell topologies are analyzed for achieving low voltage operation. ST bitcells offer low voltage operation with $2\times$ area overhead. On the other hand, various read/write assist techniques achieve significant $\mathrm{V_{min}}$ reduction, with lower area overhead. Hence, for a given $\mathrm{V_{min}}$ constraint, optimal combination of the bitcell topology + read/write assist technique should be chosen for minimal area/power overhead. Thus, the effectiveness of read/write assist techniques for each of the bitcell topology needs to be investigated for achieving lower $\mathrm{V_{min}}$.

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References

[1] K. Roy and S. Prasad, *Low Power CMOS VLSI Circuit Design*, 1st ed. New York: Wiley, 2000.

[2] N. Yoshinobu, H. Masahi, K. Takayuki, and K. Itoh, “Review and future prospects of low-voltage RAM circuits,” *IBM J. Res. Devel.*, vol. 47, no. 5/6, pp. 525–552, 2003.

[3] A. Bhavnagarwala, X. Tang, and J. Meindl, “The impact of intrinsic device fluctuations on CMOS SRAM cell stability,” *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[4] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, “Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS,” *IEEE Trans. Comput.-Aided Design (CAD) Integr. Circuits Syst.*, vol. 24, no. 12, pp. 1859–1880, Dec. 2005.

[5] M. M. Khellah, A. Keshavarzi, D. Somasekhar, T. Karnik, and V. De, “Read and write circuit assist techniques for improving Vccmin of dense 6T SRAM cell,” in *Proc. Int. Conf. Integr. Circuit Design Technol.*, Jun. 2008, pp. 185–189.

[6] K. Noda, K. Matsui, K. Takeda, and N. Nakamura, “A loadless CMOS four-transistor SRAM cell in a 0.18-μm logic technology,” *IEEE Trans. Electron Devices*, vol. 12, no. 12, pp. 2851–2855, Dec. 2001.

[7] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, “A high density, low leakage, 5T SRAM for embedded caches,” in *Proc. 30th Eur. Solid State Circuits Conf/*, Sep. 2004, pp. 215–218.

[8] B. Zhai, D. Blaauw, D. Sylvester, and S. Hanson, “A sub-200 mV 6 T SRAM in 0.13 μm CMOS,” in *Proc. Int. Solid State Circuits Conf.*, Feb. 2007, pp. 332–333.

[9] S. Tawfik and V. Kursun, “Low power and robust 7T dual-Vt SRAM circuit,” in *Proc. Int. Symp. Circuits Syst.*, 2008, pp. 1452–1455.

[10] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu, "A stable 2-port SRAM cell design against simultaneously read/write-disturbed accesses," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2109–2119, Sep. 2008.
[11] K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, "A read-static-noise-margin-free SRAM cell for low-V_{dd} and high-speed applications," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2005, pp. 478–479.
[12] R. Aly, M. Faisal, and A. Bayoumi, "Novel 7T SRAM cell for low power cache design," in *Proc. IEEE SOC Conf.*, 2005, pp. 171–174.
[13] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. R. Montoye, L. Sekaric, S. McNab, W. Topol, C. Adams, K. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in *Proc. Symp. VLSI Technol.*, 2005, pp. 128–129.
[14] N. Verma and A. P. Chandrakasan, "65 nm 8T sub-Vt SRAM employing sense-amplifier redundancy," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2007, pp. 328–329.
[15] R. Joshi, R. Houle, K. Batson, D. Rodko, P. Patel, W. Huott, R. Franch, Y. Chan, D. Plass, S. Wilson, and P. Wang, "6.6+ GHz low Vmin, read and half select disturb-free 1.2 Mb SRAM," in *Proc. VLSI Circuit Symp.*, Jun. 2007, pp. 250–251.
[16] V. Ramadurai, R. Joshi, and R. Kanj, "A disturb decoupled column select 8T SRAM cell," in *Proc. Custom Integr. Circuits Conf.*, Sep. 2007, pp. 25–28.
[17] Y. Morita, H. Fujiwara, H. Noguchi, Y. Iguchi, K. Nii, H. Kawaguchi, and M. Yoshimoto, "An area-conscious low-voltage-oriented 8T-SRAM design under DVS environment," in *Proc. VLSI Circuit Symp.*, Jun. 2007, pp. 14–16.
[18] Z. Liu and V. Kursun, "High read stability and low leakage cache memory cell," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 4, pp. 488–492, Apr. 2008.
[19] S. Lin, Y.-B. Kim, and F. Lombardi, "A highly-stable nanometer memory for low-power design," in *Proc. IEEE Int. Workshop Design Test of Nano Devices, Circuits Syst.*, 2008, pp. 17–20.
[20] S. Verkila, S. Bondada, and B. Amrutur, "A 100 MHz to 1 GHz, 0.35 V to 1.5 V supply 256 × 64 SRAM block using symmetrized 9T SRAM cell with controlled read," in *Proc. Int. Conf. VLSI Design*, 2008, pp. 560–565.
[21] M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Ohbayashi, Y. Nakase, and H. Shinohara, "A 45 nm 0.6 V cross-point 8T SRAM with negative biased read/write assist," in *Proc. VLSI Circuit Symp.*, 2009, pp. 222–223.
[22] M.-F. Chang, J.-J. Wu, K.-T. Chen, and H. Yamauchi, "A differential data aware power-supplied (D2AP) 8T SRAM cell with expanded write/read stabilities for lower VDDmin applications," in *Proc. VLSI Circuit Symp.*, 2009, pp. 222–223.
[23] B. H. Calhoun and A. P. Chandrakasan, "A 256 kb subthreshold SRAM in 65 nm CMOS," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2006, pp. 628–629.
[24] T.-H. Kim, J. Liu, J. Keane, and C.-H. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2007, pp. 330–331.
[25] H. Noguchi, S. Okumura, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, and M. Yoshimoto, "Which is the best dual-port SRAM in 45-nm process technology? — 8T, 10T single end, and 10T differential," in *Proc. IEEE Int. Conf. Integr. Circuit Design Technol.*, Jun. 2008, pp. 55–58.
[26] I. Chang, J.-J. Kim, S. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2008, pp. 628–629.
[27] S. Okumura, Y. Iguchi, S. Yoshimoto, H. Fujiwara, H. Noguchi, K. Nii, H. Kawaguchi, and M. Yoshimoto, "A 0.56-V 128 kb 10T SRAM using column line assist (CLA) scheme," in *Proc. Int. Symp. Quality Electron. Design (ISQED)*, May 2009, pp. 659–663.
[28] B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for subthreshold SRAM in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.
[29] J. Rabaey, A. chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2002.
[30] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
[31] J. P. Kulkarni, K. Kim, S. Park, and K. Roy, "Process variation tolerant SRAM array for ultra low voltage applications," in *Proc. Design Autom. Conf.* , Jun. 2008, pp. 108–113.
[32] F. Boeuf *et al.*, "0.248 $\mu\mathrm{m}^2$ and 0.334 $\mu\mathrm{m}^2$ conventional bulk 6T-SRAM bit -cells for 45 nm node low cost—general purpose applications," in *Proc. VLSI Technol. Symp.*, 2005, pp. 130–131.
[33] F. Arnaud *et al.*, "A functional 0.69 $\mu\mathrm{m}^2$ embedded 6T-SRAM bit cell for 65 nm CMOS platform," in *Proc. VLSI Technol. Symp.*, 2003, pp. 65–66.
[34] L. Chang, Y. Nakamura, R. K. Montoye, J. Sawada, A. K. Martin, K. Kinoshita, F. H. Gebara, K. B. Agarwal, D. J. Acharyya, W. Haensch, K. Hosokawa, and D. Jamsek, "A 5.3 GHz 8T-SRAM with operation down to 0.41 V in 65 nm CMOS," in *Proc. VLSI Circuit Symp.*, Jun. 2007, pp. 252–253.
[35] R. V. Joshi, S. P. Kowalczyk, Y. H. Chan, W. V. Huott, S. C. Wilson, and G. J. Scharff, "A 2 GHz cycle, 430 ps access time 34 Kb L1 directory SRAM in 1.5 V, 0.18 μm CMOS bulk technology," in *Proc. VLSI Circuit Symp.*, 2000, pp. 222–223.
[36] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "A SRAM design on 65 nm CMOS technology with integrated leakage reduction scheme," in *Proc. VLSI Circuit Symp.*, 2004, pp. 294–295.
[37] H. Pilo, V. Ramadurai, G. Braceras, J. Gabric, S. Lamphier, and Y. Tan, "A 450 ps access-time SRAM macro in 45 nm SOI featuring a two-stage sensing-scheme and dynamic power management," in *Proc. Int. Solid State Circuits Conf.*, Feb. 2008, pp. 378–379.
[38] D. W. Plass and Y. H. Chan, "IBM POWER6 SRAM arrays," *IBM J. Res. Devel.*, vol. 51, no. 6, pp. 747–756, Nov. 2007.
[39] H. Pilo, G. Braceras, S. Hall, S. Lamphier, M. Miller, A. Roberts, and R. Wistort, "A 0.9 ns random cycle 36 Mb network SRAM with 33 mW standby power," in *Proc. VLSI Circuit Symp.*, 2004, pp. 284–287.
[40] E. Seevinck, F. List, and J. Lohstroh, "Static noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 10, pp. 748–754, Oct. 1987.
[41] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of SRAM cells for nanometer technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, Nov. 2006.
[42] K. Agarwal and S. Nassif, "Statistical analysis of SRAM cell stability," in *Proc. Design Autom. Conf.*, 2006, pp. 57–62.
[43] Y. Ye, M. Khellah, D. Somasekhar, and V. De, "Evaluation of differential versus single-ended sensing and asymmetric cells in 90 nm logic technology for on-chip caches," in *Proc. Int. Symp. Circuits Syst.*, 2006, pp. 963–966.
[44] S. Mukhopadhyay, K. Kim, H. Mahmoodi, and K. Roy, "Design of a process variation tolerant self-repairing SRAM for yield enhancement in nano scaled CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1370–1382, Jun. 2007.
[45] A. Meixner and J. Banik, "Weak write test mode: An SRAM cell stability design for test technique," in *Proc. Int. Test Conf.*, Nov. 1997, pp. 1043–1052.
[46] C. Wilkerson, H. Gao, A. R. Alameldeen, Z. Chishti, M. Khellah, and S.-L. Lu, "Trading off cache capacity for reliability to enable low voltage operation," in *Proc. 35th Int. Symp. Computer Architecture (ISCA)*, Jun. 2008, pp. 203–214.

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