Nano Spiral Inductors for Low-Power Digital Spintronic Circuits

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We propose nano-scaled spiral inductors suitable for future low-power digital spintronic circuits. The proposed nano-spiral inductors can be effectively used to generate magnetic field in a class of spintronic logic/memory circuits such as magnetic random access memory (MRAM) and magnetic quantum cellular automata (MQCA). Measured results on 0.13 μm test-chip demonstrate the effectiveness of the proposed nano-spiral inductors and we estimate 3.36$\times$ lower write-current in MRAMs and 85% lower clocking energy in MQCAs.

***Index Terms*—Low-power operation, magnetic quantum cellular automata, magnetic random access memory, spintronics, spiral inductors.**

I. Introduction

With aggressive scaling of transistor dimensions, CMOS technology is approaching the limits of minimum power consumption [1]. To minimize the switching energy further, spintronic devices utilizing the electron spin for the logic/memory computations are investigated for future low-power digital circuits since the switching energy in spin based devices can be substantially lower than the corresponding CMOS counterpart [2]–[4]. In MRAMs, magnetic orientations of ferromagnetic layers are used to store the data [5]. In case of MQCAs, magnetic polarizations of nano-magnets are used for the logic computation [6]. External magnetic field is required to initiate a write (logic) operation in MRAM (MQCA). Current pulses are passed through conducting wires which generate the necessary magnetic field. However, significantly large amount of current is required to generate this magnetic field [5]. Hence, for future low-power digital spintronic circuits, it is necessary to generate the required magnetic field with reduced current.

In this paper, we propose nano-spiral inductor structure for reducing the current to generate the magnetic field in digital spintronic circuits. The paper is organized as follows. Section II presents basics of MRAM and MQCA operation. Proposed nano-spiral inductors are presented in Section III. Section IV shows the simulation results. Measurement results are presented in Section V. Section VI concludes the paper.

II. The Basics

1) MRAM Basics: The basic storage unit of an MRAM bit-cell is comprised of one magnetic tunnel junction (MTJ) and one transistor. An MTJ structure consists of two ferromagnetic layers separated by a tunneling layer (oxide) as shown in Fig. 1(a). The data is stored in a bit-cell by manipulating the relative magnetic orientation of one layer with respect to the other layer. The magnetic orientation of one layer is fixed (called as fixed layer) while the magnetic orientation of the other layer can be altered by the application of the magnetic field (called free layer). The relative orientation of the free layer with respect to the fixed layer modulates the tunneling current flowing through the MTJ, thereby changing the resistance of the tunnel junction. Parallel orientation of the ferromagnetic layers results in lower resistance compared to the antiparallel orientation. Thus, the contents of an MRAM bit-cell are determined by sensing the relative magnitude of the current flowing through the MTJ. During read operation, word-line is activated by turning ON the isolation transistor (Fig. 1(a)). During write operation, isolation transistor is OFF.

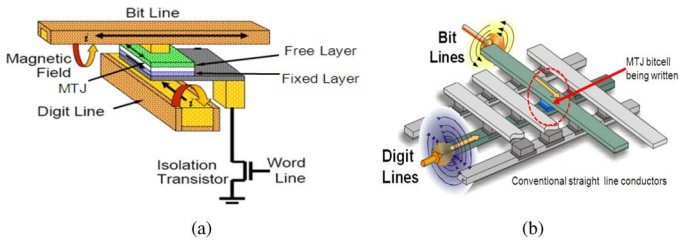

Fig. 1. (a) 1T-1MTJ structure in MRAM [5]. (b) Magnetic field assisted MRAM write operation [5].

In a conventional MRAM, the bit-line and the digit-line are placed in orthogonal direction surrounding an MTJ (Fig. 1(b)). The current flow in digit-line is unidirectional. The relative magnetic orientation of the free layer is changed by passing current through the bit-line in either direction. The magnetic field generated at the intersection of these current carrying conductors switches the magnetic orientation of the free layer resulting in successful write operation. Although digit-line current lowers the bit-line current required for a successful write operation, the write current to switch the magnetic orientation of the free layer is still high (~5–10 mA).

Higher write currents translate into higher power dissipation (I^2R power), higher resistive drop along the digit-line and bit-line (IR drop), higher magnetic cross-coupling and electro-migration issues. Increased magnetic cross coupling may limit spacing of MRAM bit-cells and may affect MRAM bit density. Higher IR drop necessitates use of wider metal lines resulting in higher power dissipation. Several technological solutions such as cladding metal lines, use of different ferromagnetic layers, and spin-torque based MRAMs have been proposed to reduce the required write current [5], [7].

2) MQCA Basics: Magnetic Quantum Cellular Automata (MQCA) is a computation paradigm to achieve very low-power dissipation. Magnetic QCAs use nano-scale magnets to form the quantum cells and the information in the cell is encoded in the

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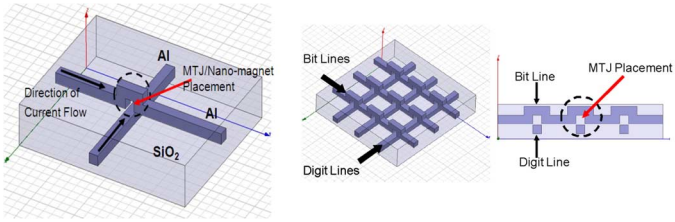
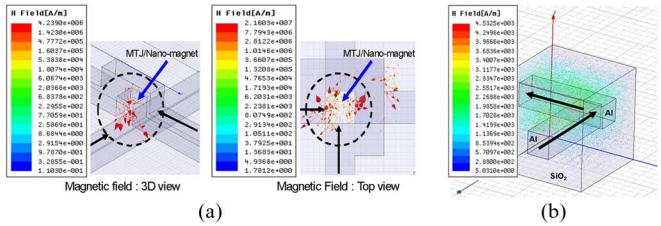


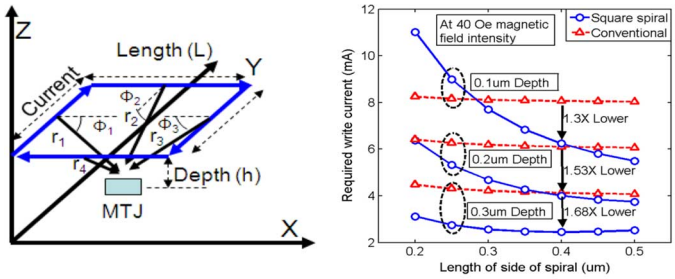
(a) (b)

Fig. 2. (a) Proposed vertical nano-spiral inductor structure. (b) Bit-line and digit-line layout employing vertical nano-spiral inductor.



(a) (b)

Fig. 3. (a) 3-D EM field simulation: vertical and planar nano-spiral inductor. (b) 3-D EM field simulation: orthogonal metal lines.



(a) (b)

Fig. 4. (a) Magnetic field estimation: planar nano-spiral inductor. (b) Write current vs. spiral side length at iso-magnetic field intensity.

form of magnetic polarizations of the nano-magnets. The preferred direction of magnetic polarization (the low energy state) is called the "easy axis" while the axis with highest energy polarization is called "hard axis." Boolean logic operations are performed utilizing the dipolar magnetic coupling between the adjacent nano-magnets. A clock signal is used to align magnetic moments of nano-magnets along the hard axis [11]. The output magnetic polarization of a logic gate is then determined by the effective input polarization. Moreover, room temperature MQCA operation using present fabrication techniques has been successfully demonstrated [6].

In such magnetic field assisted spintronic circuits, power is consumed in: 1) switching the magnetic moments of an MTJ free layer/nano-magnet; 2) clocking wires that carry the current necessary to generate the magnetic field (I^2R power); and 3) clock generation [11]. It has been shown that a large external magnetic field would be required to control/store the logical state in these spin based circuits [9]. Thus, for realizing future low-power digital spintronic circuits, it is necessary to maximize the efficiency of magnetic field generation per unit current.

III. Proposed Nano-Spiral Inductors

Our aim is to achieve same switching magnetic field but at a much lower current level. We propose nano-spiral inductors to minimize the current required to generate the necessary magnetic field. The straight line conductors are shaped to form nano-scale spiral inductors near the MTJ structures in MRAMs (nano-magnets in MQCA) (Fig. 2(a) and (b)). In this case, a vertical spiral structure is formed in the bit-line. MTJ would be placed within the spiral structure. Similarly, planar spiral can be formed in bit-lines as well as digit lines. This structure is similar to the planar spiral inductor with very small dimensions. Hence it is termed as "nano-spiral inductor." The MTJ would be placed at the intersection of the spiral regions. The nano-spiral inductor acts as a flux concentrator and achieves higher magnetic field (for a given current) inside the spiral region compared to a conventional layout. Thus, for generating the same magnetic field, the required write-current is reduced. This would result in low-power dissipation, reduced magnetic cross-coupling, and reduced electro-migration.

The primary design requirement for the proposed nano-spiral inductor is magnetic field concentration rather than high quality factor and low-parasitic capacitance as required in the traditional radio frequency (RF) circuit design. Principles of on-chip RF spiral inductors can be extended to the nano-scale dimensions to achieve higher magnetic field intensity at a given current level. Note that the MRAM write cycle time is of the order of a few nano-seconds [5]. Hence, the proposed tiny spiral inductor is operating at lower frequencies (sub-GHz range) unlike the traditional RF spiral inductor.

Three-dimensional electromagnetic wave simulations are performed for the square planar spiral and vertical spiral structure [8]. The orthogonal aluminum metal lines incorporating conventional and the proposed spiral structure are simulated. The width and the thickness of the metal lines is 0.5 μm. The length of a spiral segment is 0.5 μm, with the spacing of 0.5 μm. Thus, layout area for the planar spiral structure is 1.25 μm (length) $\times$ 0.5 μm (width). Silicon dioxide (SiO_2) parameters are used for surrounding dielectric material. A current of 5 mA (1 ns cycle time) is passed through the metal lines. The magnetic field surrounding the spiral region is observed. Fig. 3(a) shows the simulated magnetic field intensity (H) inside the vertical and planar spiral structure. The magnetic field generated in case of conventional orthogonal metal lines is shown in Fig. 3(b). It is observed that the magnetic field is concentrated inside the spiral structure and significantly higher than the conventional orthogonal metal lines as shown in Fig. 3(a) and (b).

IV. Simulation Results and Discussion

In order to quantify the write current reduction, the magnetic field intensity due to nano-spiral inductor is estimated. Fig. 4(a) shows the conceptual schematic of the current loop for square planar nano-spiral inductor.

Magnetic Field Estimation: Using Biot-Savart law, the magnetic field intensity at a radial distance "r" surrounding a current carrying conductor of length "L" is given by [9]:

$$\vec{H}_1 = \frac{\hat{\phi} I}{4\pi r}\left[\frac{\frac{L}{2}+z}{\sqrt{r^2+\left(\frac{L}{2}+z\right)^2}}+\frac{\frac{L}{2}-z}{\sqrt{r^2+\left(\frac{L}{2}-z\right)^2}}\right]$$

where I = current flowing through the conductor, z = distance of the observation point from the center of the current carrying

conductor. For the square spiral structure shown Fig. 4(a), the radial distance is given by

$$r = \sqrt{\left(\frac{L}{2}\right)^2 + h^2}$$

where L = length of the spiral, h = depth of the MTJ from the spiral structure, and $z = 0$ as the magnetic field is evaluated at the center of the spiral. For a square spiral structure, the effective magnetic field near MTJ would be vector sum of individual field components

$$\vec{H} = \vec{H}_1 + \vec{H}_2 + \vec{H}_3 + \vec{H}_4.$$

The effective Z-direction field would be

$$\vec{H}_z = \vec{H}_{1z} + \vec{H}_{2z} + \vec{H}_{3z} + \vec{H}_{4z}.$$

The Z-direction component of individual magnetic field is

$$\vec{H}_{1z} = \vec{H}_1 \times \cos(\phi_1), \quad \text{where} \quad \cos(\phi_1) = \frac{\frac{L}{2}}{\sqrt{\left(\frac{L}{2}\right)^2 + h^2}}.$$

Note that the effective magnetic field due to a current carrying square spiral is in Z-direction. The ferromagnetic layers forming the MTJ should be positioned such that the magnetic orientation in free layer is modulated by the application of magnetic field in Z-direction. At iso-magnetic field intensity (40 Oe) and for 0.1 μm MTJ depth, analytical estimation shows 30% lower write-current for square planar spiral compared to the straight line conductor (Fig. 4(b)).

In case of "vertical spiral," the MTJ would be placed inside the spiral structure. The total magnetic field is the scalar sum of the individual field components. Hence, the proposed vertical nano-spiral would give 3X current reduction compared to the conventional case. Note that the resultant magnetic field in this case is directed in Y direction.

In case of MQCAs, most of the energy is consumed in generating the external magnetic field [11]. In such case, proposed nano-spiral inductors can be used for low-power MQCA clocking schemes.

Resistance Estimation: Since the proposed spiral inductor scheme incurs increased metal length, it would exhibit higher line resistance. Hence, a tradeoff exists between the reduction in the current and the increase in the line resistance. For a conventional straight metal conductor, the resistance is

$$\mathrm{R_{conv}} = \rho \mathrm{l}/\mathrm{A}$$

where ρ = resistivity, l = metal length, A = cross section area.

In case of square spiral, the total resistance is estimated as

$$\mathrm{R_{sq\_spiral}} = \rho \mathrm{l}/\mathrm{A} + 3\mathrm{N}\,(\rho \mathrm{l_{spiral}}/\mathrm{A})$$

where N = number of MTJ cells/bit-line and $\mathrm{l_{spiral}}$ = side length of the spiral.

Although line resistance increases, the IR drop may not be significant since the reduced current limits the IR drop. The detailed schematic of a vertical spiral surrounding an MTJ is shown in Fig. 5. The vertical spiral resistance is given by

$$\mathrm{R_{vert\_spiral}} = \rho \mathrm{l}/\mathrm{A} + 2\mathrm{N}\,(\mathrm{R_{via}}/\mathrm{M})$$

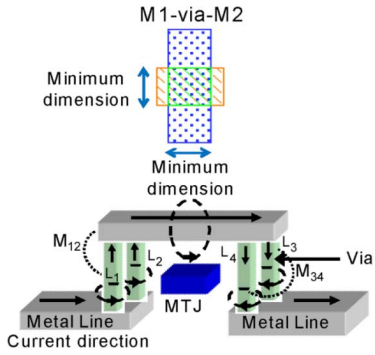


Fig. 5. Vertical spiral structure with multiple vias.

where N = number of cells/bit-line, $\mathrm{R_{via}}$ = via resistance, and M = number of vias per contact.

By increasing number of vias, effective contact resistance can be reduced. In addition, individual via segment carrying current in the same direction exhibit an additional mutual inductance, thereby increasing the magnetic field intensity. Thus, a vertical spiral structure with multiple vias would give more than 3X current reduction compared to the conventional structure.

Area Comparison: Dimensions of the proposed nano-spiral inductor should be such that the bit-cell area is not increased. This would not affect the MRAM bit density. Since the required current is lower in the proposed nano-spiral inductors, the width of the metal lines can be reduced due to reduced electro-migration. A narrower metal line gives higher inductance thereby generating higher magnetic field [10].

Scalability: As MTJ size is reduced, the MRAM bit-cell state can be altered undesirably by the thermal agitation. Due to the application of write current, the switching threshold of the unselected cells (half-selected cells) is reduced. These half-selected MTJ cells are prone to unwanted switching (i.e., write disturb) due to thermal fluctuations. Hence, the write threshold (switching magnetic field) needs to be raised with the scaling of MTJ dimensions. This results in higher write current requirement. The planar structure (square and circular) would have limited scalability as their dimensions may not be scaled due to lithography limitations. However, vertical spiral does not incur area penalty as the spiral structure is formed vertically and hence is scalable. The nano-spiral inductors can be employed in MRAM designs without affecting MTJ fabrication process.

V. Measurement Results

A test-chip containing four nano-spiral inductor structures has been fabricated using 130 nm technology (Fig. 6). Conventional, square, and hexagonal nano-spirals were implemented using metal-1 and metal-2 layers. Fig. 5 shows the layout view of via contact (M1-via-M2) and is fabricated with minimum dimensions allowed by the technology. Each contact contains four vias to reduce the resistance and to increase mutual inductance resulting in lower current requirement. The dimensions of fabricated spiral structure were identical to the values used in simulation as discussed in Section III.

Each test structure consists of 1500 series connected nano-spiral inductors. This would give observable inductance values. De-embedded scattering (S) parameters were measured using Agilent 8722 network analyzer and Cascade GSG probes.

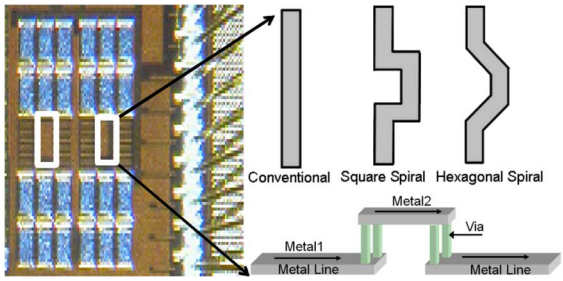


Fig. 6. 130 nm Die photograph: various spiral structures are annotated.

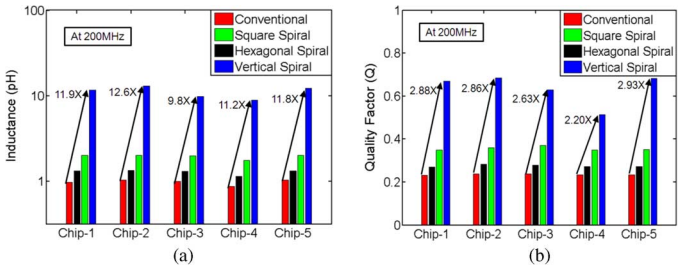


Fig. 7. (a) Measured inductance value at 200 MHz for 5 test-chips. (b) Measured quality factor at 200 MHz for 5 test-chips.

The measurements were restricted to low frequencies (up to 300 MHz) to be consistent with MRAM write cycle time (~3–5 ns). The proposed nano-spiral inductors showed higher inductance values compared to the conventional straight line conductors (Fig. 7(a)). Consistent improvement in the inductance values are observed for various test-chips (Fig. 7(a)). The vertical nano-spiral inductor showed maximum 11.46X improvement in the inductance compared to the conventional case. The energy stored in an inductor is given by

$$\mathrm{E_{inductor}} = (1/2)\mathrm{LI}^2.$$

For the same inductor energy, any increase in the inductor value due to nano-spirals would necessitate lower write-current ($\mathrm{I}\alpha\sqrt{\mathrm{L}^{-1}}$). Thus, 11.46X improved inductance due to vertical nano-spirals would result in 3.36X lower current at iso-magnetic field condition (Table I). Further, the proposed nano-spiral inductors showed higher quality factor compared to the conventional case with vertical spiral showing maximum (2.7X) quality factor improvement (Fig. 7(b)). Quality factor improvement was consistent for different test-chip measurements as shown in Fig. 7(b). Table I lists the average quality factor (Q) measured at 200 MHz. Based on the measured inductance values and using the MQCA circuit simulation framework, we estimate 85% lower clocking energy using vertical spiral inductor compared to the parallel wire clocking scheme (Fig. 8) [11].

VI. Conclusion

The proposed nano-scale inductors can be effectively used to generate the necessary magnetic field requiring lower current. The principles of RF spiral inductors can be extended to nano-scale dimensions to minimize power consumption in digital spintronic circuits. Thus, RF and digital design principles

TABLE I
ESTIMATED CURRENT REDUCTION DUE TO NANO-SPIRAL INDUCTORS (FREQUENCY = 200 MHz)

Inductor Structure	Average Quality Factor (Q)	Norm. Measured Inductance at 200MHz	Expected Current Reduction
Conv. Structure	0.22	1	-
Square Spiral	0.25	1.99	1.41X
Hexagonal Spiral	0.36	1.32	1.14X
Vertical Spiral	0.6	11.36	3.36X

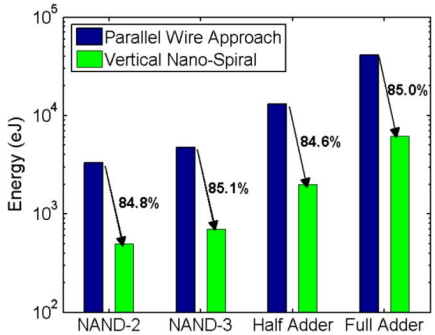


Fig. 8. MQCA clocking energy comparison, parallel wire vs. proposed vertical nano-spirals.

can be simultaneously applied for energy efficient spintronic logic/memory circuits to continue scaling in post-CMOS era.

Acknowledgment

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