Technology Circuit Co-Design for Ultra Fast InSb Quantum Well Transistors

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***Abstract*—Indium antimonide (InSb)-based quantum-well field-effect transistors (QWFETs) are conceived as a promising candidate for low-voltage high-performance applications. In this paper, we show complete technology-circuit assessment of InSb-based QWFETs. The codesign approach spans from the device/SPICE models, logic/memory circuit analysis, to technology requirements. We show the feasibility of the use of Si + InSb hybrid technology for future high-speed low-voltage applications. We prescribe the technology requirements as well as suggest the application space for InSb transistors.**

***Index Terms*—Compound semiconductor, indium antimonide (InSb), low-voltage applications, quantum-well field-effect transistors (QWFETs).**

I. Introduction

AGGRESSIVE scaling of transistor dimensions has resulted in increased integration density and improved device performance at the expense of increased power dissipation. Increased integration density along with increased leakage necessitates ultralow-power operation in present power constrained design environment [1]. Power reduction methods include the following: voltage scaling, switching activity reduction, architectural techniques of pipelining and parallelism, and CAD issues of device sizing, interconnect, and logic optimization [2]. Among these methods, power supply reduction has significant effect on power savings. Reducing the supply voltage reduces dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of low-power design. However, to improve the performance at a lower supply voltage, we need ultrafast transistors having better driving capability (ON current). Various materials and structures such as carbon nanotubes, semiconducting nanowires and III–V semiconductors are being explored for high-speed low-voltage applications [3], [9]. These materials have higher carrier mobility (either electron or hole) compared to silicon, making them potentially useful for high-speed computations. Carbon nanotubes and semiconducting nanowires, however, can be fabricated using "bottom-up" chemical synthesis methods and are prone to the problem of parallel alignment and series contact resistance [3].

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TABLE I
SEMICONDUCTOR MATERIAL PROPERTIES AT 300 K

	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility (cm^2/vs) $n_s = 10^{12}/cm^2$	600	4600	7800	20000	30000
Electron Saturation Velocity ($10^7 cm/s$)	1.0	1.2	0.8	3.5	5.0
Ballistic Mean Free Path (nm)	28	80	106	194	226
Energy Band-gap (eV)	1.12	1.42	0.72	0.36	0.18

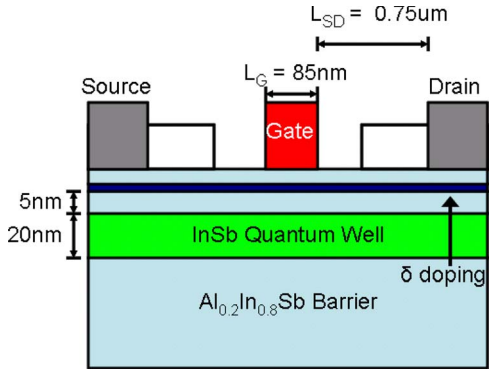

Fig. 1. The 85-nm L_G InSb/$Al_{0.2}In_{0.8}Sb$ QWFET: Layers from the bottom to top consist of an accommodation layer, $Al_yIn_{1-y}Sb$ buffer (3 μm), InSb quantum well (20 nm), $Al_{0.2}In_{0.8}Sb$ spacer (5 nm), a single Te-doped donor layer and $Al_{0.2}In_{0.8}Sb$ barrier layer (45 nm) [8].

On the other hand, III–V semiconductor-based transistors are formed using conventional "top-down" patterning approach and, hence, can easily be fabricated using the present lithographical techniques. III–V semiconductors have superior electron mobility (~50–100 X) compared to silicon (Si), giving higher I_{ON} even at lower supply voltage. Table I shows the material properties of various III–V semiconductors along with silicon [4]–[7]. Among the available III–V semiconductors, indium antimonide (InSb) has the highest electron mobility, saturation velocity, and ballistic length. Hence, InSb-based devices are good candidates for ultra fast applications. Recently, researchers have successfully demonstrated InSb quantum-well field-effect transistors (QWFETs) with sub-100-nm channel length for high-speed applications (Fig. 1) [8].

In this paper, we have analyzed technology circuit co-design aspects for InSb QWFETs. The codesign approach spans Device/SPICE models → Logic and memory circuits → InSb technology requirements (Fig. 2). We show the feasibility of the use of Si + InSb hybrid technology for high-speed logic and memory applications. We suggest technology requirements for future deployment of InSb transistors. Furthermore, we suggest the application space of InSb transistors.

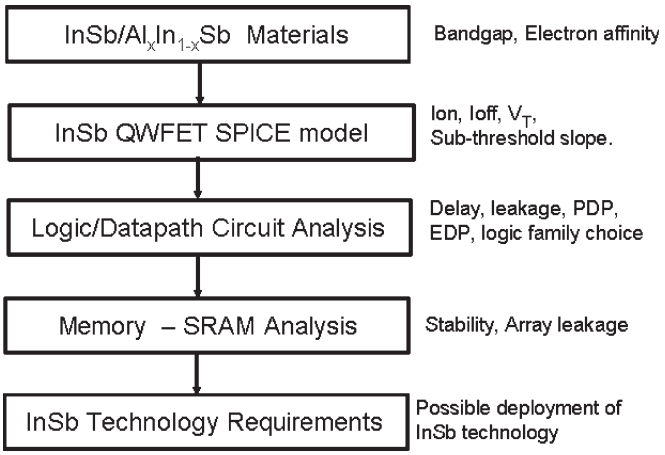

Fig. 2. Hierarchical modeling methodology: staring from the heterostructure material properties, developing SPICE models, logic and memory circuit analysis. This methodology suggests the InSb technology requirements as well as the application space of InSb transistors.

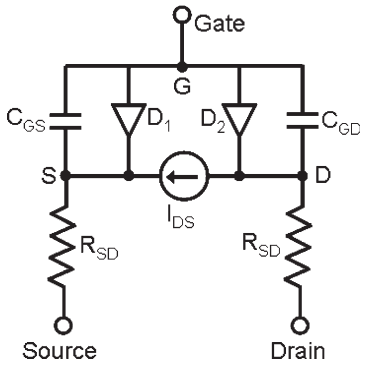

Fig. 3. QWFET SPICE model based on Heterostructure FET physics. Diodes D1 and D2 model Schottky diodes present between gate and source/drain. $R_{\rm SD}$ models the series resistance due to heterostructure interface as well as the separation between the gate and source/drain. $C_{\rm GS}$ and $C_{\rm GD}$ model the capacitance between the gate and source/drain.

This paper is organized as follows. Section II explains the SPICE model used for InSb circuit simulation. Logic circuit analysis is discussed in Section III. Section IV compares memory circuits in silicon and InSb technology. Possible application space of InSb QWFETs is discussed in Section V. Section VI concludes this paper with InSb technology requirements.

II. Device/Spice Models

The QWFET structure consists of narrowband InSb quantum well sandwiched between wider bandgap $\mathrm{Al}_X\mathrm{In}_{1-X}\mathrm{Sb}$ barrier layers. Barrier layers achieve 1) carrier confinement in the quantum well and 2) reduced junction/transistor OFF-state leakage [10]. Band-to-band tunneling in these narrow bandgap semiconductors is reduced by lowering the drain side electric field in the quantum well by optimizing the barrier thickness [11]. Modulation doping in AlInSb barrier region is achieved with Te δ-doped donor layer [8].

SPICE compatible models are generated using heterostructure FET physics (HFET) [12]. SPICE model includes Schottky diodes D_1 and D_2 to model Metal/AlInSb/InSb structure, as shown in Fig. 3. Bias dependent G–S/D capacitance due to Schottky diodes is also included in the model. Various physical mechanisms related to small geometries and high electric fields are taken into account in the SPICE model [12]. Heterostructure interface at the S/D contacts are modeled as S/D series resistance. The source/drain parasitic resistance $(R_{\rm SD})$ is significant due to Gate–S/D separation $(L_{\rm SD} = 0.75\ \mu\mathrm{m})$. In addition, we incorporate the effects of electron transfer into the barrier layer separating the InSb quantum well from the gate [12].

A. I–V Model

The drain current $(I_{\rm ds})$ is given by

$$I_{\rm ds} = \frac{g_{\rm ch} V_{\rm ds}(1+\lambda V_{\rm ds})}{\left[1+\left(\frac{V_{\rm ds}}{V_{\rm sat}}\right)^m\right]^{1/m}}$$

where

- $g_{\rm ch}$ channel conductance including S/D resistance;
- $V_{\rm ds}$ drain-to-source voltage;
- $V_{\rm sat}$ saturation drain voltage;
- λ parameter describing the finite output conductance in the saturation region;
- m parameter that determines the shape of the $I_{\rm ds}$–$V_{\rm ds}$ characteristics in the knee region.

The channel conductance $(g_{\rm ch})$ which includes source and drain resistance (R_S/R_D) is given by

$$g_{\rm ch} = \frac{g_{\rm chi}}{1+g_{\rm chi}(R_S+R_D)}$$

where $g_{\rm chi}$ is the intrinsic channel conductance given by

$$g_{\rm chi} = \frac{q n_{\rm stot} W \mu}{L}$$

where

- q electronic charge;
- $n_{\rm stot}$ total electron sheet density at the surface;
- W width of the device;
- L channel length;
- μ low field mobility.

HFET transport characteristics are affected by the limitation of carrier sheet density in the quantum well due to the energy band discontinuity at heterostructure interface. At large $V_{\rm GS}$, the electron quasi-Fermi level inside wide bandgap layer approaches the bottom of the conduction band. This causes significant transfer of electrons into the wide gap barrier layer. If barrier layer has defects present, these electrons can get trapped and may not contribute to the current flow. Hence, at higher gate bias, the sheet carrier density $(n_{\rm stot})$ gets saturated. The maximum sheet carrier density $(\mathrm{n_{max}})$ typically achieved is $1-2\times10^{12}$ cm^{-2} [8], [13]. Thus, total electron sheet density $(n_{\rm stot})$ is given by

$$n_{\rm stot} = \frac{n_s'}{\left[1+\left(\frac{n_s'}{n_{\rm max}}\right)^\gamma\right]^{1/\gamma}}$$

where

- γ characteristic parameter for the transition to the saturation region;

n'_s sheet carrier density estimated by Unified Charge Control model [13].

It is calculated as

$$n'_s = 2n_0 \ln\left[1 + \frac{1}{2}\exp\left(\frac{V_{\rm GS} - V_T}{\eta V_{\rm th}}\right)\right]$$

where

n_0 sheet carrier density at threshold;
V_T threshold voltage;
η body effect parameter $= 1 + C_d/C_I$.

Gate current is modeled as diode current and given as

$$I_{\rm GS} = I_s\left[\exp(V_{\rm GS}/mV_{\rm th}) - 1\right]$$

I_S diode saturation current;
m ideality factor;
$V_{\rm th}$ thermal voltage.

B. C–V Model

The G/S and G/D capacitances are calculated using unified gate-channel capacitance with Meyer's capacitance model [14]

$$C_{\rm GS} = \frac{2}{3}C_{\rm ch}\left[1 - \left(\frac{V_{\rm GS} - V_T - V_{\rm DSe}}{2(V_{\rm GS} - V_T) - V_{\rm DSe}}\right)^2\right]$$

$$C_{\rm GD} = \frac{2}{3}C_{\rm ch}\left[1 - \left(\frac{V_{\rm GS} - V_T}{2(V_{\rm GS} - V_T) - V_{\rm DSe}}\right)^2\right]$$

$$V_{\rm DSe} = V_{\rm DS}, \qquad \text{for } V_{\rm DS} < V_{\rm GS} - V_T$$
$$= (V_{\rm GS} - V_T), \qquad \text{for } V_{\rm DS} > V_{\rm GS} - V_T.$$

The channel charge $C_{\rm ch}$ is given by

$$C_{\rm ch} = WLq\frac{dn_s}{dV_{\rm GS}} \approx \frac{C'_{\rm ch}}{[1 + (n'_s/n_{\max})^\gamma]^{1/\gamma}}$$

where $C'_{\rm ch}$ = channel charge without sheet carrier density saturation.

$$C'_{\rm ch} = C_i\left[1 + 2\exp\left(-\frac{(V_{\rm GS} - V_T)}{\eta V_{\rm th}}\right)\right]^{-1}$$

where C_i = insulator capacitance given by

$$C_i = \frac{WL\varepsilon_i}{d_i}$$

ε_i and d_i are the permittivity and the thickness of the wide bandgap barrier layer, respectively. The SPICE simulated $I_{\rm DS}$–$V_{\rm DS}$ and $I_{\rm DS}$–$V_{\rm GS}$ characteristics for an enhancement mode (e-mode) InSb NFET are matched with the experimental data (Figs. 4 and 5). SPICE simulation shows 3% error in ON current compared to the experimental data. For the depletion mode devices (due to unavailability of published data), SPICE parameters are kept the same as the enhancement device except the threshold voltage.

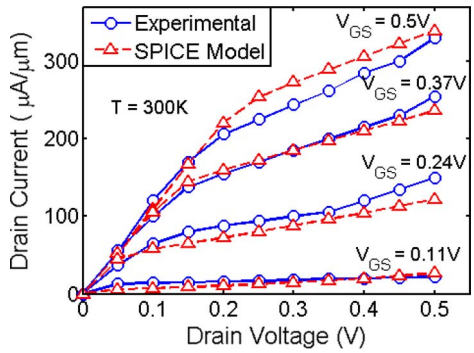

Fig. 4. Enhancement mode 85-nm InSb QWFET I_D–V_D characteristics: SPICE versus experimental data [8].

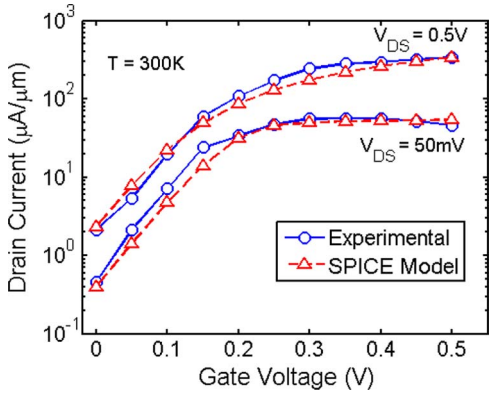

Fig. 5. Enhancement mode 85-nm InSb QWFET I_D–V_G characteristics: SPICE versus experimental data [8] for $V_{\rm DS} = 50$ mV and $V_{\rm DS} = 0.5$ V.

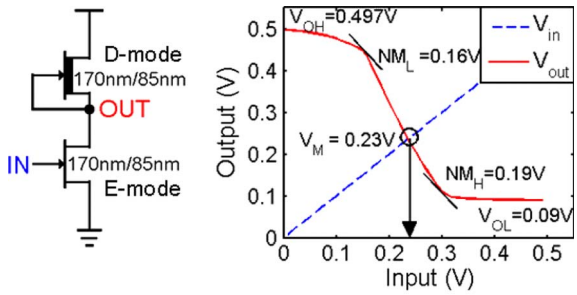

Fig. 6. DCFL: (a) Inverter structure is formed using depletion mode (d-mode) transistor as load device, while enhancement mode (e-mode) transistor acts as driver device. (b) Inverter input–output characteristics, output high voltage ($V_{\rm OH} = 0.497$ V), output low voltage ($V_{\rm OL} = 0.09$ V), switching threshold ($V_M = 0.23$ V), low-noise margin ($\rm NM_L = 0.16$ V), and high-noise margin ($\rm NM_H = 0.19$ V) are indicated. Output voltage swing is reduced due to static current consumption resulting in degraded noise margin.

III. Logic Circuit Analysis

A. InSb Inverter Analysis

Hole mobility in InSb is small compared to electron mobility. As a result, high-speed logic circuits using complementary InSb FETs is difficult to achieve. Hence, logic styles based on NFETs are implemented for high-speed design using direct-coupled FET logic (DCFL) [15]. Fig. 6 shows inverter schematics using DCFL. Depletion mode QWFET (d-mode) is used as resistive load. Gate and source nodes of the d-mode QWFET

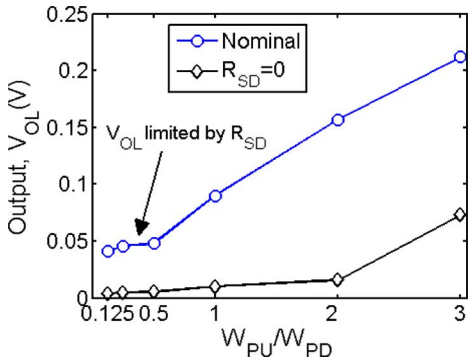

Fig. 7. Effect of series resistance ($R_{\rm SD}$) on output low voltage ($V_{\rm OL}$): Higher series resistance limits the low output voltage even if width of pull up device ($W_{\rm PU}$) is smaller than the width of pull down device ($W_{\rm PD}$). Nominal case refers to the experimental data [8]. In ideal case ($R_{\rm SD} = 0\ \Omega$), $V_{\rm OL}$ significantly reduces with pull up size reduction.

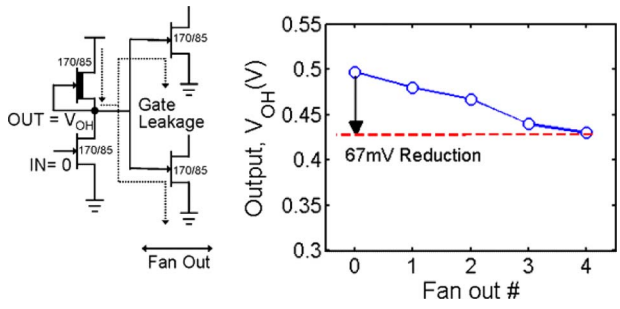

Fig. 8. Effect of fan-out on high output voltage ($V_{\rm OH}$): Increasing fan-out results in $V_{\rm OH}$ degradation. Increased gate leakage current is supplied by the load device of the previous stage. Higher fan-out may affect the functionality of a logic gate. Gate dielectric would reduce the gate leakage as well as improve the input–output isolation.

are connected together. Enhancement mode (e-mode) QWFET is used as the driver transistor. Fig. 6 shows the voltage transfer characteristics for minimum-sized inverter ($W = 2^{*}L_{\rm min}$, $L_{\rm min} = 85$ nm). When input gate voltage is logic "1," the output voltage is determined by the ratio of the drive strengths of load device and driver device. The logic family is said to be "*ratio-ed*." Hence, output low voltage ($V_{\rm OL}$) is not zero, and the output voltage transition is not rail to rail. This results in degraded noise margins. As shown in Fig. 6, the low-noise margin ($\rm NM_{\it L}$) is lower than the high-noise margin ($\rm NM_{\it H}$).

Parasitic S/D resistance plays a significant role in determining low output voltage ($V_{\rm OL}$). Reducing the size of load device should result in lower $V_{\rm OL}$. However, it is found that $R_{\rm S/D}$ limits output voltage, and $V_{\rm OL}$ does not reduce even if the load device is weaker than the driver device (Fig. 7). SPICE simulations with $R_{\rm S/D} = 0\ \Omega$ (ideal case) show that $V_{\rm OL}$ significantly reduces with reducing S/D resistance, as shown in Fig. 7. Hence minimization of S/D resistance is important for successful deployment of InSb QWFETs in logic circuits. Typically, the heterostructure interface at quantum-well/SD contact and the separation between the gate and S/D contacts results in higher $R_{\rm S/D}$.

Due to the absence of good quality gate dielectric, G/S and G/D diodes cause significant gate leakage current [16]. Fig. 8 shows the effect of increasing fan-out on output high voltage ($V_{\rm OH}$). With increasing fan-out, the input gate leakage current increases, which is supplied by the load device (d-mode QWFET) of the previous stage circuit. Increased fan-out results in $V_{\rm OH}$ degradation and leads to functional failures. Hence, gate leakage should be reduced for power reduction as well as to achieve better input–output isolation (for correct logic functionality).

B. Comparison With Silicon Technology

For performance, 85-nm InSb QWFET technology is compared with 90-nm Si MOSFET technology. Predictive technology models are used for 90-nm silicon technology [17], [18]. Since InSb QWFET shows higher ON current as well as higher OFF current compared to the standard Si MOSFETs, it is worthwhile to compare ON current improvement in InSb devices under identical OFF-state current condition. OFF-state current in 90-nm Si NMOS is matched with 90-nm InSb e-mode QWFET ($I_{\rm OFF} \approx 1\ \mu{\rm A}/\mu{\rm m}$, $V_{\rm DS} = 0.5$ V) by reducing the threshold voltage of Si NMOSFET. Fig. 9 shows I_D–V_G characteristics of 90-nm InSb QWFET and 85-nm Si MOSFET under identical OFF-state current condition. It is observed that lower V_T Si NMOS marginally gives higher ON current than the present 85-nm InSb QWFET. Higher S/D resistance limits the ON current in InSb devices. If S/D resistance is reduced (ideal case being $R_{\rm S/D} = 0$), then ON current in InSb QWFET is 40% higher than the corresponding Si MOSFET (At iso-$I_{\rm OFF}$ condition). This analysis indicates that InSb QWFETs with reduced S/D resistance can possibly result in higher speed computation units compared to low-V_T Si MOSFETs.

C. Effect of S/D Resistance

As the QWFET fabrication process becomes mature, the S/D resistance would be reduced. In such case, it would be useful to evaluate the ON current improvement in InSb devices for different S/D resistance. Fig. 10 shows variation of circuit parameters as a function of percentage reduction in S/D resistance. It is observed that ideal case ON current (with $R_{\rm S/D} = 0\ \Omega$) is 77% higher than the present experimental device.

The nine-stage ring oscillator circuit built using minimum-sized DCFL inverters gives 67% improvement in the ring oscillator frequency compared to the present experimental device. Further, the power delay product (PDP) reduces by 10%, and energy delay product (EDP) by 46% compared to the present experimental device [as shown in Fig. 10(b)]. Fig. 11 shows normalized circuit metrics for 90-nm Si NMOS and 85-nm InSb QWFET under iso-$I_{\rm OFF}$ condition. It is observed that low-V_T Si NMOS marginally gives higher ON current compared to present 85-nm InSb QWFET. However, ring oscillator (nine stages) frequency in InSb devices is higher than Si NMOS due to lower gate capacitance present at the intermediate nodes of the ring oscillator. If S/D resistance in InSb devices is reduced by 50% (for example), it results in 14% higher ON current than Si NMOS. This leads to 12.3X better ring oscillator frequency and consequently 12X reduction in EDP. However, due to higher static leakage current in DCFL, the power consumption is higher in InSb DCFL logic resulting in PDP comparable to Si NMOS. The PDP indicates the amount of energy consumed in

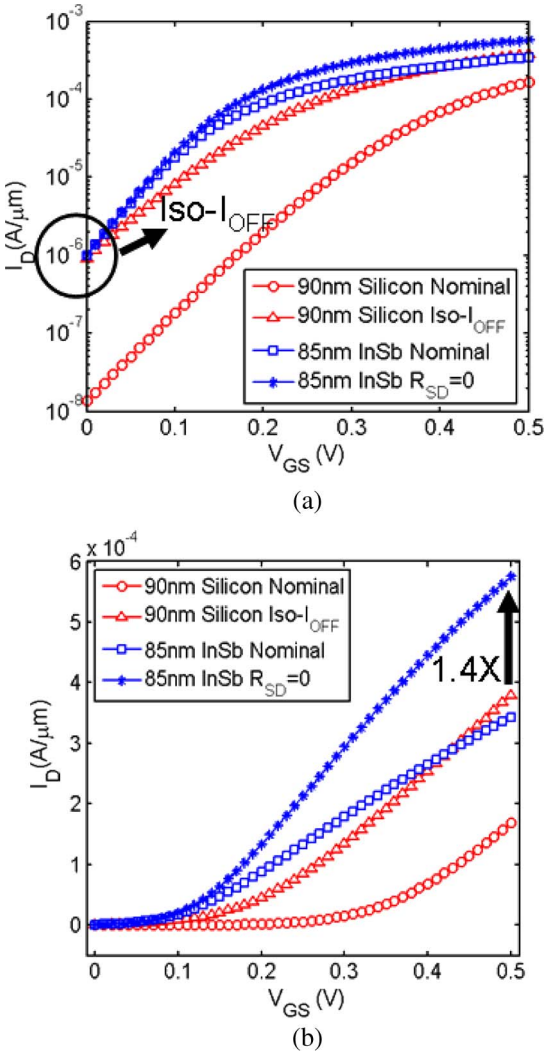

Fig. 9. The 90-nm silicon MOSFET versus 85-nm InSb QWFET I_D–V_G characteristics [8], [18]. (a) Log scale. (b) Linear scale. The 90-nm nominal threshold voltage (V_T) Si MOSFET shows lower OFF-state current compared to 85-nm InSb QWFET. Threshold voltage of Si-MOSFT is reduced, to match the OFF-state current the same as that of InSb QWFET. At Iso-OFF current, low-V_T Si MOSFET marginally gives higher ON current compared to present InSb QWFET. Reduced series resistance in InSb QWFET gives much higher ON current compared to low-V_T Si MOSFET.

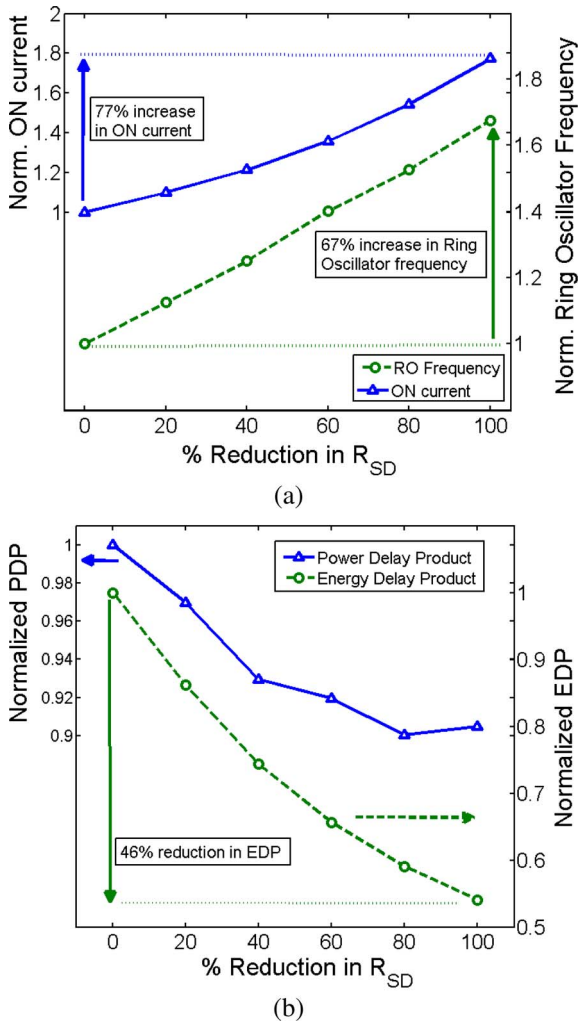

Fig. 10. Circuit parameter variation with series resistance. (a) ON current and ring-oscillator-frequency variation. (b) PDP and EDP variation. The percentage reduction is based on the S/D resistance in experimental 85-nm InSb QWFET [8].

logic computation. Thus, 85-nm InSb DCFL (with 50% reduced $R_{S/D}$) shows ~12X faster computation compared to 90-nm Si CMOS (operating at $V_{DD} = 0.5$ V) for the same energy consumption. Moreover, for a 4-b ripple carry adder, the carry propagation delay is reduced by 5X in InSb DCFL adder, as shown in Fig. 11.

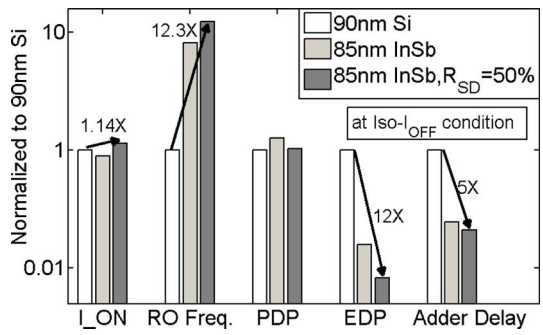

Fig. 11. Circuit metrics comparison of 90-nm silicon NMOS and 85-nm InSb e-mode QWFET: InSb QWFET with reduced $R_{S/D}$ results in 14% higher ON current, 12.3X higher ring oscillator frequency, ~12X lower EDP compared to silicon NMOS at iso-OFF current condition. Carry propagation delay of a 4-b ripple carry adder is reduced by 5X using InSb QWFETs.

D. Si + InSb Hybrid Logic Technology

As DCFL incurs significant static leakage current and lower noise margins, we believe that hybrid technology consisting of InSb NFET + Si PMOS can be used along with the standard Si CMOS technology. Fig. 12 shows the inverter schematics using Si CMOS, InSb DCFL, and Si + InSb hybrid technology. Use of Si PMOS reduces the static leakage and results in complementary logic style. Use of InSb devices would give better performance than "dual V_T" Si MOSFET approach [19]. In a Dual V_T design, low-V_T transistors are used in the critical paths to improve the performance, while high-V_T transistors are used in noncritical paths to reduce the leakage current [19]. Si + InSb CMOS can be used in *critical paths* while Si CMOS in noncritical paths [Fig. 13(a)]. InSb QWFETs can

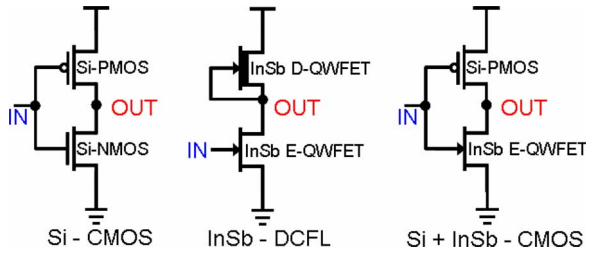

Fig. 12. Inverter design in (a) Si-CMOS, (b) InSb-DCFL, and (c) proposed complementary Si + InSb hybrid technology.

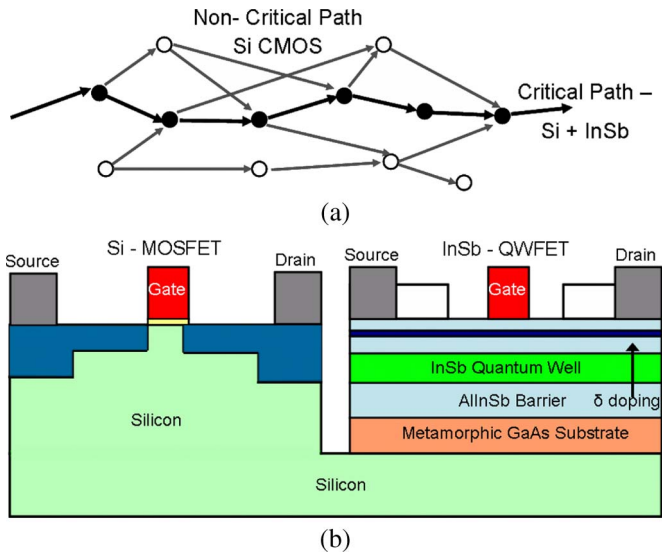

Fig. 13. Si + InSb hybrid technology integration. (a) InSb NFET + Si PMOS hybrid complementary logic can be used in critical paths for better performance while Si-CMOS with lower leakage current can be used in noncritical paths. (b) Si + InSb "hybrid technology" on single silicon substrate [20].

be integrated with Si MOSFETs on a single Si substrate [20]. Fig. 13(b) shows the cross section of Si + InSb devices on single Si wafer. Similar integration of InGaAs-based devices on silicon substrate has been demonstrated [21]. Fig. 14 shows the comparison of circuit metrics for Si CMOS and Si + InSb hybrid technology ($R_{S/D} = 50\%$ of the present experimental device $R_{S/D}$). Si + InSb hybrid technology gives 14% higher ring oscillator frequency with 17% lower EDP. The carry propagation delay for Si + InSb adder is 15% lower than Si CMOS-based adder. Thus hybrid Si+ InSb technology can give better performance than Si CMOS at iso-I_{OFF} condition.

IV. Memory Circuit Analysis

A. 6T Bitcell Analysis

Embedded cache memories are expected to occupy 90% of the total die area of a system on a chip [22]. We also evaluated InSb QWFETs for possible use in memory applications. 6T SRAM bitcells in Si and InSb technology are compared for stability and leakage. InSb 6T SRAM bitcell is formed using cross-coupled DCFL inverter pair, as shown in Fig. 15. This results in static current consumption in the branch storing "0" (i.e., node voltage is V_{OL}). Static noise margin (SNM) is evaluated for comparing the SRAM bitcell stability. SNM is

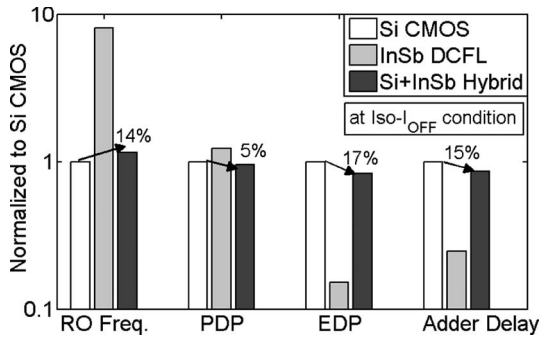

Fig. 14. Silicon CMOS and Si + InSb hybrid technology comparison: Si + InSb gives 14% higher ring oscillator frequency with 17% reduction in EDP. The carry propagation delay in a 4-b adder is reduced by 15%. At iso-OFF current, Si + InSb can give better performance compared to dual V_T Si CMOS.

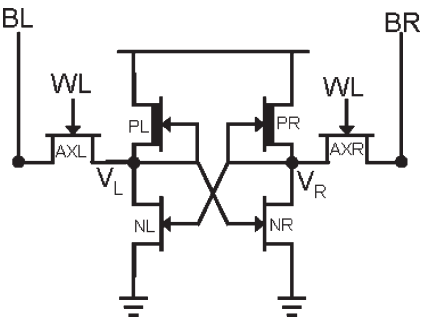

Fig. 15. Six transistor InSb QWFET-based DCFL SRAM bitcell: Cross-coupled DCFL inverters are formed with PL–NL and PR–NR transistors. Read and write operation to the memory cell is controlled by wordline signal (WL) and bitline signals (BL and BR) connected to the e-mode access transistors (AXL and AXR).

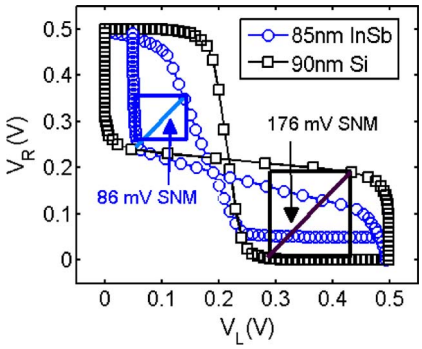

Fig. 16. Si versus InSb technology hold SNM comparison: SNM is graphically estimated as the length of a side of the largest square that can be embedded inside the lobes of the transfer characteristics [23]. V_L and V_R represent the storage node voltages. Due to higher series resistance and nonzero V_{OL} hold SNM in InSb bitcell is 86 mV compared to 176 mV in Si bitcell.

graphically estimated as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [23].

Due to higher $R_{S/D}$ and ratio-ed logic family, InSb SRAM bitcell shows lower SNM compared to Si SRAM bitcell. At 0.5-V V_{DD}, InSb bitcell shows read SNM of 10 mV compared to 86 mV read SNM in 6T Si bitcell. Reducing $R_{S/D} = 0\ \Omega$ improves read SNM to 18 mV indicating marginal improvement in InSb SRAM read stability. For the hold case, InSb bitcell shows 86-mV hold SNM compared to 176 mV in Si bitcell (2X reduced hold SNM), as shown in Fig. 16. Reducing S/D resistance helps in improving the hold SNM. Reducing

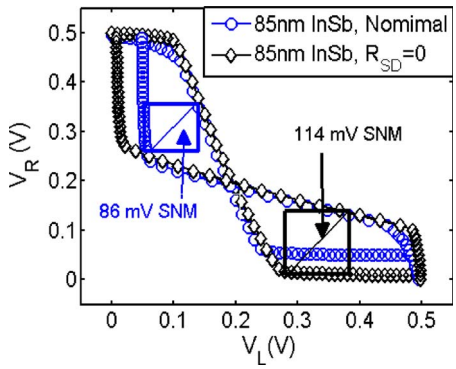

Fig. 17. Effect of series resistance on hold SNM in InSb SRAM cell: Reducing the series resistance improves hold SNM by 35% in InSb bitcell. Nominal case refers to 85-nm experimental data [8].

$R_{S/D} = 0\ \Omega$ in InSb device, results in 114-mV hold SNM which is 1.3X better compared to the present experimental InSb device (Fig. 17). Due to Schottky diode (G-S/D) leakage and ratio-ed logic family InSb bitcell incurs much higher leakage ($\sim$2 orders of higher magnitude) compared to Si bitcell. Sleep transistors are found effective in reducing InSb bitcell leakage by $\sim$5X.

In summary, 6T silicon bitcell gives better cell stability as well as reduced cell leakage compared to InSb-based DCFL bitcell. For high-density memory applications, bitcell area, cell stability, and cell leakage are important criteria for robust low-voltage operation. For such cases, InSb QWFETs may find limited use in high-density low-voltage SRAMs such as Level 2(L2) and/or Level 3 (L3) caches.

B. 8T Bitcell Analysis

For Level 1 (L1) data cache, access-time is an important metric which has direct implications on the processor execution time and, hence, the clock speed. In such timing critical applications, higher ON current in InSb devices can be utilized for faster bitline discharge by employing an InSb read buffer in an 8T bitcell [24] (also called as register file cell) [Fig. 18(a)]. Transistors N1 and N2 form the read buffer (read port). The stability of the proposed Si + InSb hybrid 8T bitcell is determined by the cross-coupled inverter pair formed using standard Si MOSFETs. Fig. 18(b) shows the "Thin-cell" layout of the proposed hybrid 8T bitcell employing InSb NFET based read buffer [25]. As InSb QWFET fabrication follows traditional "top-down" patterning approach, the proposed hybrid Si + InSb 8T bitcell fabrication can be compatible with the present Silicon technology. Fig. 19 shows L1 cache schematics utilizing the 8T Si + InSb hybrid bitcell. InSb QWFETs are used as read port transistors of an 8T hybrid bitcell. The access transistors in cross-coupled inverter pair are omitted for the clarity. The local bitline (LBL) is precharged to V_{DD} using a clock signal (Clock = 0). During the evaluation phase (Clock = 1), one of the read word line (RWL) turns ON, and LBL gets discharged if stored data (D) is "1." Keeper PMOS is a weak device which tries to pull up the LBL node to prevent unintentional LBL collapse due to leakage and/or noise. Global bitline is then evaluated depending on the LBL evaluation. Si + InSb hybrid 8T bitcell gives 18% lower LBL evaluation time (C_{BL} = 300 fF, $V_{DD} = 0.5$ V). Furthermore, with reduced $R_{S/D}$, LBL evaluation delay reduces by 60%, as shown in Fig. 20(a). Due to higher speed of operation, the proposed Si + InSb hybrid 8T bitcell shows 27% lower PDP compared to 8T Si bitcell [Fig. 20(b)]. During the standby mode, the leakage current in the memory blocks can significantly be reduced using sleep transistor [2]. The sleep transistor technique can be applied to Si as well as hybridSi + InSb cell. Thus, InSb transistors would be useful in high-speed L1 caches. This would result in faster memory (L1 cache) accesses and would improve the processor clock speed.

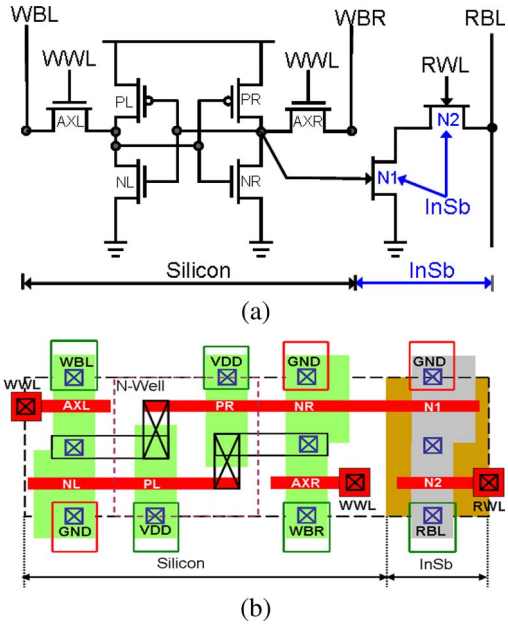

Fig. 18. Si + InSb hybrid 8T SRAM bitcell: (a) Cell stability is governed by the cross-coupled inverter pair formed using contemporary silicon MOSFETs. The read port (N1 and N2) is formed using e-mode InSb QWFETs giving improved bitline sensing speed. (b) 8T hybrid Si + InSb "Thin-cell" layout: InSb QWFETs follow traditional top-down patterning approach and, hence, can be integrated with the present silicon MOSFET technology.

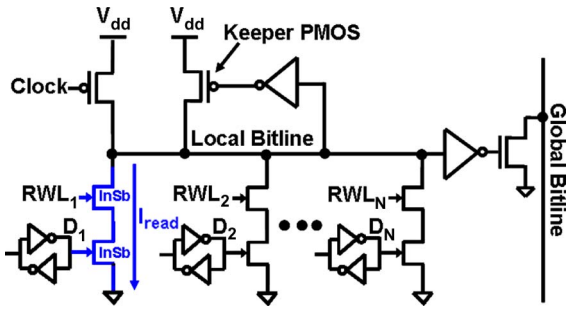

Fig. 19. L1 cache memory schematics employing 8T Si + InSb hybrid bitcell.

V. Application Space of InSb QWFETs

Addition of gate dielectric and minimization of S/D resistance would be beneficial for the scalability of ultra-fast InSb QWFETs. Due to the absence of good P-type FET, high-speed rail-to-rail output CMOS logic family would be difficult to achieve using InSb QWFETs. Furthermore, higher leakage current and poor cell stability might limit the use of InSb devices in

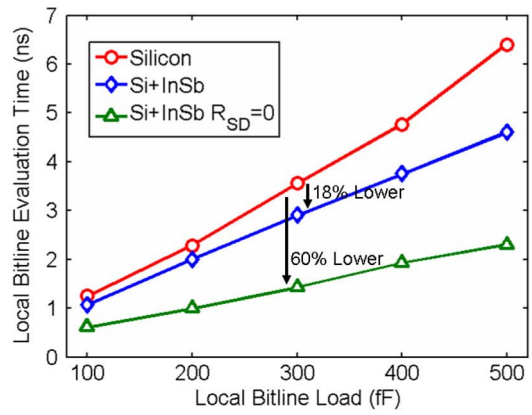

Fig. 20. LBL evaluation time comparison: Si + InSb hybrid 8T bitcell gives 18% lower LBL evaluation time with 27% lower PDP compared to silicon 8T bitcell ($C_{\rm BL} = 300$ fF, $V_{\rm DD} = 0.5$ V).

dense memory designs. High-speed N-type InSb QWFETs can be used as a supplement to the present Si CMOS technology. InSb QWFETs can be useful in performance critical datapath circuits operating at ultra low voltage. A circuit designer would choose either a low-V_T Si NMOS device or e-mode N-type InSb QWFET depending on the speed requirements. For high-speed memory design, InSb QWFETs can be useful in read port of a hydrid Si + InSb 8T SRAM bitcell for improved access time.

VI. Conclusion

We have shown the use of Si + InSb hybrid technology for high-speed logic and memory with a complete technology-circuit assessment. The codesign approach spans from the device/SPICE models to the logic and memory circuit analysis. We provide technology requirements for feasibility of InSb circuits viz., 1) gate insulator: for reducing Schottky diode leakage and better input–output isolation. 2) $L_{\rm SD}$ reduction and better heterostructure interface: for better $R_{\rm SD}$ to improve the speed and noise margins. 3) Reduced $I_{\rm OFF}$: for leakage power reduction. Furthermore, we suggest *the application space* of Si + InSb hybrid technology as 1) critical high performance datapath circuits, 2) high-speed L1 cache. However higher leakage would limit the use of standalone InSb devices in L2/L3 caches.

Appendix

The SPICE model parameters used to fit the experimental 85-nm InSb enhancement mode N-type QWFET characteristics are as follows. AIM-SPICE tool is used for the QWFET circuit simulation [12].

Sr. No.	SPICE Parameter	Parameter Description	Parameter Value
1	D_1	Distance to buffer layer charge	25E-9m
2	D_2	Distance from gate to second channel	25E-9m
3	EPS_I	Dielectric constant for interface layer	1.4E-10F/m
4	ETA	Subthreshold ideality factor	1.5
5	J_S	Forward bias saturation current	300E-9 A/m^2
6	LAMDA	Output conductance parameter	2.22/V
7	M	Knee shape parameter	8
8	MU	Low field mobility	1.8m^2/Vs
9	N_{MAX}	Maximum sheet charge density	1E16m^{-2}
10	R_D /R_S	Source/Drain resistance	450Ω
11	Vs	Saturation velocity	5e5m/s
12	V_{T0}	Threshold voltage	0.15V
13	Sigma0	DIBL parameter	0.1V/V

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