Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS

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Outline

- Introduction: 8T SRAM Array
- Proposed Low Swing (LS) Bitline Design
- Proposed Column Multiplexed (CM) Bitline Design
- Measurement Results
- Summary

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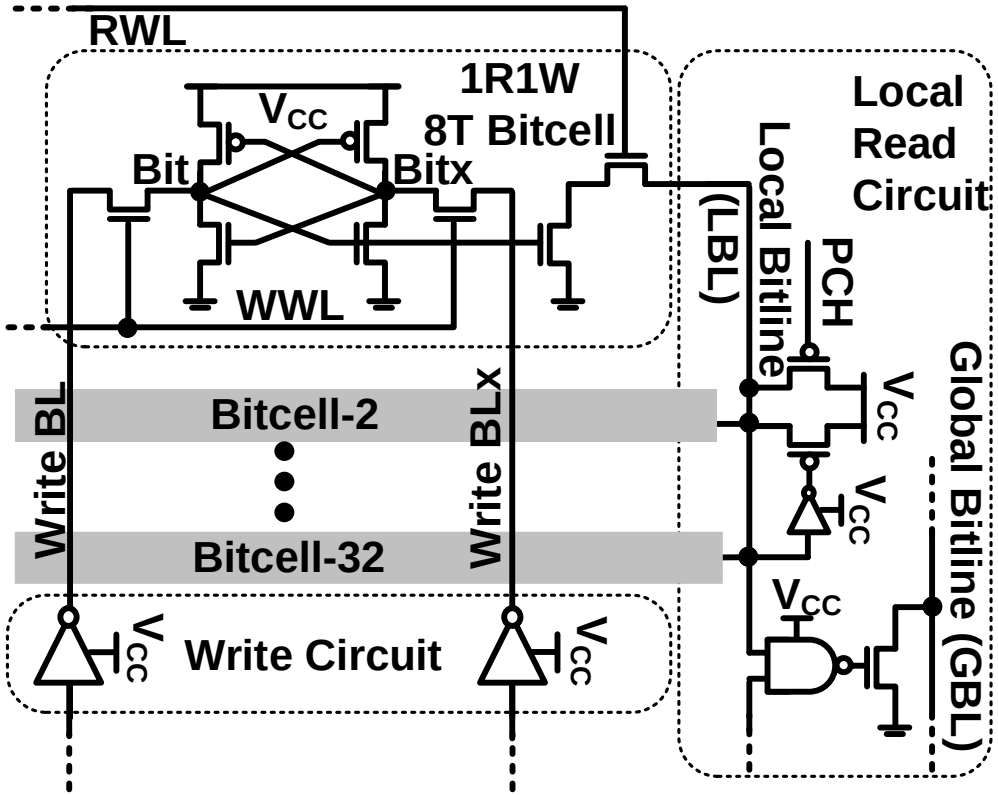
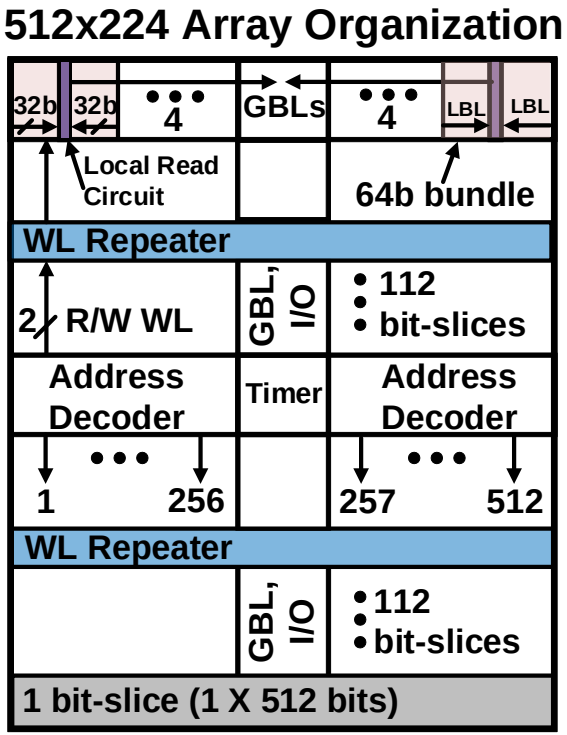
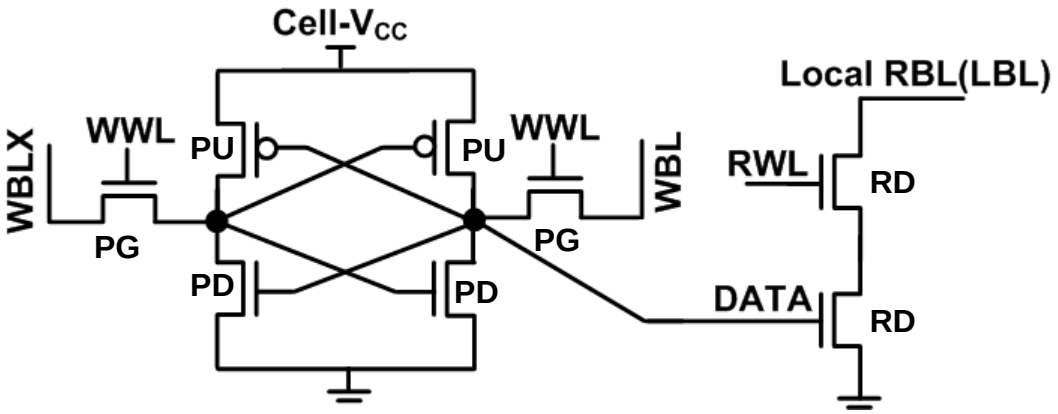
Introduction: 1R1W 8T SRAM Bitcell Array





- Decoupled read/write ports for lower Vmin (Register files, L1 caches)
- Hierarchical read bitlines for high performance design
- Large signal sensing limits no. of bits/LBL degrading bit-density

Review: High Density, Low Vmin 1R1W 8T SRAM

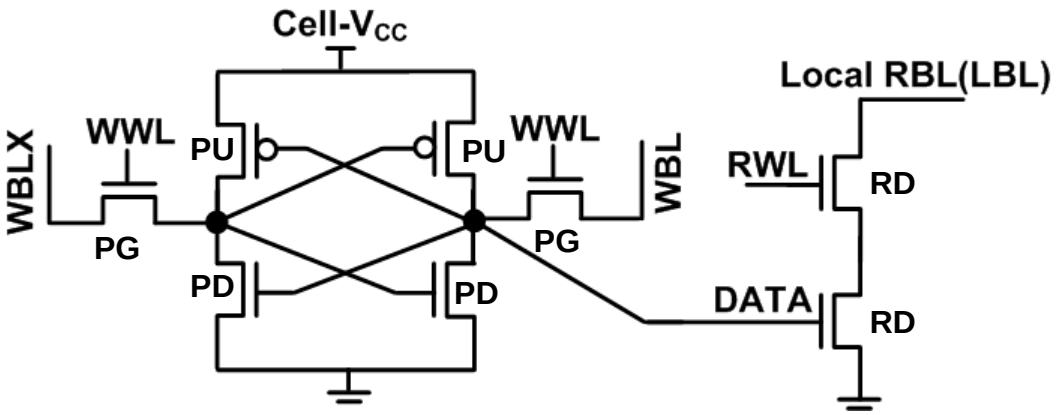


PU (Pull-Up) = 1Fin, PG (Pass-Gate) = 1Fin
PD (Pull-Down) = 1Fin, RD (Read Port) = 2Fins

Ref: K-H. Koo, VLSI Symposium 2015

- High Density 1-1-1-2-2 fin bitcell with 32b/LBL, Large signal sensing

Review: High Density, Low Vmin 1R1W 8T SRAM



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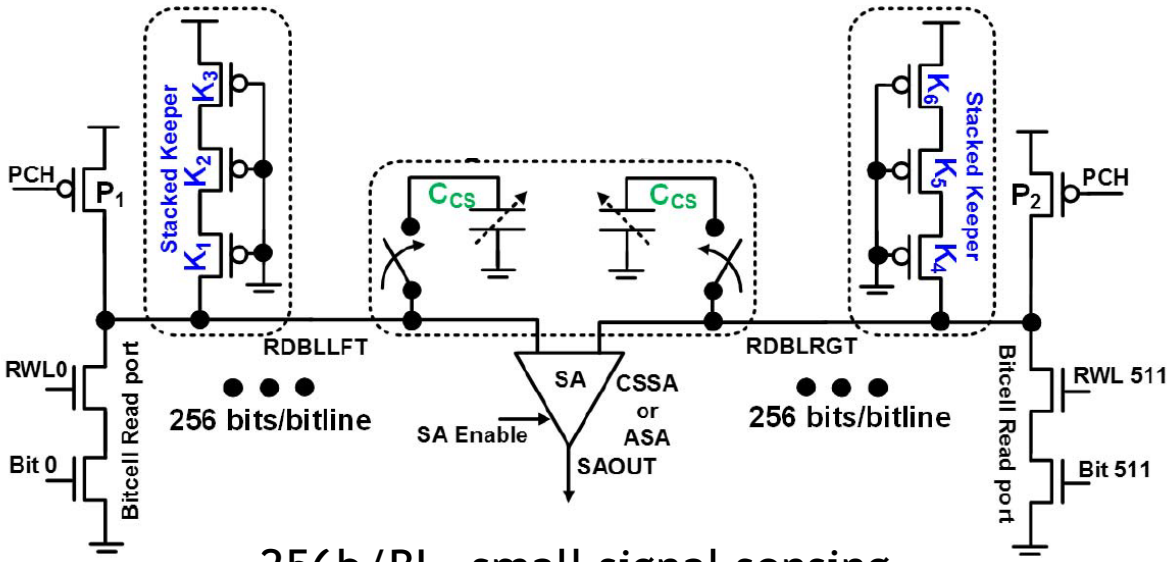

256b/BL, small signal sensing

Ref: J. Keane, ISSCC 2016, J. P. Kulkarni, JSSC, 2017

- High Density 1-1-1-2-2 fin bitcell with 32b/LBL, Large signal sensing
- Increasing array level bit density using charge share or asymmetric sense amplifier with 256b/BL at the expense of increased power

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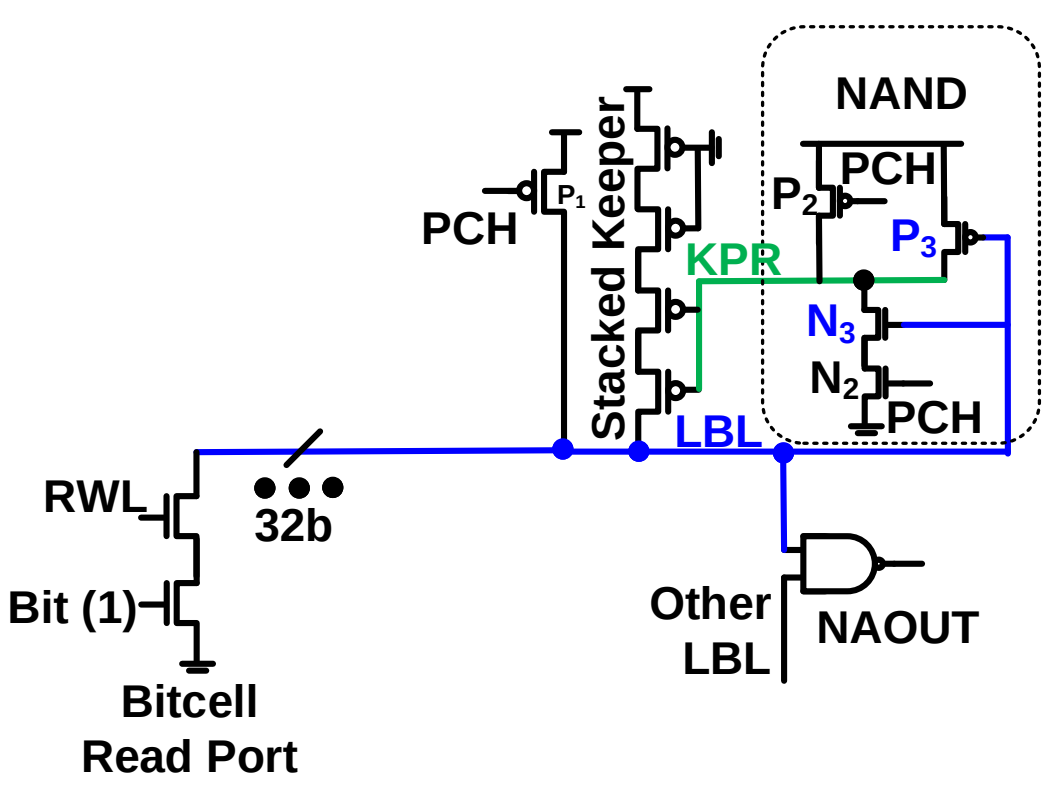
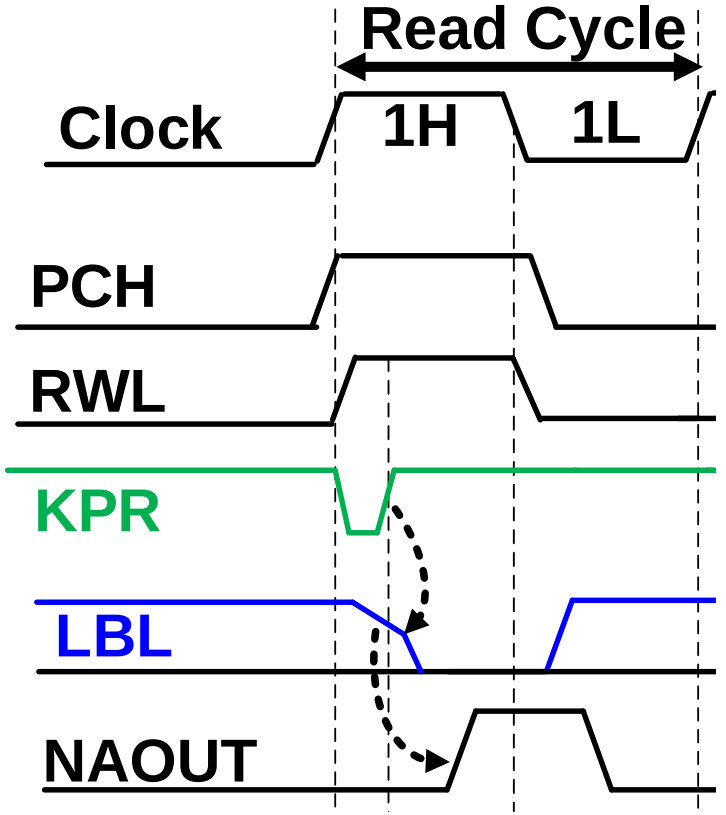
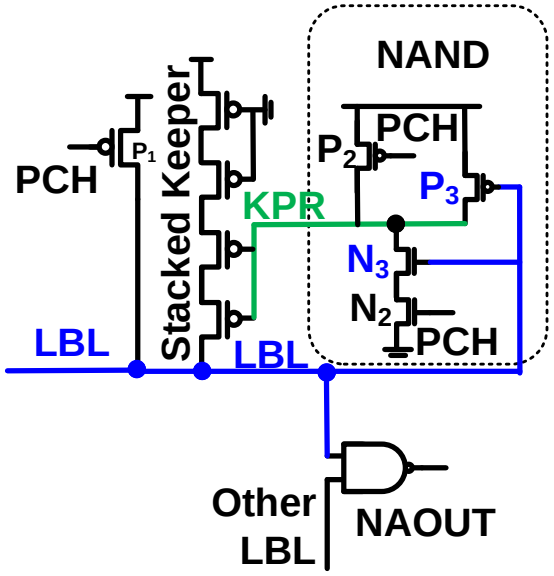
Baseline Design- Read Path Timing Diagram





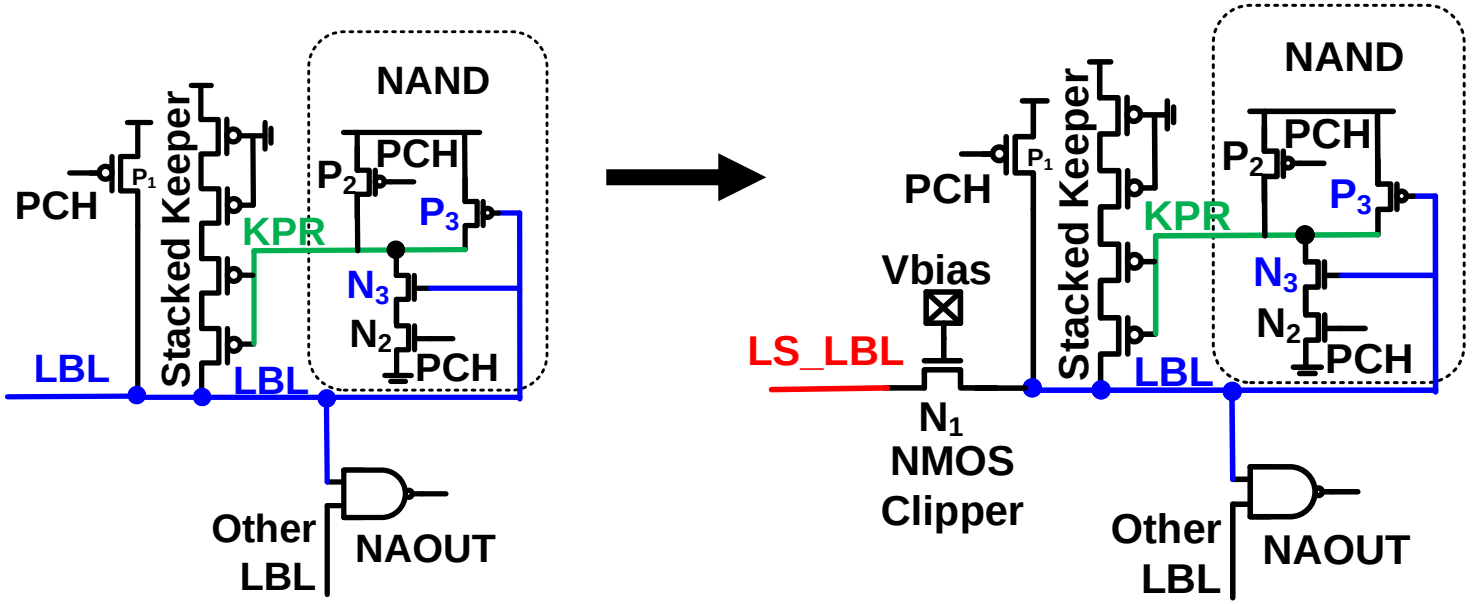
- Large signal, single ended sensing, 1 cycle domino read cycle
- NAND gate driven keeper stack turned OFF during precharge for aging

Low Swing Bitline Evolution



Baseline full swing LBL

Low Swing Bitline Evolution

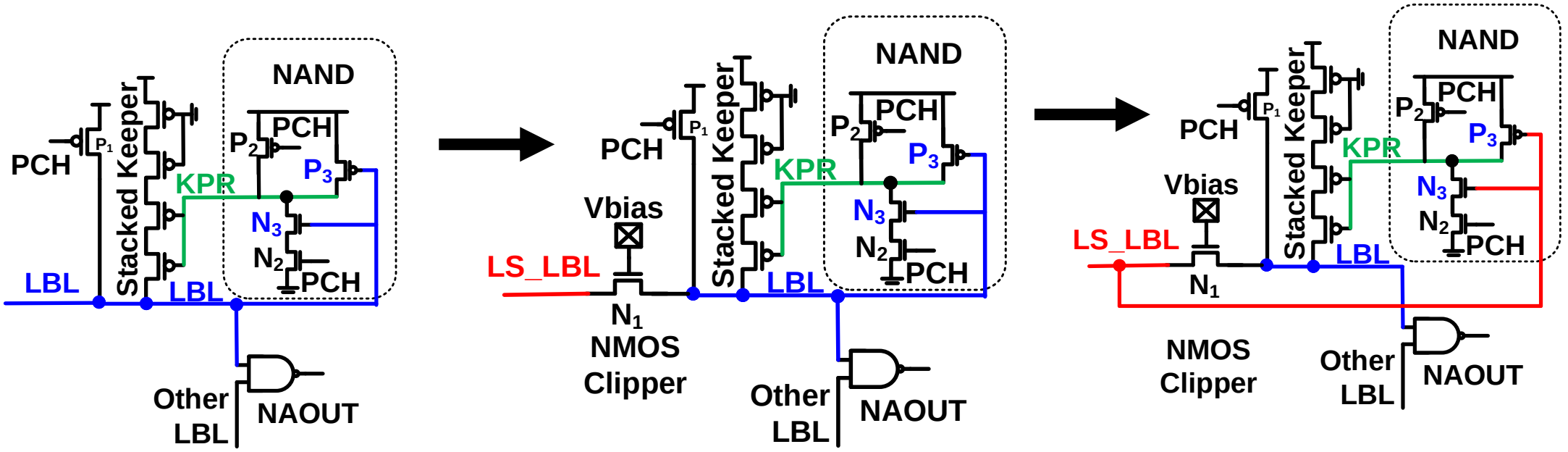


Baseline full swing LBL

Low Swing LBL with Clipper

- A series NMOS clipper (N_1) read path → LBL C_{DYN} reduction
- C_{DYN} reduction partially offsets delay degradation due to series clipper

Low Swing Bitline Evolution



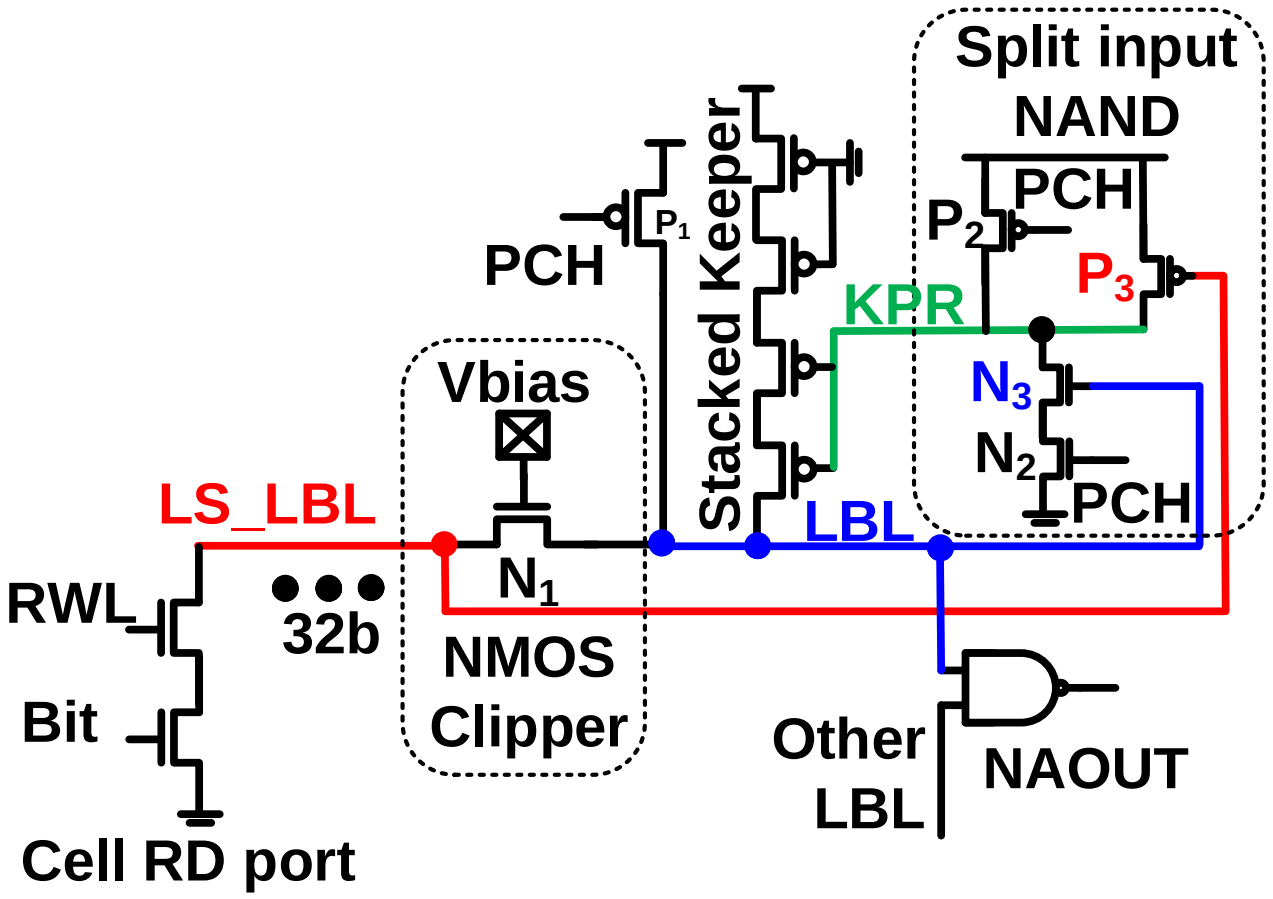
Baseline full swing LBL

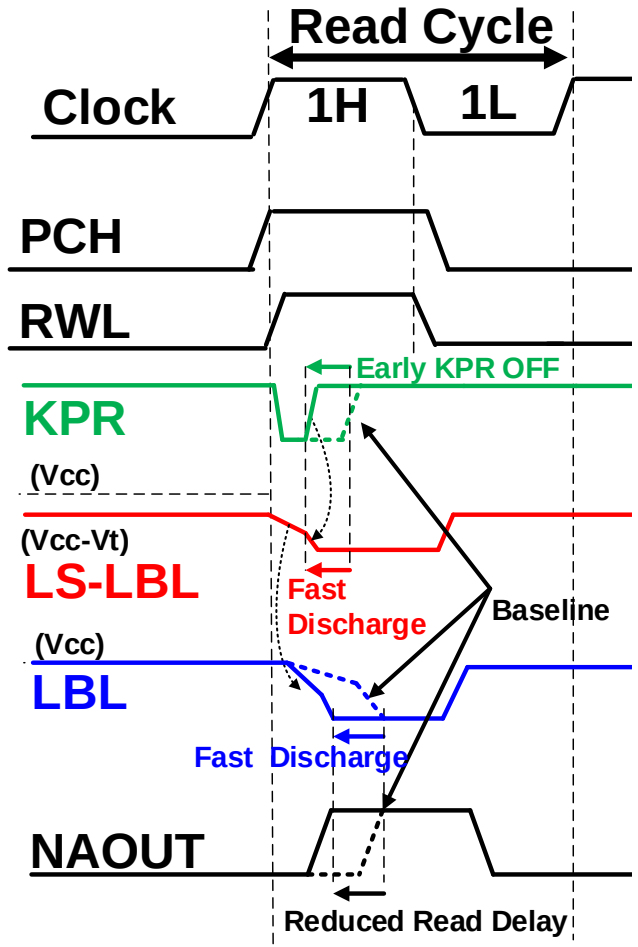
Low Swing LBL with Clipper

Low Swing LBL + Common NAND input

- A series NMOS clipper (N_1) read path → LBL C_{DYN} reduction
- C_{DYN} reduction partially offsets delay degradation due to series clipper
- If LS_LBL drives NAND, delay improves but reduced noise tolerance

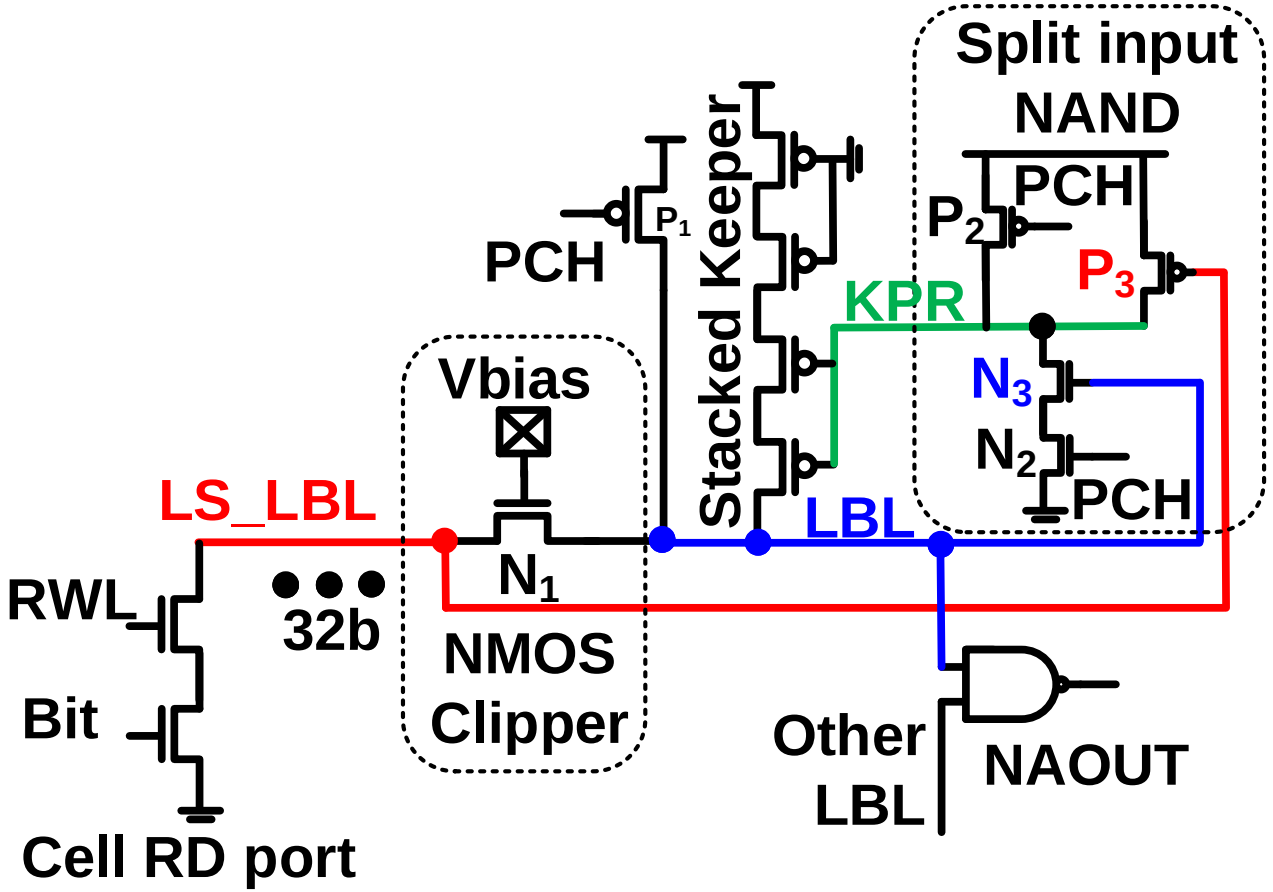
Low Swing Bitline with Split Input NAND Keeper-1/2





- NAND inputs for P3 and N3 are split for read delay vs. noise trade-off
- Low swing LBL node drives NAND PMOS (P_3) → Early keeper turn off

Low Swing Bitline with Split Input NAND Keeper-2/2



- Transient noise event: Clipper (N_1) in sub-threshold → shields LBL node
- Split input NAND with NMOS (N_3) strongly connected to full swing LBL

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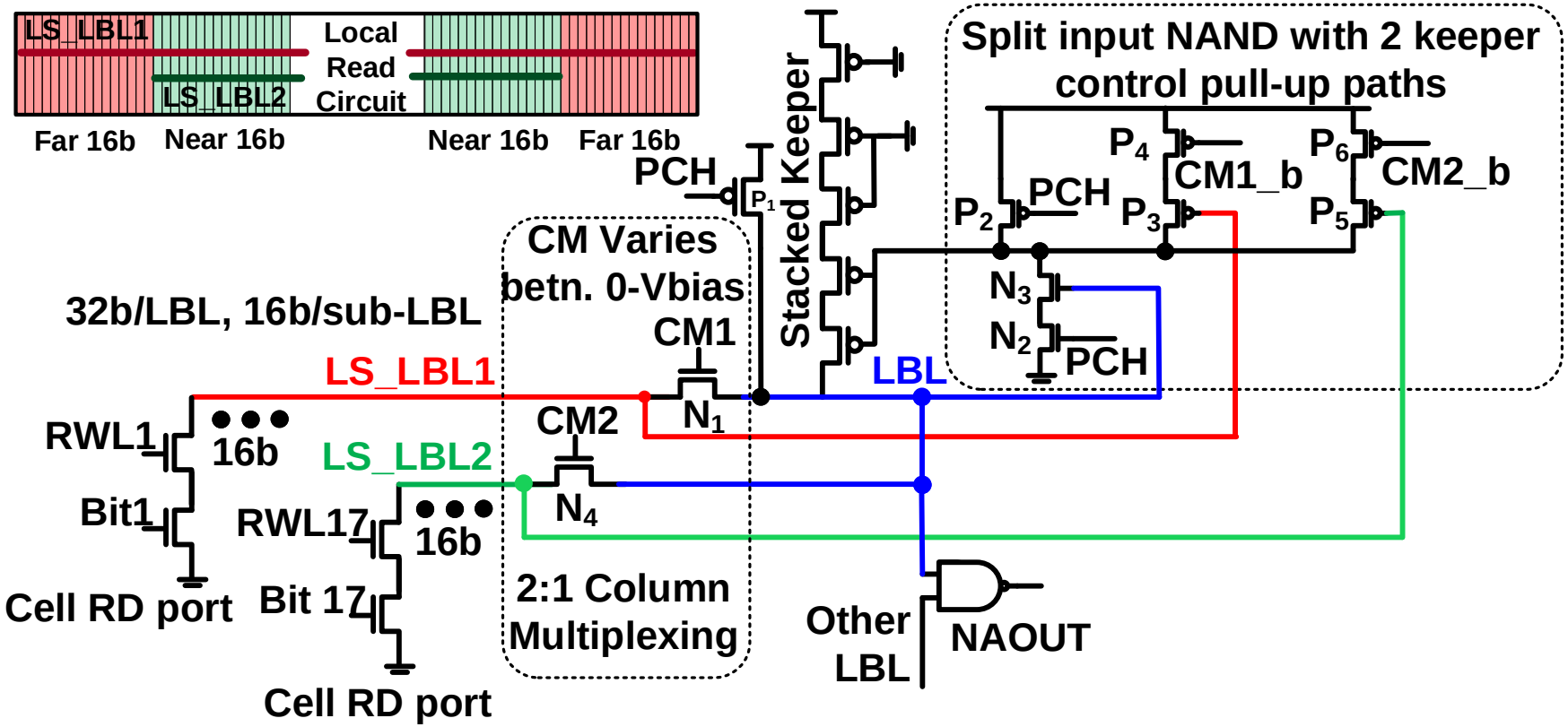
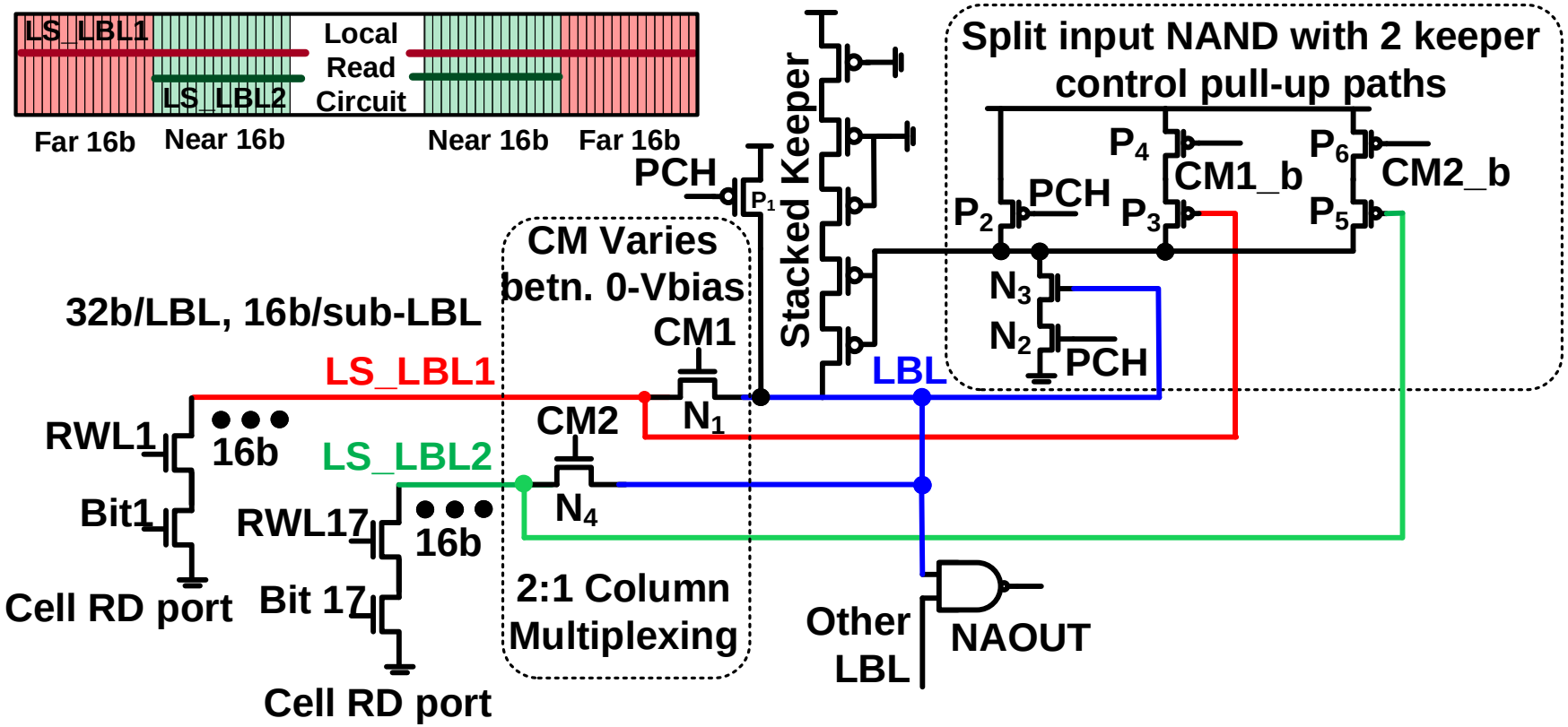
Column Multiplexed + Low Swing BL Technique-1/2



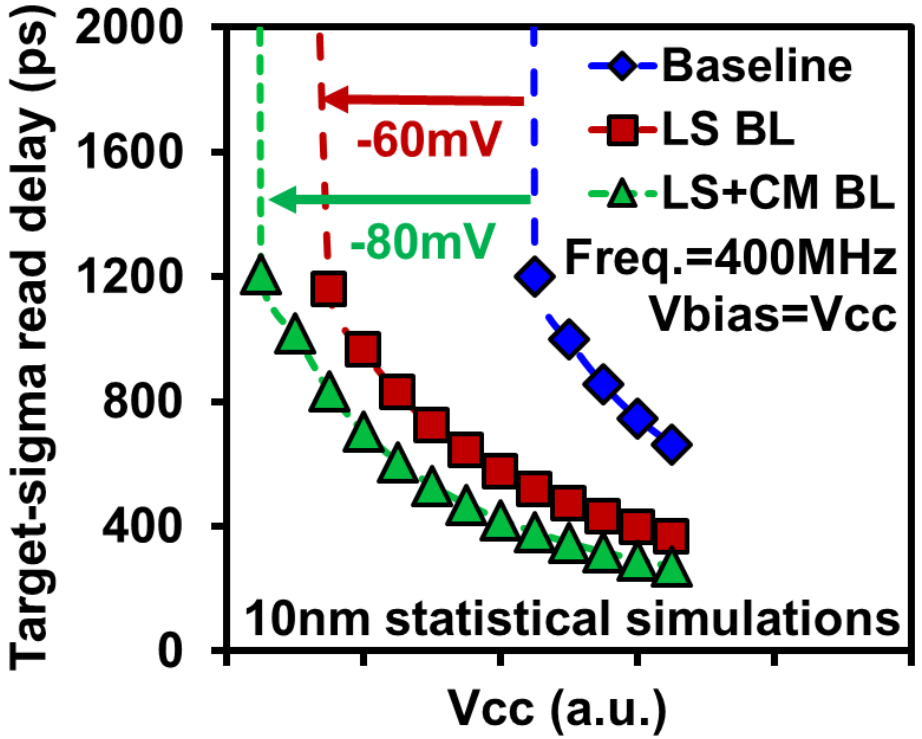
- Configuring statically biased clipper into a column multiplexer control
- Split input NAND with 2 keeper control pull-up paths
- Reduced C_{DYN} due to BL multiplexing + low swing operation

Column Multiplexed + Low Swing BL Technique-2/2



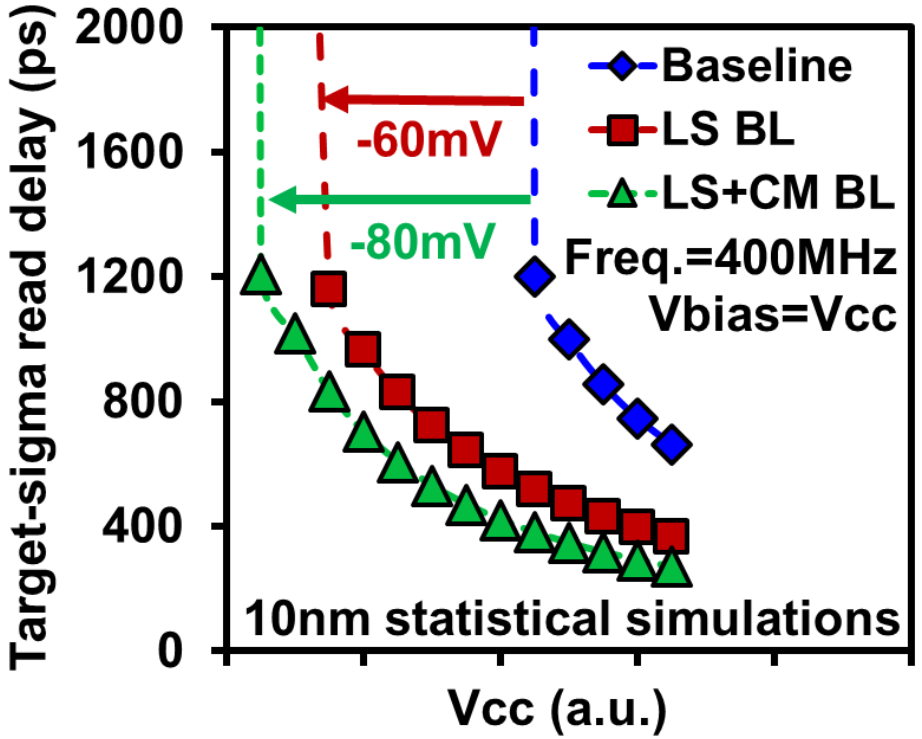
- Reduced bitline leakage due to stacking effect of inactive clipper
- Keeper can be downsized due to reduced BL leakage → lower Vmin
- Vmin, C_{DYN} savings can be utilized for increased bit density

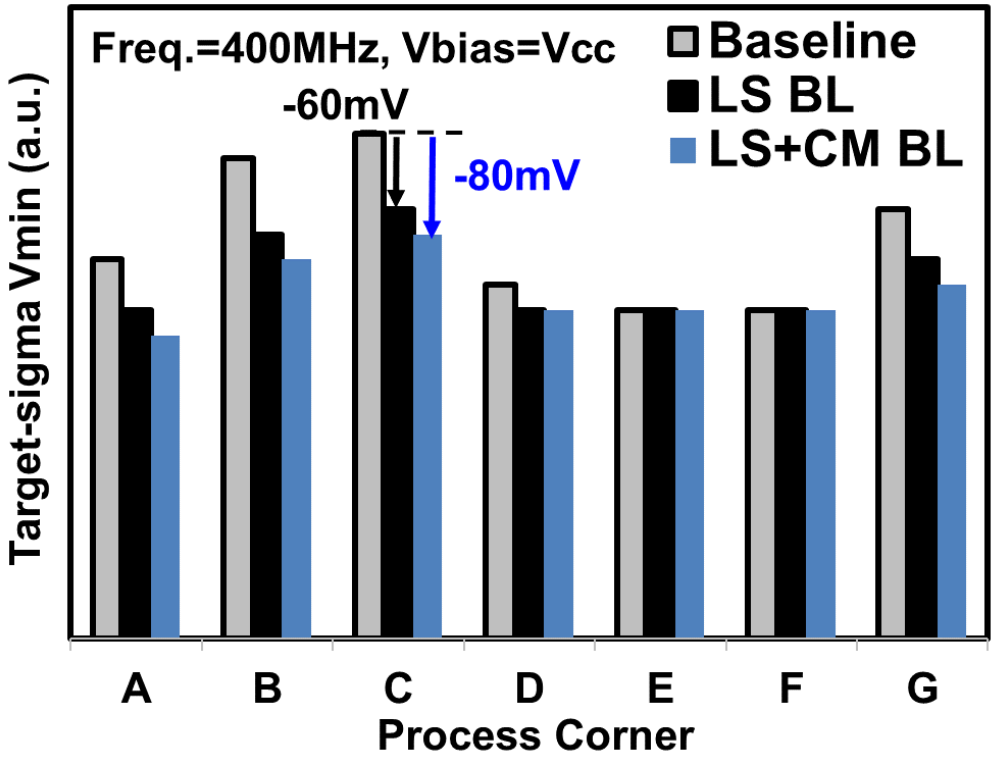
Vmin and Read Delay Statistical Simulations



- Lower read Vmin: 60mV for LS BL, 80 mV for LS+CM BL technique

Vmin and Read Delay Statistical Simulations





- Lower read Vmin: 60mV for LS BL, 80 mV for LS+CM BL technique
- Lower Vmin across multiple process corners

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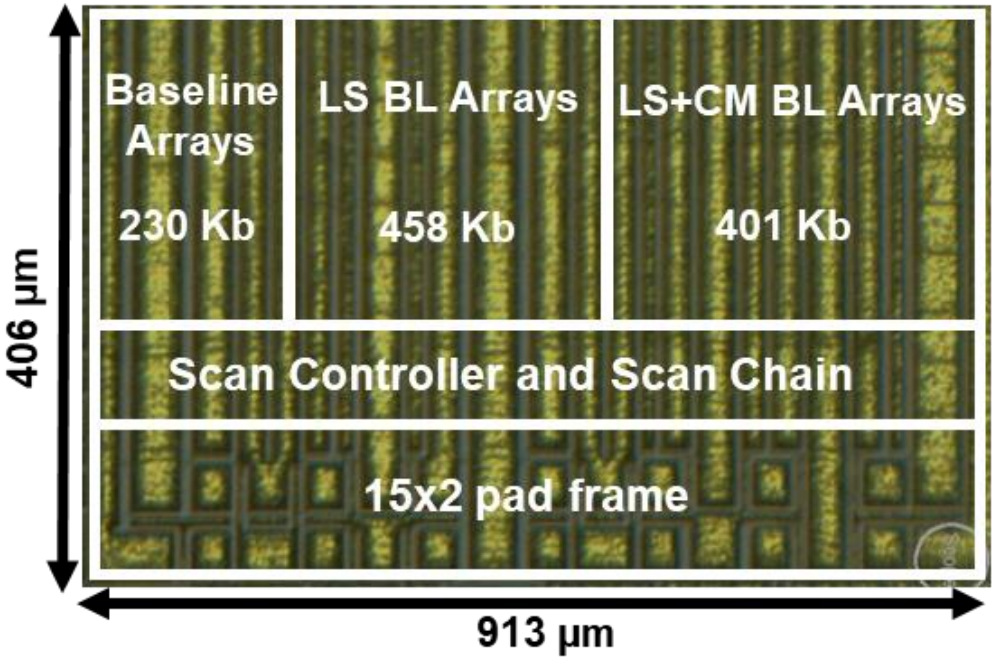
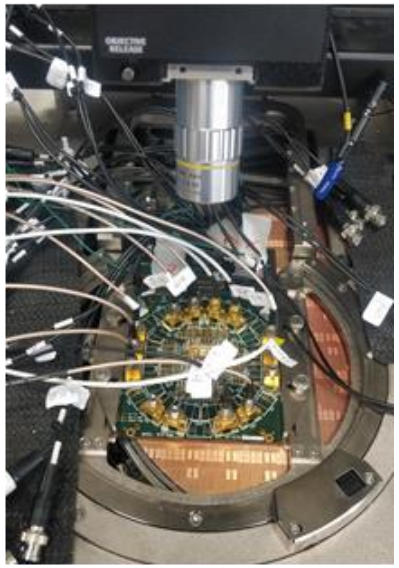
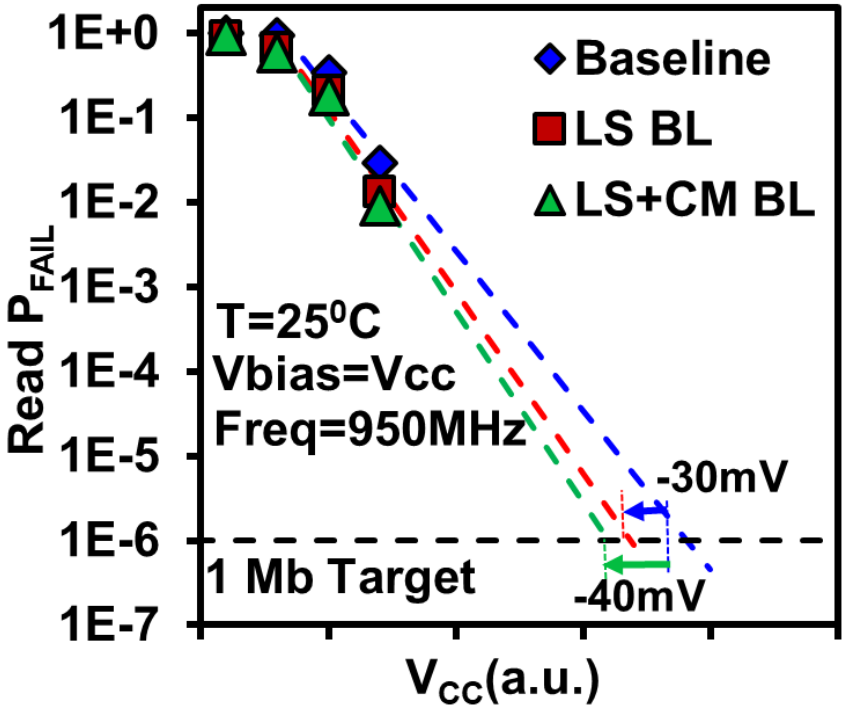
10nm FinFET Test-chip





Technology	10nm FinFET CMOS
# Transistors	16 million
Total die area	0.37 mm^2
Total array capacity	1.09 Mb
8T bitcell sizing, area	1-1-1-2-2, 0.048μm^2
Test interface	Membrane probe

Measured Read Vmin Results



- 30mV lower read Vmin with LS BL technique alone @950MHz, 1Mb target
- 40mV lower read Vmin with combined LS+CM BL technique

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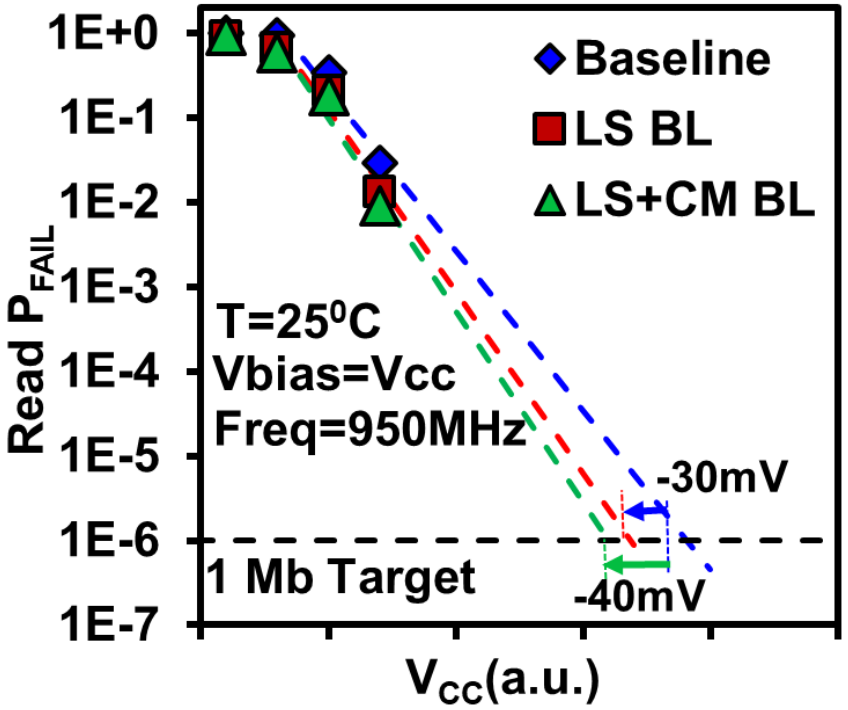
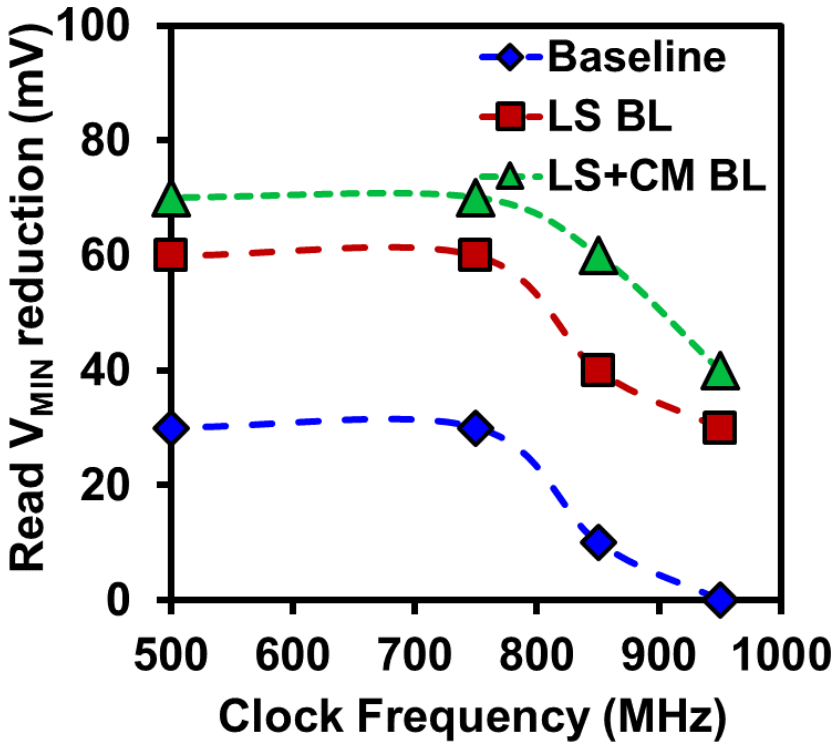
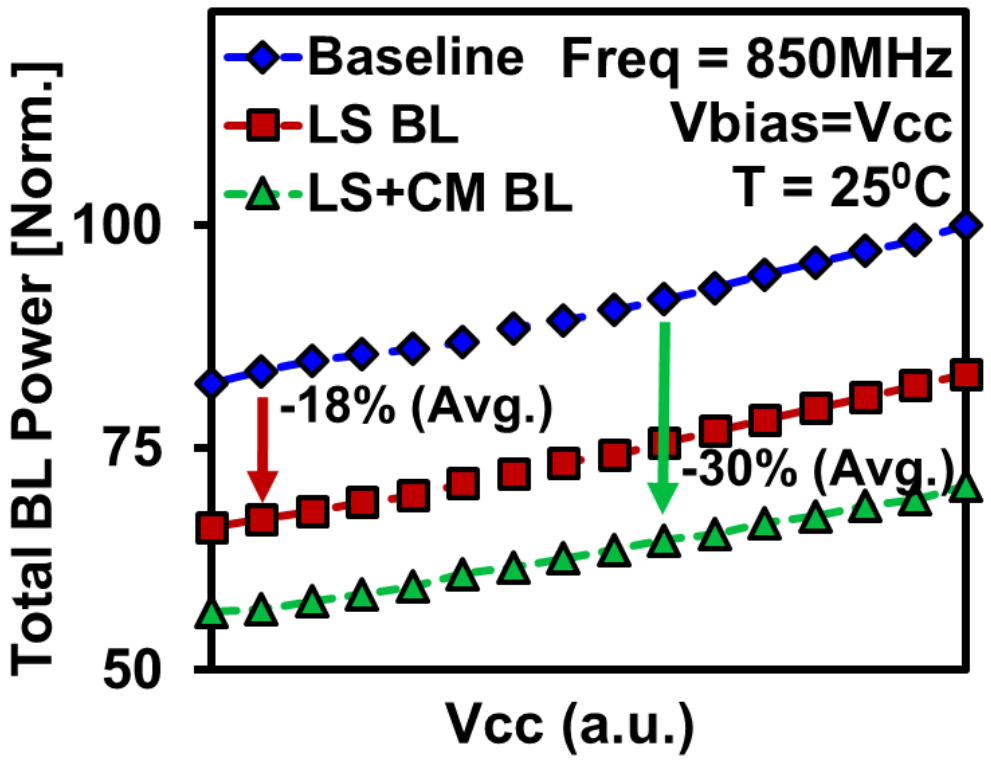




- 30mV lower read Vmin with LS BL technique alone @960MHz, 1Mb target
- 40mV lower read Vmin with combined LS+CM BL technique
- Consistent Vmin savings across operating frequency range

Measured Bitline Power Results



- 18% savings for LS BL, 30% savings for LS+CM across the voltage range

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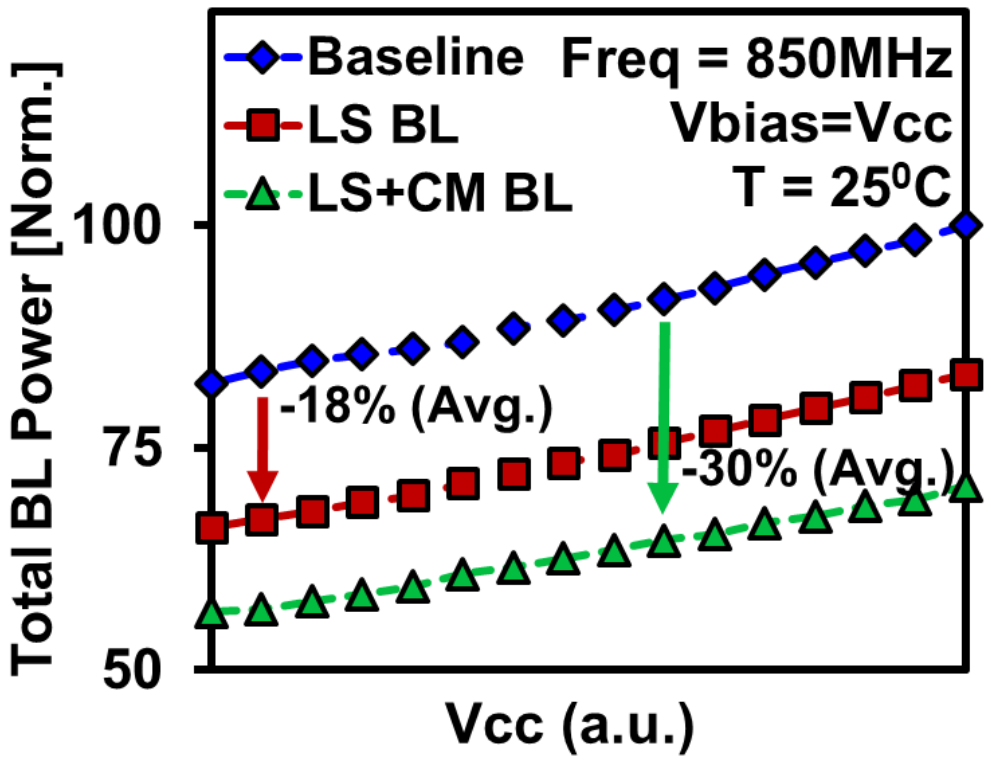
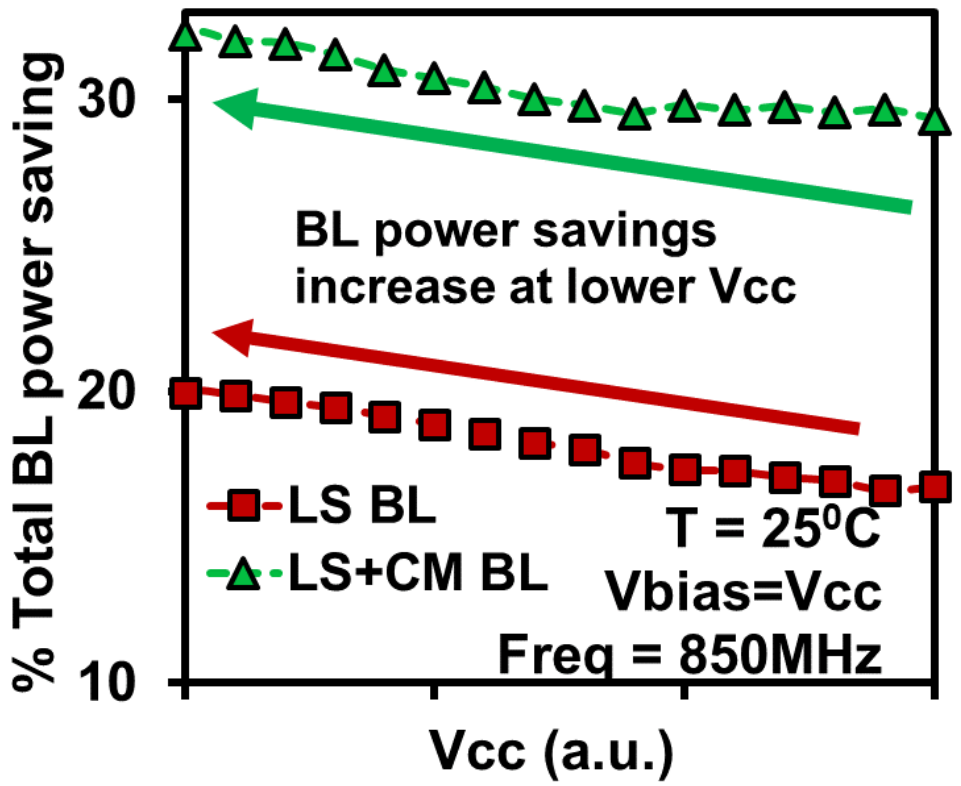
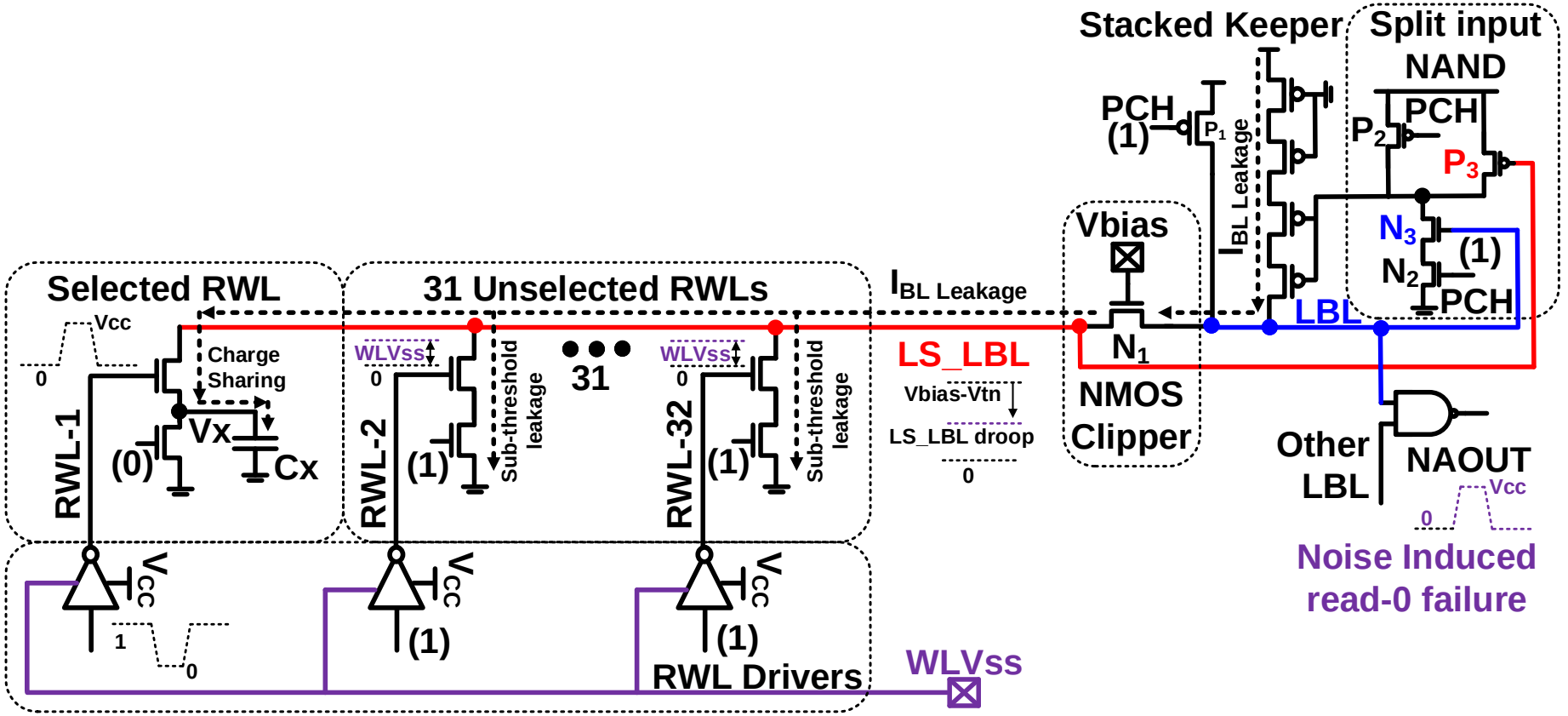




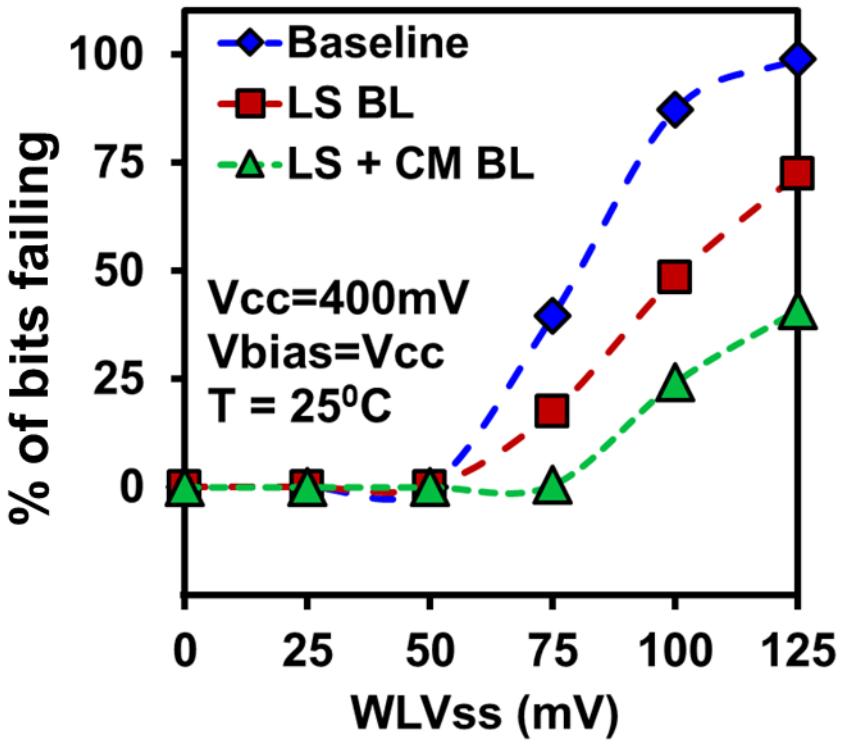
- 18% savings for LS BL, 30% savings for LS+CM across the voltage range
- BL power savings increase at lower Vcc as Vcc-Vt swing reduces

Noise Induced Failures in Read-0 Operation



- Low frequency read-0 test with all ‘1’s stored on unselected bits
- WLVss node voltage of wordline drivers is gradually increased
- Increased BL leakage due to weakly turning ON unselected RWLs

Measured Noise Induced Read-0 Failures



- LS+CM BL with reduced # of bits/sub-LBL achieves superior noise tolerance than LS BL; although both are better than baseline case

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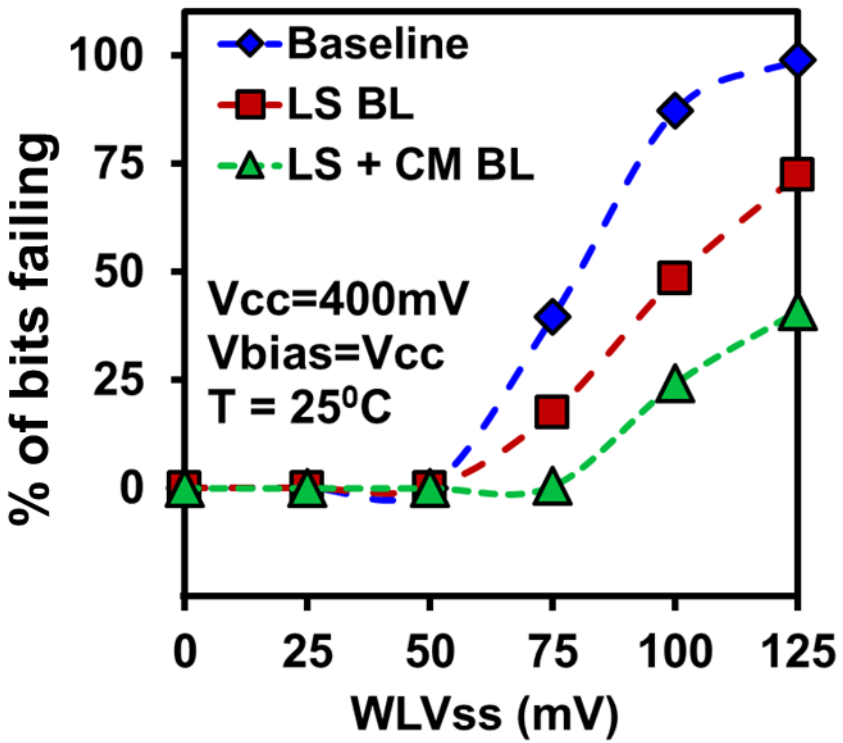
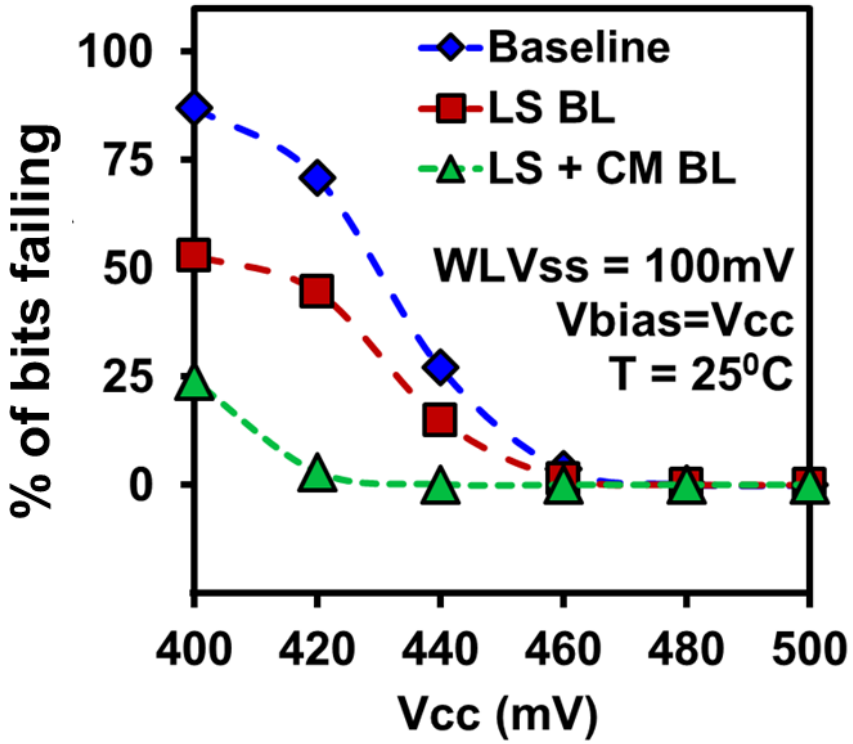
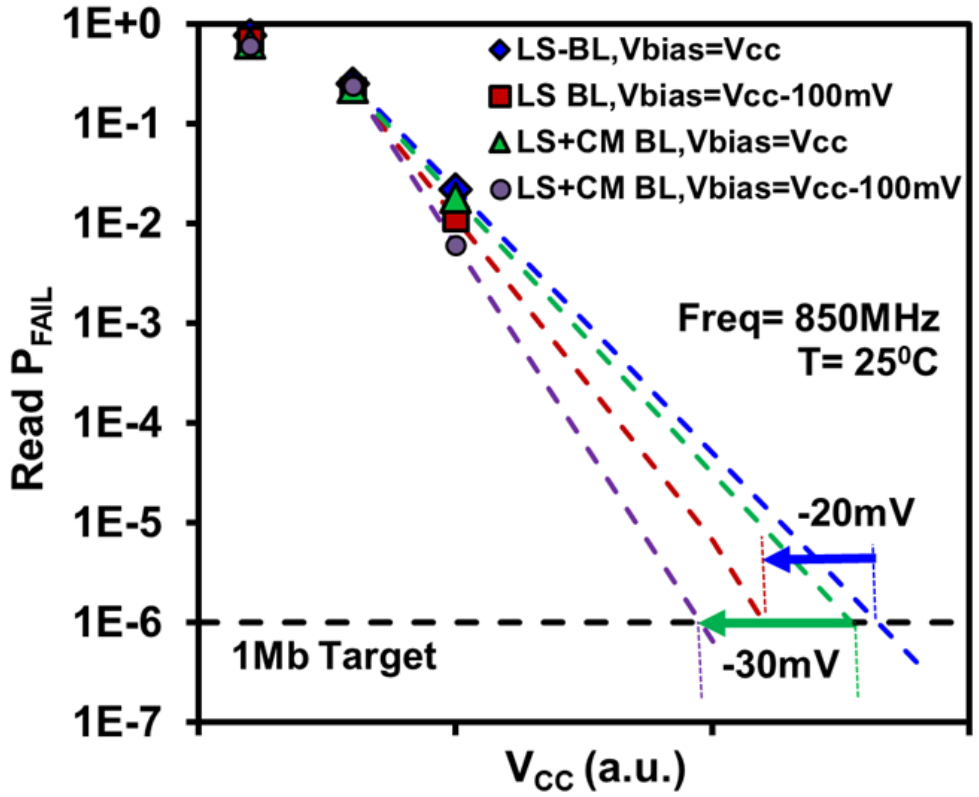




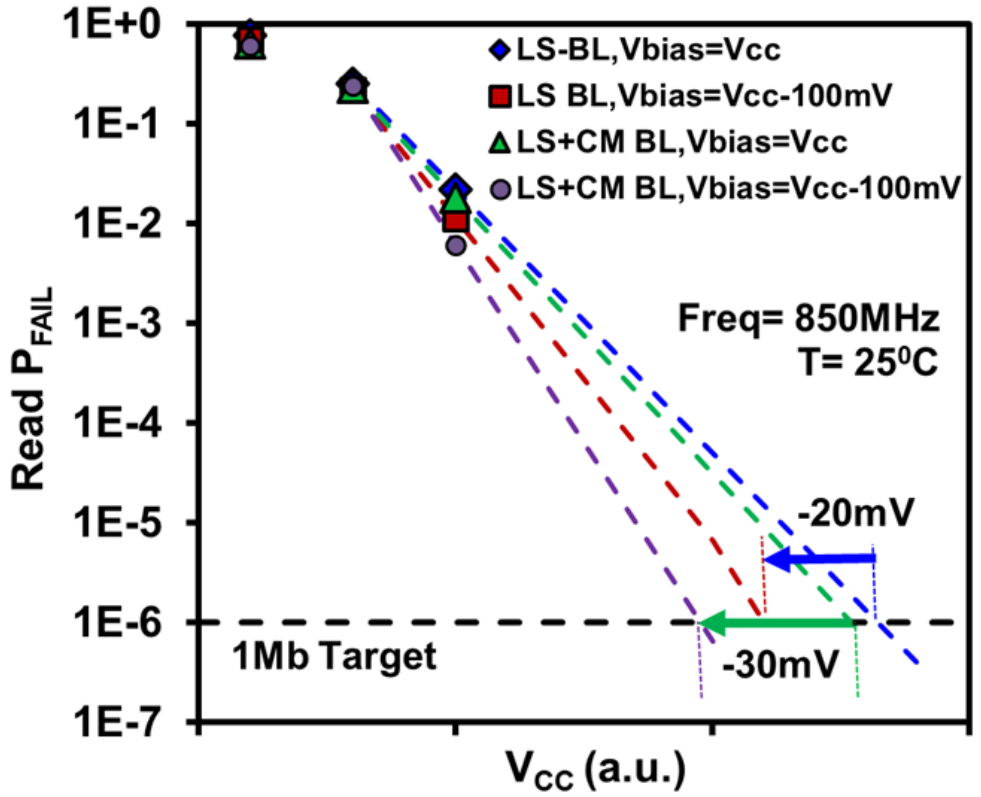
- LS+CM BL with reduced # of bits/sub-LBL achieves superior noise tolerance than LS BL; although both are better than baseline case
- Sustained noise tolerance improvement even at lower Vcc

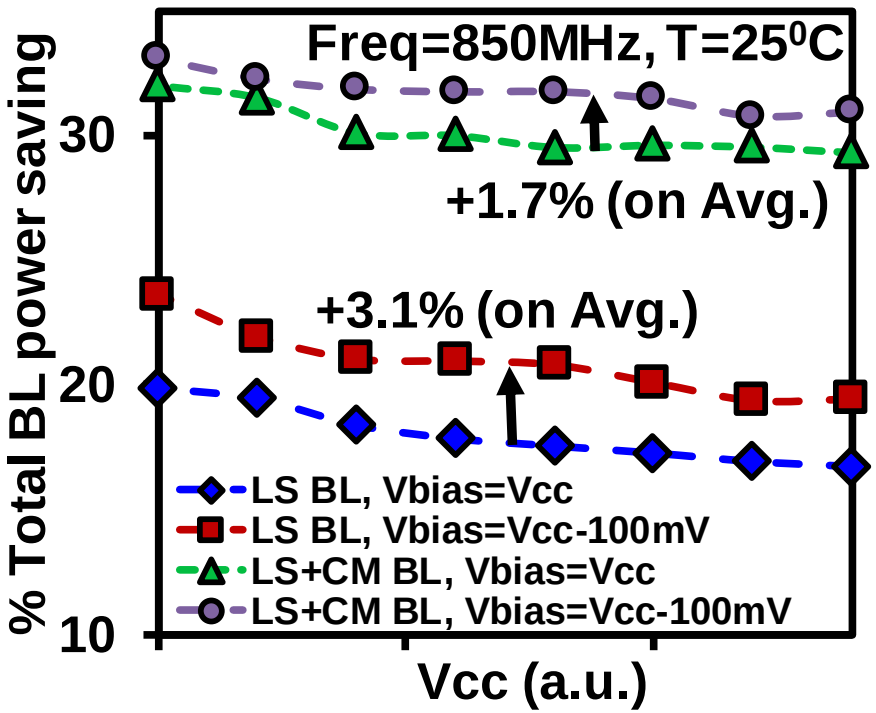
Measured Vmin, Power Sensitivity to LBL Precharge



- Vmin reduced further by lowering LBL precharge level (changing Vbias)
- 20-30mV lower read Vmin with 100mV lower LBL precharge level

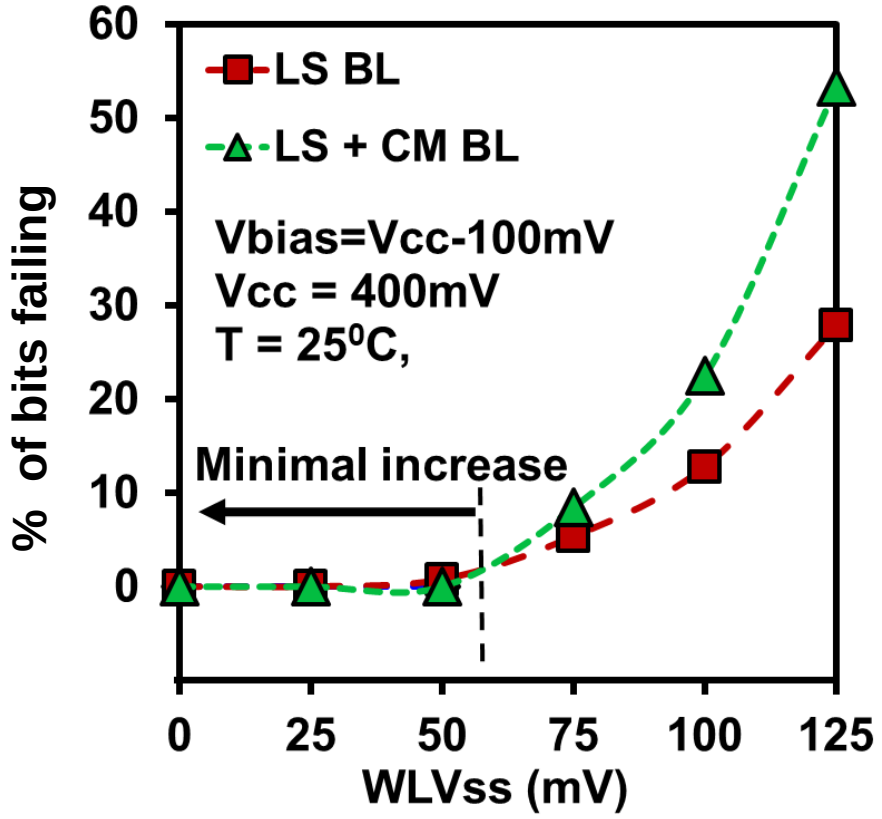
Measured Vmin, Power Sensitivity to LBL Precharge

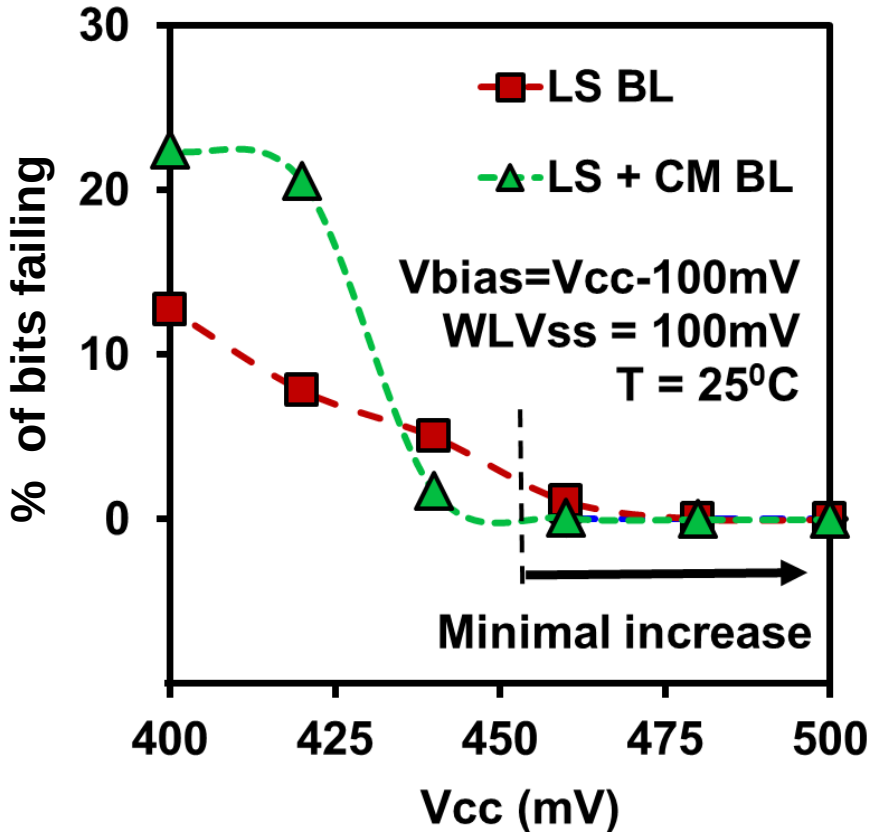




- Vmin reduced further by lowering LBL precharge level (changing Vbias)
- 20-30mV additional read Vmin savings with lower LBL precharge level
- BL power savings increase across the operating voltage range

Measured Noise Sensitivity to LBL Precharge





- With lower LBL precharge, noise induced failures not degraded for WLVss< 50mV and Vcc> 460mV, showing robust noise tolerance

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- Further saving by configuring clipper as column multiplexer

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- Series clipper in read bitline path with split input NAND Keeper
- Further saving by configuring clipper as column multiplexer
- 10nm FinFET CMOS measurements: 1.09Mb HD 1R1W 8T SRAM Array

Figure of Merit (FoM)	LS BL	LS+CM BL
Read Vmin savings	30mV	40mV
Bitline power savings	18%	30%
Noise tolerance increase	44%	72%
Extra transistors in LBL I/O	1	5
Array level area overhead	0%	1.8%

- Simultaneous improvement in FoMs with no (minor) area increase