High Noise Margin, Digital Logic Design using Josephson Junction Field-Effect Transistors for Cryogenic Computing

Siddhartha Raman Sundara Raman[1], Feng Wen[1], Ravi Pillarisetty[2], Vivek De[2], and Jaydeep P. Kulkarni[1]
[1]: University of Texas at Austin, [2]: Intel Corporation, Hillsboro, OR

Abstract — As compute demands and their large energy costs continue to rise in the datacenter, it is imperative to identify low energy compute solutions. One approach is to investigate device schemes based on collective mode phenomena arising at low temperatures where power dissipation and switching voltage can be extremely low. Additionally, such devices could also have applications in quantum computing where such a low power logic/memory scheme could possibly be integrated onto the qubit plane, which is typically at ~10mK temperature. Josephson Junction Field Effect Transistor (JJFET) is a promising candidate for low power operation with zero voltage drop across its drain-source terminals while operating in the superconducting regime. JJFET logic gate is typically realized as a n-type JJFET connected in a common-source configuration with a current source load. This results in high noise margin for logic-1 input but not for both logic-1 and 0. In this paper, we propose an overdamped region, n-type JJFET based digital logic using a cascaded common-source configuration-based design yielding high noise margin for both the logic inputs. DC noise margin sensitivity analysis is performed for the bias current and threshold voltage modulation. The noise margin can be further improved (approaches ideal inverter case) by cascading multiple common source stages yielding higher inverter gain.

***Index Terms*— Common source, Cooper pairs, Critical current, Inverter, Josephson Junction, Noise margin, ,**

I. Introduction

Currently, data center power consumption accounts for over 1% of the world's energy usage. With this figure expected to increase significantly over the next decade [1], it is imperative to identify new ways to reduce computing power consumption. This includes looking at the device level for new types of logic and memory for low power circuit applications. While a variety of different novel device schemes have been looked at for beyond CMOS [2] applications, these have been typically evaluated at operating temperatures at or above room temperature, consistent with conventional processor applications. With recent advancements in cryogenic cooling technology [3], it is timely to explore the applicability of novel cryogenic devices in solving the data center energy problem. In particular, new types of collective mode phenomena, having no counterpart at room temperature, such as superconductivity can exist at low temperature. Additionally, such cryogenic devices could also have applications in quantum computing [4]. Such quantum computers offer the promise to provide an exponential speedup for certain compute applications, which are pervasive across multiple segments of the economy. The quantum bits (qubits) are extremely noise sensitive, so are typically operated on the mixing chamber plate of a dilution refrigerator at ~ 10mK. One of the grand challenges in scaling a quantum system to large numbers of qubits is the need for logic and memory co-integration on the qubit plane. Since this chip is operating at 10 mK, this places extreme switching energy constraints on the device scheme due to cooling overhead cost and a novel cryogenic collective mode device is needed. Low temperature CMOS operation results into, higher threshold voltage, improved subthreshold slope which further leads to low leakage power [5]. Despite these advantages, cryogenic CMOS operations need to operate at moderately higher supply voltage due to higher threshold voltage for achieving same operating frequency. Higher supply voltage leads to higher switching energy dissipation resulting in increased cooling cost. Hence,

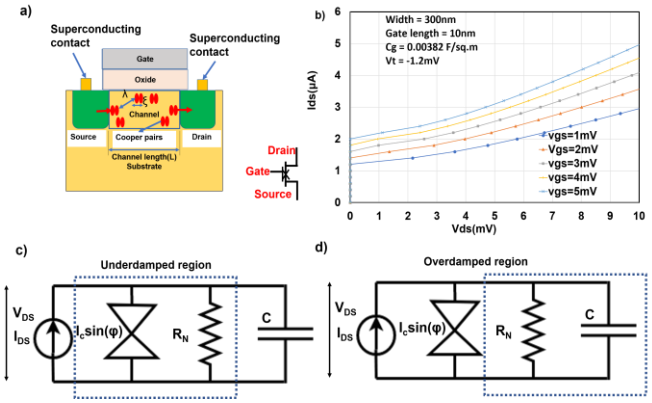

Fig.1a) JJFET schematic with source/drain contacts made of a superconductor. Arrow indicates the direction of cooper pair transport at cryogenic temperatures. L is the channel length, λ is the cooper pair mean free path and ξ is the coherence length of cooper pairs. L<λ and L<ξ ensures that cooper pairs are not destroyed from source to drain transport **b)** I-V characteristics of JJFET in overdamped regime (non-hysteretic); operates in superconducting regime when drain current (Ids) is less than the critical current (Ic) and in resistive regime when drain current exceeds the critical current. **c)** RCSJ model with a parallel RLC network having a phase varying with time for the overdamped region of JJFET with dotted box showing the dominant time constant. Josephson time constant is less than RC time constant **d)** RCSJ model for the underdamped region of JJFET with dotted box showing the dominant time constant. Josephson time constant is greater than RC time constant

S. Siddhartha Raman, Feng Wen and Jaydeep P. Kulkarni are with the Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712, USA.

Ravi Pillarisetty and Vivek De are with Intel Corporation, Hillsboro, OR.
E-mails: s.siddhartharaman@utexas.edu, jaydeep@austin.utexas.edu
Manuscript received. Manuscript submitted

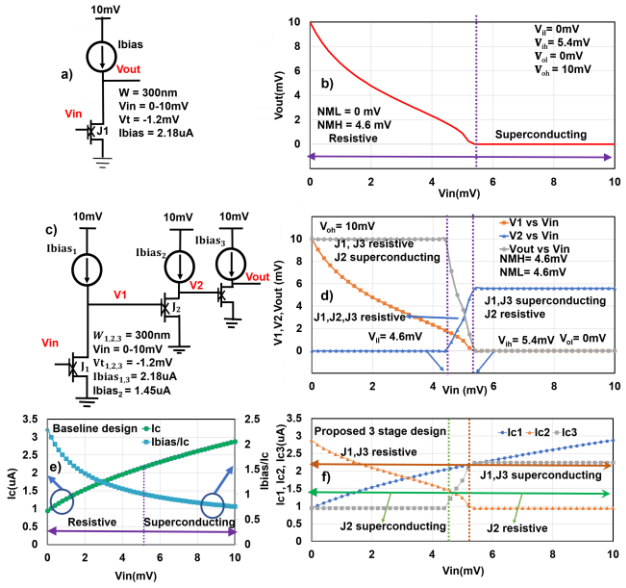

Fig.2 a) The common-source (baseline) JJFET inverter schematic [5] **b)** Baseline inverter DC voltage transfer characteristics **c)** The proposed 3-stage common source JJFET inverter schematic **d)** DC voltage transfer characteristics for the proposed JJFET inverter; V_{il}/V_{ih} refers to the maximum/minimum input value for which the inverter recognizes it as a logic 0/1. The output voltage swing ranges from V_{ol} to V_{oh} . Noise Margins (NM) for both stages of the inverter design. NML = V_{il} - V_{ol} , NMH = V_{oh} - V_{ih} x=1,2 corresponds to the first, second stage of the proposed source follower JJFET. The regions of operation of the configuration is also marked **e)** For Icritical > 2.18uA, JJFET behaves like a superconductor and like a resistor for Icritical < 2.18uA. Ratio of Ibias and Icritical values decreases as Ic keeps increasing with increase in Vin **f)** JJFET operating mode change with input voltage variation for different values of critical current

there is a need to explore alternative devices which can enable lower operating voltage for lower power consumption [5,6]. Josephson Junction Field Effect Transistor (JJFET) is a promising candidate for low power operation with zero voltage drop across its drain-source terminals while operating in superconducting regime [5]. JJFETs are formed by connecting Josephson Junctions which are in turn made of superconducting contacts with a weak link that allows transport of electrons. In the case of JJFET's, it can be viewed like the source and drain contacts made of superconductors as Josephson Junctions with the in-between channel providing a path for the current flow. JJFETs operating at very low supply voltage can minimize the cooling energy cost at cryogenic temperatures. A JJFET logic gate is typically realized as a n-type JJFET connected in a common-source configuration with current source load [5]. This results in high noise margin for logic-1 input but not for logic-0 as the JJFET transitions into resistive regime.

In this paper, we propose a digital logic using an overdamped region, common-source based JJFET yielding high noise margin for both logic inputs. We analyze the DC noise margin sensitivity to the design parameters and outline JJFET device requirements. Further, the noise margin can be improved by cascading multiple common source stages improving the overall inverter gain.

II. JJFET Device Modeling

JJFET is a three terminal MOSFET-like device (Fig. 1a) that relies on superconductivity [5,7,8], the property by which charge moves through a material in the form of cooper pairs without any resistance for their transport. The cooper pairs in superconductors are formed due to the electron-phonon interactions at very low temperatures [8]. These cooper pairs form the channel of JJFET and are responsible for the drain-source current. The source, drain contacts can be made of superconductors like Niobium (Nb) or Aluminum (Al) [9], as shown in Fig.1a. The JJFET exhibits superconducting behavior for drain current (Ids) less than a critical current (Ic) resulting in zero voltage drop across drain to source terminals as depicted in Fig. 1b. The JJFET exhibits a resistive behavior when the drain current exceeds the critical current. The gate voltage modulates the JJFET critical current altering the transition point between superconducting region and resistive operating region.

JJFET devices comprise of Josephson junctions which can operate in either as short or long, diffusive or ballistic mode of operation. In this work, JJFET is modeled assuming short channel ballistic transport [5]. The device is short because the channel length is assumed to be smaller than the coherence length and this is sufficiently small to allow coherent movement of cooper pairs [5]. In case of a Nb contact, the coherence length ~15nm and it is ~40nm in case of Al contact [5]. The transport mechanism of cooper pairs is ballistic because the channel length is assumed to be smaller than the cooper pair mean free path. The mean free path for Al contacts has been reported to be around 87nm[10].

JJFET can be modelled using RCSJ model wherein the current-voltage characteristics are derived in terms of the Josephson phase φ(t), the phase difference of the wave function between the source and drain superconducting contacts [5].

$$I_{DS} = C\frac{dV_{DS}}{dt} + \frac{V_{DS}}{R} + I_C \sin(\varphi(t)) \quad (1)$$

Where $V_{DS} = \frac{h}{2e} \cdot \frac{d\varphi(t)}{dt}$

Where V_{DS} is the drain to source voltage, I_{DS} is the drain to source current, R_N is the normal resistance and I_C is the critical current of the JJFET.

$$R_N = \frac{V_0}{I_c}; \quad (2)$$

where $V_0 = \pi \cdot \triangle/2$ (3)

Where $\triangle$ is the superconductor gap voltage [11] and $\triangle$ is equal to 3.05mV or 0.45mV when the superconducting contact is Nb or Al respectively [5].

$$I_c = \frac{4.V_0.W.e}{h}\sqrt{2 \cdot e \cdot \frac{C_g}{\pi} \cdot (V_g - V_t)} = g \cdot V_0 \quad (4)$$

Where C_g is the gate capacitance per unit area, V_t is threshold voltage, V_g is the gate voltage, W is the device width, h is Planck's constant, e is electronic charge.

The conductance (g) of the device when normalized with the average velocity along the direction of the channel, can be modelled using the below equation:

$$g = W \cdot 4e^2 \cdot \frac{\sqrt{(2 \cdot \pi \cdot n)}}{(\pi \cdot h)} \quad (5)$$

Equation (1) can be written as

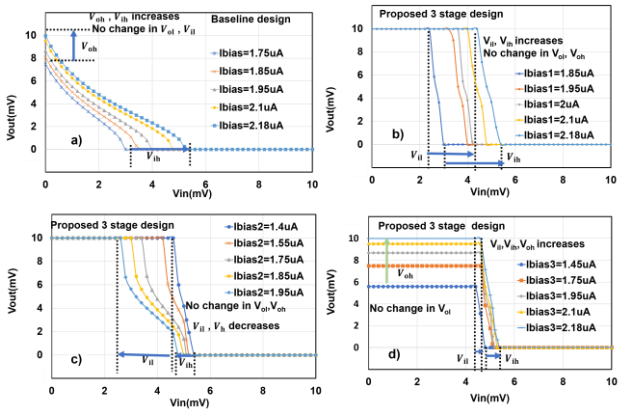

Fig.3 a) DC voltage transfer characteristics for the baseline inverter varying I_{bias}; V_{ol} and V_{il} are 0 irrespective of I_{bias} **b)** DC voltage transfer characteristics for the proposed 3 stage design as a function of Ibias1 keeping Ibias2, Ibias3 fixed at 1.45uA, 2.18uA respectively. V_{oh} and V_{ol} are at Vcc (10mV) and 0mV respectively irrespective of Ibias1 **c)** DC voltage transfer characteristics for the proposed 3 stage design as a function of Ibias2 keeping Ibias1, Ibias3 fixed at 2.18uA,2.18uA respectively. V_{oh} and V_{ol} are at Vcc (10mV) and 0mV respectively irrespective of Ibias2 **d)** DC voltage transfer characteristics for the proposed 3 stage design vs. Ibias3 with Ibias1, Ibias2 fixed at 2.18uA,1.45uA respectively. V_{ol} is 0mV irrespective of Ibias3.

$$\frac{I_{DS}}{I_c} = \sin(\varphi) + \frac{d\varphi}{d\tau} + \frac{\beta d^2\varphi}{d\tau^2} \quad (6)$$

Where τ is defined as $\frac{t}{\tau_j}$; τ_j is defined as the Josephson time constant given by

$$\tau_j = \frac{Lj}{R} = \frac{h}{2e} \cdot \frac{1}{I_c . R_N} \quad (7)$$

And β is defined as the square of Stewart McCumber parameter which is further equal to the ratio of Josephson time constant and time constant due to RC network

$$\beta = Q^2 = \frac{\tau_j}{\tau_{RC}} = 2 \cdot e \cdot {R_N}^2 \cdot \frac{C}{h} \quad (8)$$

Qualitatively, this can be viewed as a parallel RLC network with a time varying phase. JJFET is operating in overdamped region when the Josephson time constant due to RL (L/R) is greater than the time constant due to RC (RC) and in underdamped region when the Josephson time constant due to RL (L/R) is lesser than the time constant due to RC (RC) network as shown in Fig.1c and 1d. JJFET inverter in common source configuration can operate in either underdamped regime or over-damped regime [5,7,8,9], governed by the Q parameter

$$Q = \frac{(\pi^{1.5} \cdot V_0 \cdot (C_L + C_j))}{\sqrt{(2 \cdot e \cdot C_g \cdot (V_{in} - V_t)}} \quad (9)$$

Where, C_L, C_j is the load and junction capacitance/per unit device width respectively. It is important to note that JJFET operating in under-damped (Q>1) regime exhibits hysteretic characteristics as well as ringing due to inductive nature of JJFET I-V relationship induced by the phase of cooper-pairs, both of which are not suitable for robust logic circuit operation. Hence, the device parameters need to be optimized in such a way that the JJFET is operating in the overdamped regime (Q<1) resulting in non-hysteric behavior for achieving high noise margin and functionally correct logic circuits at cryogenic temperature.

Overdamped (non-hysteretic) regime JJFET Verilog-A model introduced in [5] is adopted for the circuit analysis. I-V characteristics of a JJFET operating in overdamped regime, where the Stewart-McCumber parameter is assumed to be 0, can be expressed as [7,8]:

$$V_{DS} = R_N \cdot \sqrt{{I_{DS}}^2 - {I_C}^2}\,; I_{DS} > I_C \quad (10)$$

$$V_{DS} = 0\,; \qquad I_{DS} < I_C \quad (11)$$

I-V characteristics showing JJFET in overdamped regime for varying values of V_{gs} is plotted in Fig.1b. It is worth mentioning that JJFET used here has been modelled similar to a depletion mode MOSFET with negative threshold voltage as described in [5].

III. COMMON SOURCE JJFET LOGIC

Fig. 2a and 2b show the schematic and the DC voltage transfer characteristics (Vcc=10mV) of the JJFET common-source inverter design (referred as the baseline design) [5]. For logic-1 input with higher gate bias, the critical current given by Eq. (4) exceeds the bias current resulting in superconducting JJFET behavior with V_{DS}=0 (i.e. V_{ol} =0mV). However, for logic-0 input with zero gate bias, the critical current is less than the bias current resulting in resistive JJFET behavior, with reduced noise margin (i.e. V_{il}=0mV). Fig. 2e shows the variation of critical current as a function of Vin depicting different regions of JJFET inverter circuit operation.

Fig. 2c and 2d show the schematics and DC voltage transfer characteristics of the proposed common source based 3 stage JJFET inverter. The three-stage inverter circuit consists of JJFET's with current source load connected in a common-source configuration which are cascaded together. The device parameters and biasing current for all stages are optimized to achieve overdamped regime of JJFET behavior for both input conditions. JJFETs are biased in such a way that the value of the bias current is in between the critical current corresponding to the logic-0 input low and logic-1 input high. For low Vin, I_{C1} is less than I_{bias1} resulting in J_1 device operating in resistive regime. As Vin is ramped up, I_{C1} increases (given by Eq. 4) resulting in reduced output resistance (given by Eq. 3) which decreases V1. As Vin ramps up to a critical voltage (V_{crit1}= the voltage at which I_{c1}= I_{bias1}), J_1 device transitions into superconducting regime, resulting in zero voltage drop across its output, i.e. V=0. The first stage is necessary predominantly to set the high noise margin of the inverter. Similarly, for the second stage, J_2 device would be in superconducting regime with its V_{ds}=0 when I_{C2} exceeds I_{bias2}. This could happen for V1 values which are greater than the voltage necessary to ensure that the critical current of J_2 is greater than I_{bias2}. V1=0 voltage corresponds to J_2 being in resistive stage and saturates V2 at around 6mV. The voltage saturates at 6mV because the voltage in the resistive regime corresponding to the current bias of 1.45μA is 6mV. The second stage coupled with first stage is necessary for obtaining non-zero low noise margin. The third stage is necessary for logic functionality of an inverter. The biasing current of the third stage is chosen in such a way that V_{oh}=10mV as shown in Fig. 2d. The third stage is superconducting for voltages greater than V_{ih} of the inverter and is resistive for other input voltages. V_{oh} of the design is predominantly set by the third stage. Thus, by combining

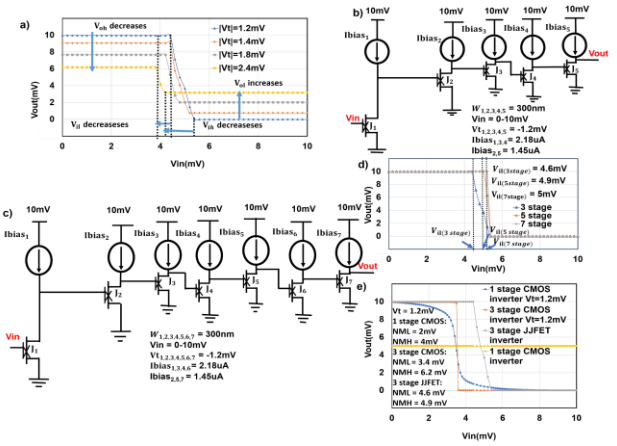

Fig.4 a) Vout vs Vin with |Vt| modulation with 3 stage common source JJFET Inverter; V_{oh}, same but V_{ol} increases with |Vt| **b)** JJFET inverter with 5 stages of common-source configuration cascaded **c)** JJFET inverter design with 7 stages of common-source configuration cascaded **d)** Improving noise margin and inverter gain with increasing source follower stages; DC voltage transfer characteristics for 3,5 and 7 stage design . **e)** Comparison between 3-stage cryo-CMOS, 1-stage cryo-CMOS with V_t modulated to 1.2mV, 1-stage cryo-CMOS with no V_t modulation(yellow line) and 3-stage JJFET inverter

common source JJFET's, superconducting regions of the 3 stages of JJFETs are utilized for achieving high noise margins for both input conditions (Vout saturating at Vcc/0 for low/high V_{in}). The proposed design increases V_{il} to 4.6mV which is 45% higher than the baseline design for 10mV Vcc design. Fig. 2f shows the critical current variation for all stages of the proposed 3-stage common source inverter design and operating regions of J_1, J_2, J_3 as a function of input voltage. It is important to note that all the JJFETs are in resistive regime when the output transitions from 10mV to 0mV as shown in Fig. 2d and determines the gain of the inverter circuit.

IV. DESIGN SENSITIVITY ANALYSIS

JJFET region of operation and the noise margin of the inverter is governed by the bias current as well as the critical current. Critical current is further determined by the threshold voltage which determines the supply voltage for JJFET operation and careful consideration of threshold voltage is required for low voltage, low temperature operation.

The bias current plays an important role in determining the noise margin of the inverter. For the baseline design, as I_{bias} increases, V_{ds} increases as given by Eq.1 which leads to higher V_{oh}(Fig. 3a). Also, with increased I_{bias}, the required Ic (basedon Vin modulation) to transition JJFET into superconducting regime increases leading to higher V_{oh} (Fig. 3a). For the proposed 3 stage design, with I_{bias1} increase, V_{ih} increases because the resistive operating region of J_1 expands and since V_{ih} is predominantly set by the first stage, there is a large sensitivity of V_{ih} with respect to I_{bias1}. V_{il} increase is because the range of voltages for which J_2 is superconducting increases as the range of voltages for which J_1 is resistive increases (Fig. 3b). Furthermore, with I_{bias2} increase, the range of voltages for which J_2 operates as a resistor increases thus decreasing V_{il} and V_{ih} (Fig. 3c). V_{il} is highly sensitive to I_{bias2} because the V_{il} of the inverter is predominantly fixed by I_{bias3}. V_{oh} and V_{ol} are not affected by I_{bias1} and I_{bias2} modulation. Similarly, I_{bias3} increase results in an increase of resistive regime of J_3 resulting in an increase in V_{il} and V_{ih} (Fig.3d). It is important to mention that V_{il} and V_{ih} are not highly sensitive to changes in I_{bias3}. V_{oh} increases because the voltage at the output of the J_3 increases as described in Eq. 10.

Threshold voltage of JJFET modulates the critical current of the device which further affects the inverter noise margin as shown in DC transfer characteristics of 3-stage design in Fig. 4a. As $|V_t|$ increases, critical current increases (V_t is negative), as given in Eq. 4, thus decreasing the voltage at the output when J_3 is in resistive region, resulting in lowered V_{oh}. V_{il} of the design is set by the combination of first and second stages. V_{ih} of the design is predominantly set by the first stage. As critical current increases, the range of voltages for which J_1 operates in superconducting regime increases which decreases V_{ih}. Also, another effect is that the output voltage swing decreases at the output of first stage because of decrease in V_{ds} for resistive regime which further results in decrease in the range of voltages for which J_2 is superconducting, thus decreasing V_{il}. It is important to note that as critical current increases, the output voltage of the second stage corresponding to voltage low at the output of first stage decreases, which results in J_3 not entering superconducting regime, further resulting in increase of V_{ol}. As the number of stages increases from 3 to 5 as shown in Fig. 4b, V_{il} increases from 4.6mV to 4.9mV. DC voltage transfer characteristics for 7 stage design are similar to the ideal inverter characteristics with noise margin low and high approximately equal to 5mV (Vcc/2) as shown in Fig. 4c and 4d. Cascading multiple common source JJFET stages reduces the voltage range for which all the JJFET's are in resistive regime and results in increase of V_{il} and V_{ih} which further results in high noise margin for the logic-0 and logic-1 inputs.

The proposed JJFET inverter design is compared with CMOS inverter designed using ASU 7nm Predictive Technology model(PTM)[12]. The analysis compares cryo-CMOS(4K) inverter with i) JJFET of iso-threshold voltages assuming the metal work function can be modified to modulate V_t so as to compensate for the increase in V_t due to carrier freezeout and ii) without changing V_t as shown in Fig. 4e .

V. CONCLUSION

This work presents a 3-stage, common source based JJFET inverter design yielding high noise margin for both logic-0 and logic-1 inputs, unlike the baseline common-source configuration which yields high noise margin for logic-1 input only. Detailed comparison of the proposed design with the baseline design, along with the noise margin sensitivity to different parameters (V_t, I_{bias1}, I_{bias2}, I_{bias3}) is presented. Three stage, common source inverter utilizes the resistive operating region of the JJFETs J_1, J_2 to improve logic-0 input noise margin by 45% compared to the baseline design. By inserting additional source-follower stages, logic-0 noise margin can be further improved achieving near-ideal noise margin of ~Vcc/2 for both inputs while operating at low V_{cc}.

VI. ACKNOWLEDGEMENT

This research work is supported by Intel Corporation. Authors would like to thank Prof. Emanuel Tutuc and Prof. Javad Shabani for technical discussions.

VII. REFERENCES

[1] N. Jones, "The information factories", Naure, 13 september 2018, Vol. 561, pp. 163- 166

[2] S. Salahuddin, K. Ni, S. Datta, "The era of hyper-scaling in electronics", Nature Electronics, pp. 442–450, 2018

[3] Wang, B., and Z. H. Gan. "A critical review of liquid helium temperature high frequency pulse tube cryocoolers for space applications." *Progress in Aerospace Sciences* 61 (2013): 43-70.

[4] S. S. Tannu, D. M. Carmean, M. K. Qureshi "Cryogenic-DRAM based Memory System for Scalable Quantum Computers: A Feasibility Study", MEMSYS '17: Proceedings of the International Symposium on Memory Systems, Pp 189–195, October 2017

[5] F. Wen, J. Shabani and E. Tutuc, "Josephson Junction Field-Effect Transistors for Boolean Logic Cryogenic Applications," in *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5367-5374, December 2019.

[6] M. Aoki, S. Hanamura, T. Masuhara and K. Yano, "Performance and hot-carrier effects of small CRYO-CMOS devices," in *IEEE Transactions on Electron Devices*, vol. 34, no. 1, pp. 8-18, January 1987.

[7] T. R. Gheewala, "Josephson-Logic Devices and Circuits," IEEE Transactions on Electron Devices, vol. ED-27, pp. 1857- 1869, 1980.

[8] *C. R. Nave,* "Cooper pairs, Hyperphysics", *Dept. of Physics and Astronomy, Georgia State Univ. Retrieved 2008-07-24, 2006*

[9] W. C. Stewart, "Current-Voltage Characteristics of Josephson Junctions," Applied Physics Letters, vol. 12, pp. 277-280, 1968.

[10] Mayer, W., Yuan, J., Wickramasinghe, K. S., Nguyen, T., Dartiailh, M. C., & Shabani, J. (2019). Superconducting proximity effect in epitaxial Al-InAs heterostructures. *Applied Physics Letters*, *114*(10), 103104

[11] D. E. McCumber, "Effect of ac Impedance on dc Voltage-Current Characteristics of Superconductor Weak-Link Junctions," Journal of Applied Physics, vol. 39, pp. 3113-3118, 1968.

[12] http*://ptm.asu.edu*