

Field-Emission Enhanced Contacts for Disordered Semiconductor based Thin-Film Transistors

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Our presentation will report on substantial improvements to the performance characteristics of small channel length thin-film transistors (TFTs) made with disordered semiconductors such as amorphous indium gallium zinc oxide (IGZO) and pentacene with channel lengths in the range 10-200 nm. These improvements include reduced contact resistances that are deduced from the total channel resistance, increased effective carrier velocities, and improved sub-threshold response. The primary reason for these improvements is the improved carrier injection from source and drain contact metals to nominally undoped semiconductors resulting from using tapered geometries (nanospikes). Field emission, analogous to that seen in vacuum devices with sharp electrode tips, increases the local electric field at the contact tips and results in improved injection of charge from the metal contact to the band states or conducting states of the semiconductor. Conventional flat electrode devices have been fabricated alongside the nanospike TFTs for comparison. For all TFTs, a side guard electrode, held at the drain potential, was included that blocked spreading current from the source to the drain from regions away from the actual channel. This was necessary since the gate and the semiconductor were not patterned.

With ~200 nm channel length nanospike IGZO TFTs fabricated by electron beam lithography as shown in **Fig. 1**, carrier velocities up to 3×10^6 cm/s are attained, as deduced from the drain current magnitudes. This value is the highest achieved for IGZO and one of the highest for a thin-film semiconductor. This nanospike TFT's carrier velocity was also much higher than that extracted from a flat electrode TFT fabricated alongside. The field effect mobility is more than $12 \text{ cm}^2/\text{V-s}$ for a single nanospike TFT. In **Fig. 2**, the total channel resistance, which is the sum of contact resistance and channel resistance, is as low as 2 Ohm-cm, the lowest value attained for IGZO so far. In all these metrics, the nanospike TFTs outperform the flat electrode TFTs as shown in the figures. The output characteristics, corrected for gate leakage, show that both nanospike and flat TFTs are relatively well-behaved. A comparison of the transfer characteristics of single nanospike and flat electrode devices show that the nanospike TFTs have steeper sub-threshold swings. This is attributed to the better gate control of the drain current near the drain due to the tapered geometry of the electrode. It is expected that this advantage will also exist in multi nanospike TFTs (to increase channel width) if the individual nanospikes are separated.

The data from pentacene TFTs is very analogous to amorphous IGZO TFT data, but with smaller channel lengths down to 10 nm seen in SEM images in **Fig.3**. The carrier mobility of pentacene in these TFTs at low electric fields is near $0.1 \text{ cm}^2/(\text{V-s})$. The output characteristics in **Fig. 4** show saturation and the total device resistance per unit channel width is an order of magnitude lower than for flat electrode devices, reaching values near 40 Ohm-cm, which is comparable to the lowest contact resistance reported for any organic TFT. It is expected that the contact resistance will be reduced further if semiconductors with higher carrier mobility are employed in conjunction with nanospike electrodes. The output characteristics of a nano-spike TFT with a 5 nm thick SiO_2 gate insulator are especially noteworthy as they demonstrate low voltage operation and saturation. Finally, it is noted that the nano-spike TFT design is scalable to arbitrary channel widths by using multiple nanospikes. The fabrication of such structures can be performed in the future by high-throughput nanomanufacturing techniques such as nanoimprint lithography.

In summary, we have demonstrated a new technique to substantially improve the performance of TFTs with small channel lengths using field-emission type contacts. This approach was demonstrated for two semiconductors, IGZO and pentacene, and should also work for other semiconductors.

[1] X. Wang *et al.*, *IEEE-TED*, vol. 68, p. 125, (2021).

[2] H. Ye *et al.*, *IEDM Tech. Dig.*, p. 613. (2020).

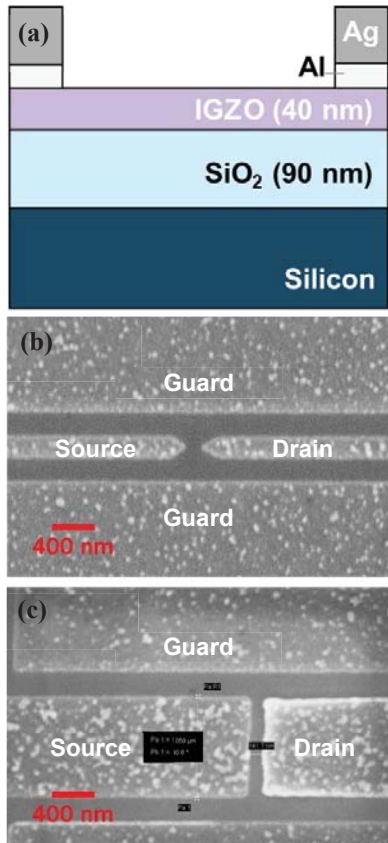


Fig. 1 (a) Device structure of IGZO TFTs and SEM images of (b) nanopike- and (c) flat-electrode TFTs with guard electrodes.

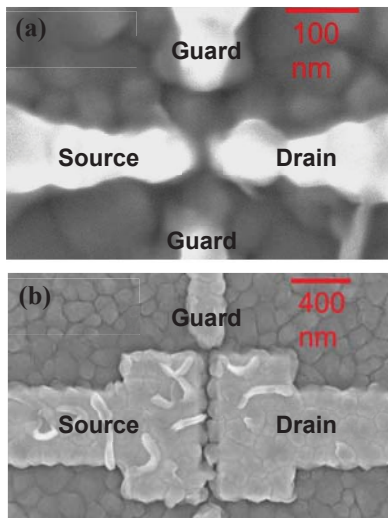


Fig. 3 SEM images of pentacene TFTs with (a) nanopike- and (b) flat-electrode TFTs with guard electrodes.

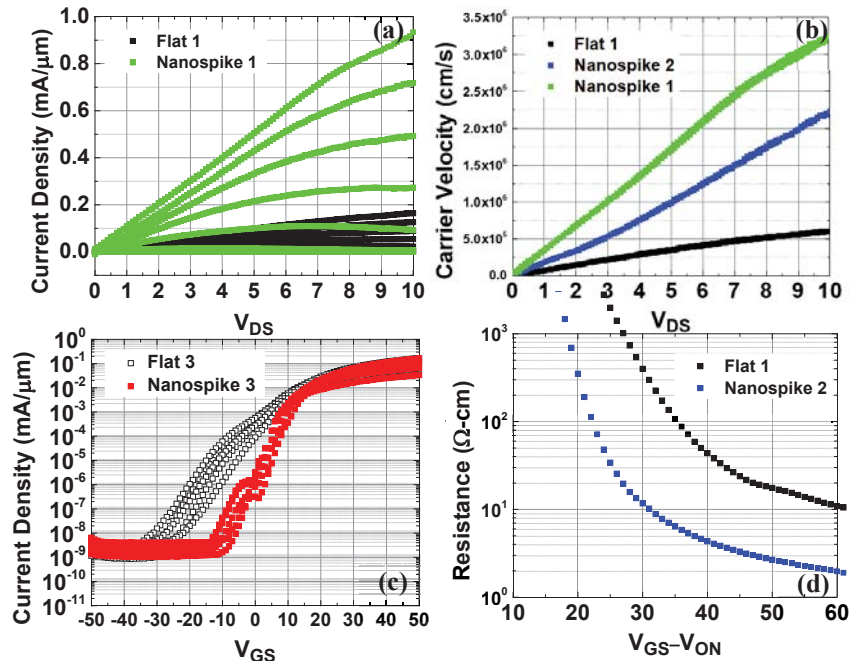


Fig. 2 IGZO TFTs. (a) Output characteristics comparing nanopike and flat TFTs. (b) Carrier velocities reaching 3×10^6 cm/s for nanopike. $V_{GS} = 50$ V. (c) Subthreshold swing improvement with nanopike design. (d) Device resistance reduced by factor of 5-30, indicating lower contact resistance in the nanopike device. $V_{DS} = 10$ V.

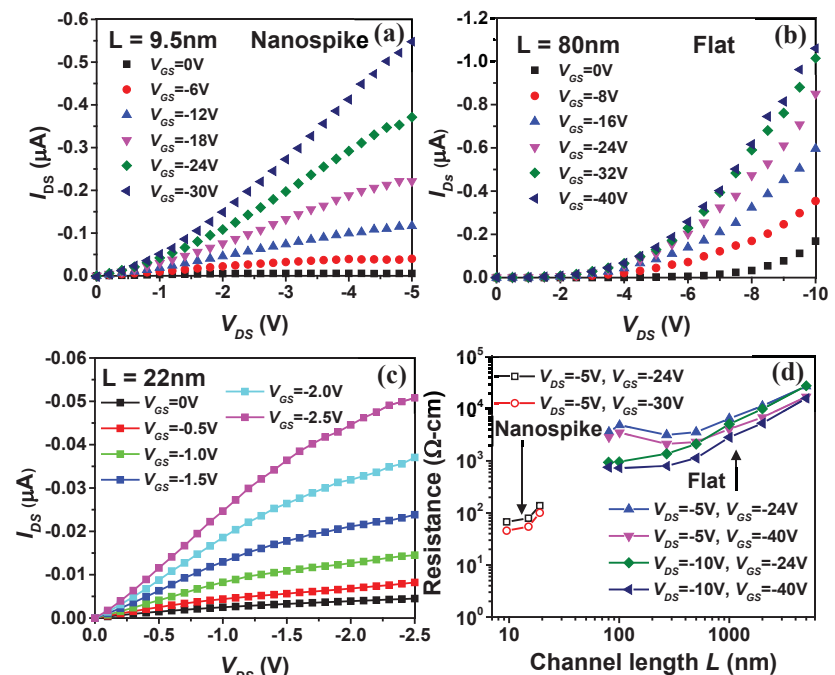


Fig. 4 Pentacene TFTs. Output characteristics of (a) 10 nm channel length nanopike TFT, (b) 80 nm channel length flat electrode, and (c) 22 nm channel length nanopike TFT with thin 5 nm gate dielectric and low operating voltages. (d) Lower resistance with nanopike contacts at small channel lengths compared to flat contacts.