# A High Output Power 1V Charge Pump and Power Switch for Configurable, In-Field-Programmable Metal eFuse on Intel 4 Logic Technology

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**Abstract:** A flexible, low-cost design solution for In-Field-Programmable (IFP) metal eFuse is presented. The design maximizes fuse yield through a tunable program voltage provided by a two-stage charge pump (CP), placed in closed-loop (CL) with a low dropout regulator (LDO). The integration of CP and LDO solves electrical over-stress (EOS) concerns, and achieves stability and low voltage operation through several design innovations, and does not require a specific power sequence or MIM cap. This design is implemented and characterized on Intel 4 technology, where >99.9% successful fuse bit program was measured across [-40C, 125C] temperature, and down to 0.95V.

**Keywords:** charge pump, OTP-ROM, metal fuse.

**Introduction:** One-time programmable (OTP) metal fuse is an on-chip memory, programmed during both high-volume manufacturing (HVM) and in the field (IFP) to enable features such as chip identification, post-Si circuit tuning, security key storage, etc. Metal fuse requires an EHV voltage (~1.6-2.1V) and 10s of mA to properly program. In an HVM setting, a high quality HVM supply provides a specific, yield-optimized programming voltage. On the customer platform, this function is performed by an IFP power solution. Prior solutions use either an on-die power switch with generic EHV platform supply, or an on-die power generation, such as CP or LDO [1,2]. The power switch with platform supply typically creates a power sequence requirement between nominal and EHV supplies to avoid EOS, and prevents the technology from choosing a yield-optimized programming voltage since this supply is shared with non-fuse IP. Prior on-die implementations used either a single-stage open-loop (OL) CP, which provides lower voltage head room for yield optimization for different processes or rely on thick-gate (TG) devices, which are incompatible with performance-optimized logic process [1,2]. The proposed solution adds another stage to the single stage CP, and places it in a feedback loop for tunability, and to mitigate EOS from the added stage. An internal resistor reference is used, and bandgap reference is also included where greater PSRR might be required. The CP connects to the fuse macro via power-gate power-switch (PGPS), which switches between CP output and nominal voltage for read. Fig. 1(b) shows the system diagram, including CP with feedback, BGref, and fuse array with PGPS, with fanout to multiple arrays.

**Charge Pump:** The CP is based on Pelliconi voltage doubler [3] and is operated at high frequency (>1 GHz) to maximize current density, minimizing pump area. Power delivery IP typically minimize voltage transients by placing large metal-insulator-metal (MIM) cap on their output. Fuse avoids this cap on its programming supply due to MIM cap reliability constraints on programming voltage, availability concerns, and integration complexity. To minimize voltage ripple without MIM, The CP is split into 8 parallel sub-blocks connected by an embedded ring oscillator clock [4]; Fig. 1(d), 3(c) show the circuit and transient sim of the CP core, respectively. The CP core contains two stages to enable a programming voltage range of 1.6-2.1V and compensate for an input supply which is <1V. Under light load, the second stage addition will produce an ultra-high voltage (~3V) output, exceeding technology EOS limits. Placing the CP in a feedback loop will not only provide voltage tunability for programming, but also prevent EOS within the CP and any downstream circuitry, Fig. 2(a, d). Since fuse does not add MIM on the program supply, frequency, pulse-width, etc. based CP feedback control schemes will not meet accuracy, voltage ripple requirements (under light load condition, these schemes rely on output cap to prevent large voltage overshoot) [5-8]; Fig. 2(b) illustrates the detriment from absent MIM cap with these control schemes. To achieve acceptable accuracy without MIM, this design requires cascade control by LDO. Many cascade control designs only regulate one of the two CP inputs, which limits the output voltage range due to CP minimum operating voltage (Vmin), Fig. 2(c). This design has both CP inputs powered by LDO to achieve the full 1.6-2.1V output voltage range, Fig. 2(d).

**LDO Design and Integration:** The LDO must achieve (1) high gain, (2) high slew rate, to compensate for absent MIM cap and large CP within the feedback loop, and (3) operate at 1V. LDOs have a gain stage and output power stage, and commonly have a buffer stage in between, to produce acceptable bandwidth and slew. The traditional buffer stage will not work at 1V, and low voltage, cascoded flipped voltage follower (CAFVF), are difficult to implement in advanced CMOS process due to gain limitation on the common drain device. In lieu of a buffer stage, this LDO uses the recycled folded cascode (RFC) as a gain stage, for sufficient gain and 2X slew benefit over the traditional folded cascode (FC) [9], and implements a modified 'R-2R' resistor ladder as the feedback circuit, which maximizes CL bandwidth, and eliminates the need for EHV level shifters (LS) within the feedback network, schematics shown in Fig. 3(a, b). Stability is achieved by current buffer compensation, which provides greater bandwidth compared to traditional miller compensation [11]. A performance comparison (Fig. 4(d)) shows the chosen design is the most robust across skew, temperature, and load vs. mentioned alternatives (FC, CAFVF, traditional R ladder); to analyze stability of the CL system, a linearized model is adopted for the CP stages, shown in Fig. 1(a) [10]. Achieved load and line regulation, and transient

simulation for the complete design is shown in Fig. 4(a, b, e). At power-on, a bleeder circuit is momentarily activated to prevent large voltage overshoot. A power-good signal is then generated from the resistor feedback which trips a Schmitt trigger when CP output reaches the prescribed voltage, Fig. 1(c). This signal is synced with SOC clock and polled by firmware during IFP programming setup.

**Power Gate Power Switch:** A PGPS is used to select between the CP output voltage during fuse programming, and nominal supply for fuse read, and to maximize CP to fuse array fanout. Resistor ladders are used as EHV LS to prevent EOS on the thin gate power-switch devices, and are used instead of diode-connected FETs over Vmin concerns during CP power-on. 'Make-before-break' timing is used for all PGPS switches to prevent power supply shorting, Fig. 6(a). When fuse is not active, the power-gate portion of PGPS is enabled, to cut-off all power. With PGPS, the CP can connect to a total of 48K fuses, for a maximum array efficiency of 43.8%.

**Measurement Results:** These circuits have been Si verified on Intel 4 process. Load regulation capability is shown in Fig. 5 for various feedback settings, along with light load output vs. BGref input, showing less than ±3.6% variance, majority coming from BGref. Programming Vmin is also demonstrated (Fig. 6(b)) at 0.95V and expected to improve using up to metal 15 within the design. 100% of units which passed reset successfully completed fuse programming and margin read, at -40C, 30C, and 125C, Fig. 6(c).

**References:** [1] S. H. Kulkarni et al., *IEEE JSSC*, pp. 1003-1008, 2016. [2] Z. Chen *et al.*, *IEEE JSSC*, pp. 993-939, 2017. [3] R. Pelliconi et al., *IEEE JSSC*, pp. 1068-1071, 2001. [4] D. Somasekhar et al., *IEEE JSSC*, pp. 751-758, 2010. [5] Rao A. et al., *IEEE JSSC*, pp. 422-429, 2005. [6] J. A. Starzyk et al., *IEEE TCAS1*, pp. 350-359, 2001. [7] J. Soldera et al., *SBCCI 03*, pp. 177-180, 2003. [8] J. Yi et al., *IEEE ISCAS,* 2008. [9] R. S. Assad et al., *IEEE JSSC,* pp. 2535-2542, 2009. [10] C. Hu et al., *IEEE TPEL,* pp. 2187-2194, 2008. [11] P. Hurst et al., *IEEE TCAS1,* pp. 275-285, 2004.

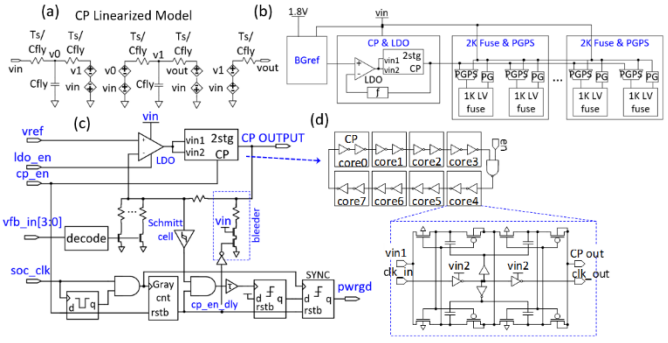



Fig. 1. Linear CP model (a), System Schematic (b), power-up logic (c), CP core schematic (d)

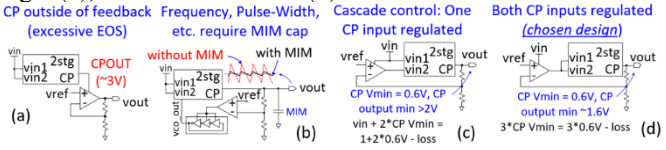



Fig. 2. (a) LDO-CP interaction, showing issues of CP outside of feedback loop, (b) regulation methods requiring MIM, (c) 'partial' vs. (d) 'full' regulation of CP inputs (chosen design).

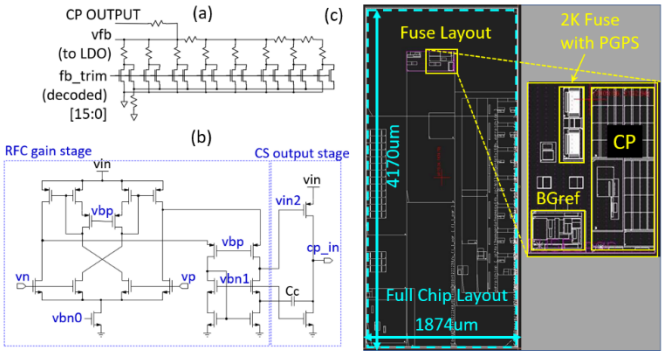



Fig. 3. (a) 'Fast' R-2R resistor ladder circuit, (b) LDO Topology, (c) full die showing Fuse layout

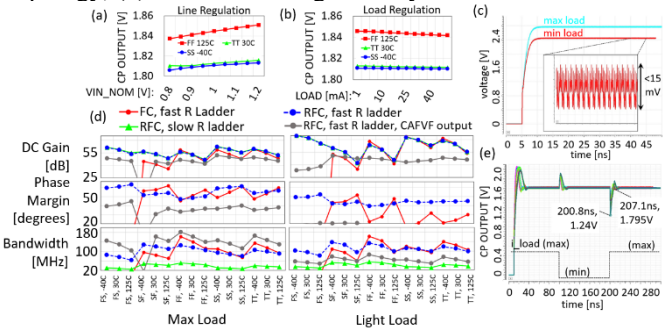



Fig. 4. (a,b) system line and load regulation simulation, (c) CP OL transient simulation, (d) LDO design simulation comparison, (e) system transient simulation

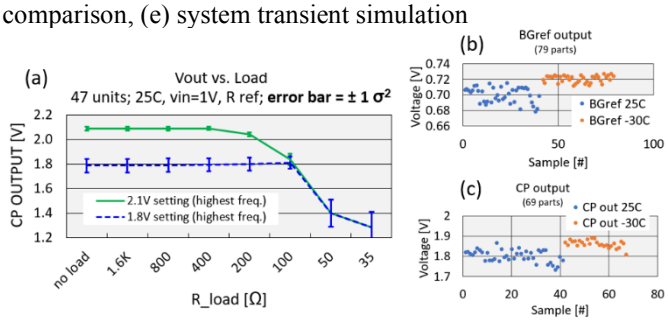
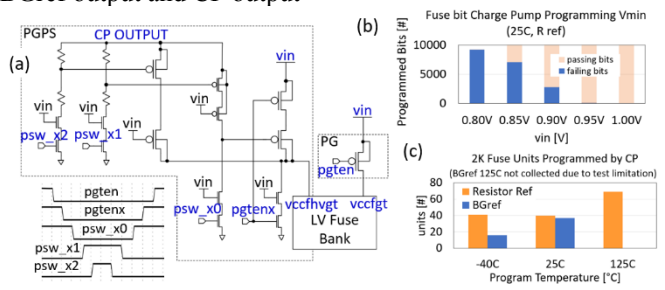



Fig. 5. Si Measurement results: (a) Output vs. Load, (b,c) BGref output and CP output




| (d) | Power Switch with Platform Supply | Thick-Gate LDO [2] | 1V Doubler [1] | Proposed Design |
|---|---|---|---|---|
| Power Sequence (or always-on circuit) Requirement | Yes | Yes | No | No (if BGref is not used) |
| Compatible with Logic Process | Yes | No | Yes | Yes |
| Achieved Program Voltage | Fixed 1.8V | 1.6V – 2.1V+ | <1.6V | 1.6V – 2.1V |
| Program voltage optimized for Yield | No | Yes | Not across processes | Yes |
| Fuse Array Efficiency | - | - | 19% | 43.8% (max with PGPS) |

Fig. 6. (a) PGPS circuit and timing with Fuse bank, Measurement Results: (b) system yield vs. voltage and (c) temperature, (d) design comparison table with prior art