High density NV-SRAM using memristor and selector as technology assist

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Abstract — This work proposes 6T-2R-2S Non-Volatile (NV)-Static Random Access Memory (SRAM) bitcell for state retention applications with minimal sneak path current without incurring active cell area overhead. Various operating modes are described and Vmin/power comparisons with the baseline 6T SRAM are presented.

I. INTRODUCTION

Total power consumption is of paramount importance in energy constrained battery operated sensor nodes and IoT devices. Leakage power dominates the total power consumption in such devices due to very low activity factor. Large capacity embedded SRAMs consume significant leakage power while in retention mode, during the standby mode. For improved energy efficiency 2-level macro with SRAM for active mode storage and an off-chip non-volatile memory (e.g. FLASH) for standby mode storage has been used. However, this approach incurs significant energy and latency overhead due to data movement between SRAM-FLASH arrays during the state store/restore operation. This limits the overall power savings and frequency of activating such state retention modes. To mitigate these issues, multiple Non-Volatile SRAM (NV-SRAM) topologies such as 8T-2R, 7T-1R, 6T-2R (T= Transistor, R= memristor), have been proposed for in-situ state retention using different memristors [1-3]. However, additional transistors in 8T-2R, 7T-1R result in active bitcell area growth while 6T-2R bitcell results in sneak path current across the bitcells. In this work, we propose a novel 6T-2R-2S NV-SRAM bitcell for in-situ state retention featuring (1) zero standby leakage (2) zero active area growth (3) minimal sneak path current.

II. PROPOSED 6T-2R-2S BITCELL

A. *Bitcell configuration*

The proposed bitcell configuration utilizes CMOS 6T-SRAM, 2 memristors (2R) and 2 selector devices (2S) as shown in Fig.1(a). Fig.1(b) and Fig.1(c) show the I-V characteristics of a typical memristor (RRAM in this case) and the selector device (Phase Transition Material (PTM) in this case) respectively. The selector device is designed to exhibit large off-state resistance which reduces the sneak path current across the bitcells. Also, the selector switch can be engineered such that its insulator to metallic phase transition voltage (V_{IMT}) is higher than $V_{CC}/2$. The 2R-2S device stack is accessed through a Control Line (CL) which is shared across all bitcells routed along the bitcell row, parallel to the wordline direction. The 2R-2S stack can be formed over the bitcell storage nodes and can mitigate the SRAM bitcell active area growth.

B. *State store operation*

State retention is accomplished through a specific sequence of voltage signals applied to the control line (CL) (Fig.2.a, 2.d, Table.2). In the first step, the CL node shared along the bitcell row is raised to V_{CC}. This results in a current flow from CL to the node storing '0' (VL) whereas no current flows from CL to the node storing '1' (VR). The selector device transitions into metallic phase when voltage across the PTM exceeds the transition threshold and connects the memristor to the CL node. This initiates current flow in the bitcell from CL→ PTML (metallic phase) → RL → VL → NL → V_{SS}. The voltage developed across RL memristor ($V_{RL} > V_{RESET}$) is large enough to program it to a High Resistance State (HRS). In the next step, the CL node voltage is lowered to V_{SS}. This would result in a current flow from the node storing '1' (VR) to CL. Again, selector device (PTMR) transitions to metallic phase and large current flows from PR→ VR → RR → PTMR (metallic phase) → CL. The voltage developed across RR memristor ($V_{RR} > V_{SET}$) is large enough to program it into a Low Resistance State (LRS).

C. *State restore operation*

Restore operation is performed in three steps. First, all CLs are initialized to $V_{CC}/2$ to make sure PTM devices are in insulating phase to avoid any false programing of the memristors corrupting the stored resistance state. Next, as the bitcell-V_{CC} is ramped up, the SRAM storage nodes (VL and VR) are initialized with random values. In the second step, the WL is triggered with both bitlines at Vss. This would result in forcing '0' on both storage nodes. Note that CL is held at $V_{CC}/2$ to maintain the PTM selector in the insulating phase and isolate the 2R-2S stack (especially the LRS memristor) which would otherwise increase the crowbar current significantly during bit-cell V_{CC} ramp up. In the third step, as soon as WL is transitioned low, the CL is also transitioned to Vss. With bitcell-V_{CC} enabled, both bitcell PMOS transistors start charging VL and VR nodes towards V_{CC}. However, one of the sides is connected to V_{SS} (through CL) with low resistance state of RRAM and other side is connected to V_{SS} (through CL) with high resistance state of RRAM. This difference in the RRAM resistances results in the differential voltage development across the storage nodes (VL and VR) which then resolve to full-rail voltage due to positive feedback effect of the cross coupled inverters. Once the storage nodes restore the RRAM states, the CL is maintained at $V_{CC}/2$ to isolate 2R-2S stack from the subsequent active SRAM mode operations. Thus, row wise sequential restore mechanism with unselected CLs held at $V_{CC}/2$ can mitigate the peak current and IR drop along the bitcell-V_{CC} grid at the expense of increased restore time.

D. *Active SRAM – mode*

In this mode, the state retention component (2R-2S) is kept inactive to minimize the sneak path among bitcells and to prevent any disturbance to the subsequent active mode SRAM operations (read/write). All CLs are biased at $V_{CC}/2$ (Fig. 2.e) to maintain both selector devices (PTML, PTMR) in the insulating phase ($V_{IMT} > V_{CC}/2$).

III. SIMULATION RESULTS

Baseline 1-1-1 fin 6T SRAM bitcell and the proposed 6T-2R-2S bitcell are compared using 7nm predictive FinFET, and memristor /selector Verilog-A models (Table 1). Zero standby mode leakage attribute in the 6T-2R-2S bitcell can be utilized to lower FinFET Vt to achieve lower active-Vmin (minimum operating voltage). The 6T-2R-2S bitcell with 50mV reduced Vt shows 100(120) mV lower read(write) Vmin (@1e-6 P_{FAIL}) compared the baseline 6T SRAM requiring high Vt transistors for leakage reduction (Fig.4.a, 4.b). Lower active Vmin in the 6T-2R-2S bitcell results in lower total power for the activity factor (α) below 18%, making it very attractive for memory leakage power sensitive IoT designs (Fig. 5.a). Power savings increase for large arrays for small activity factors (Fig. 5.b). Table 3 compares 6T-2R-2S bitcell with prior approaches.

ACKNOWLEDGMENTS

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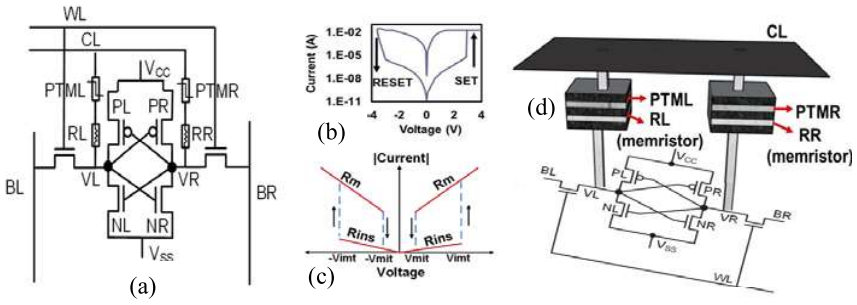


Fig. 1 (a) Proposed 6T-2R-2S SRAM bitcell with memristor and selector devices (b) Memristor (Resistive-RAM) (c) selector (Phase Transition Material) I-V characteristics (d) 3D conceptual view of the proposed 6T-2R-2S bitcell. The non-volatile memory stack can be fabricated in BEOL process.

Simulation technology node	7nm Predictive FinFET models [4]
Simulation tool	HSPICE
SRAM design	All 1 fin transistor SRAM
Memristor specifications	SET/RESET – 0.6/-0.6 ; ratio HRS/LRS - 100; Verilog-A model – [5]
Selector specifications	V_{IMT}/V_{MIT} – 0.5/0.04 ; ratio met/ins – 10^4 ; Verilog-A model – [6]

Table 1: FinFET, memristor and selector models

Mode	CL	WL	BL/BR
SRAM mode	$V_{CC}/2$	Normal operation	Normal operation
Store-0	V_{CC}	V_{SS}	Floating
Store-1	V_{SS}	V_{SS}	Floating
Restore – step 1	$V_{CC}/2$	V_{SS}	Floating
Restore – step 2	$V_{CC}/2$	> V_{CC}	V_{SS}
Restore – step 3	V_{SS}	V_{SS}	Floating

Table 2: Bitcell operating conditions

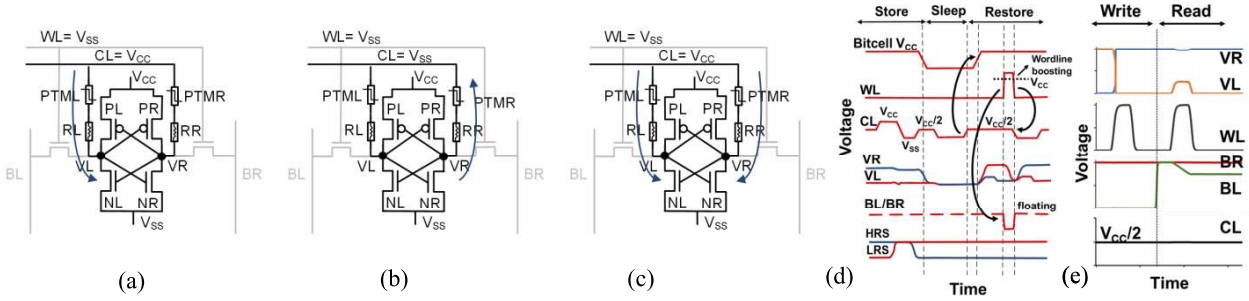


Fig. 2 Schematic showing the current flow direction in (a) & (b) State store operation (c) State restore operation (d) Timing diagram for store/restore operation (e) Timing diagram for SRAM mode. CL is held at $V_{CC}/2$ for minimal sneak path current.

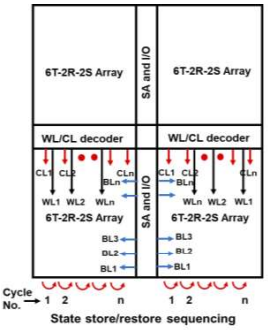


Fig.3: 6T-2R-2S SRAM array floorplan: CLs can be routed along the wordline and can be activated sequentially to limit the peak current and IR drop during store/restore operations.

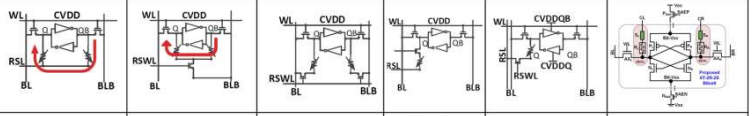
Topology	6T2R[3]	7T2R[7]	8T2R[1]	7T1R[8]	7T1R[2]	6T-2R-2S (This Work)
Cell Schematic						
Restore Method	Differential R Sensing	Differential R Sensing	Differential R Sensing	Single ended sensing	Initialization-and-overwrite	Differential R Sensing
Restore Yield	High	High	High	Low	High	High
SRAM mode short circuit current	Yes	Yes	No	No	No	No

Table 3. 6T-2R-2S bitcell comparison with prior NV-SRAM topologies

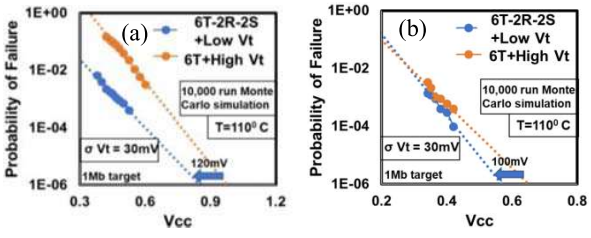


Fig.4 (a) Write Vmin improvement for the proposed 6T-2R-2S bitcell with 50mV reduced Vt compared to the baseline 6T SRAM bitcell which would require higher Vt to minimize leakage during retention mode. Write failure is quantified as the number of bit flips for a constant wordline pulse-width (500ps) (b) Read Vmin improvement for the proposed 6T-2R-2S bitcell with 50mV Vt reduction. Read failure is quantified as the number of bit flips during a read operation for a constant wordline pulse width of 500ps employing wordline underdrive (WLUD) of 0.8Vcc (110^{0}C used for worst case analysis).

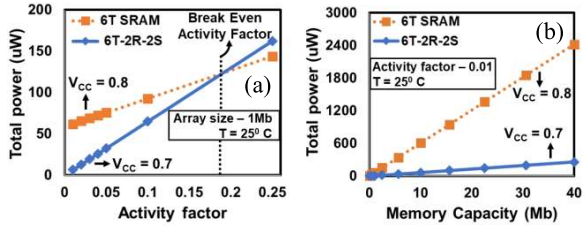


Fig.5 (a) Total power consumption variation with activity factor for the baseline 6T SRAM* using high Vt FinFETs and the proposed 6T-2R-2S SRAM$ using 50mV lower Vt FinFETs operating at 100mV lower V_{CC}. Breakeven activity factor is 0.18 beyond which 6T-2R-2S bitcell array consumes higher power than 6T bitcell array (b) Total power consumption as a function of memory capacity.

* 6T SRAM $P_{Total} = \alpha*(P_{active\_dyn\_0.8V} + P_{active\_ret\_0.8V}) + (1- \alpha)*P_{ret\_0.32V}$

$ 6T-2R-2S $P_{Total} = \alpha*(P_{active\_dyn\_0.7V} + P_{active\_ret\_0.7V}) + \alpha*(P_{store\_0.7V} + P_{restore\_0.7V})$