

Jaydeep P. Kulkarni

Assistant Professor of Electrical and Computer Engineering

Fellow of AMD Chair in Computer Engineering, Fellow of Silicon Labs Chair in Electrical Engineering

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Group: Circuit Research Lab, Website: <http://sites.utexas.edu/CRL/>

Research Interests:

Machine learning hardware accelerators, In-memory Computing, Neuromorphic computing, Emerging nano-devices, heterogenous and 3D integrated circuits, hardware security and cryogenic computing

Education:

- **Purdue University**, West Lafayette, IN
Ph.D. Electrical & Computer Engineering, 2009
Dissertation: Low Voltage Robust Memory Circuit Design, Advisor: Prof. Kaushik Roy
- **Indian Institute of Science (IISc)** Bangalore, India
M. Tech. in Electronics Design and Technology, 2004
- **College of Engineering Pune (COEP)**, University of Pune, India
B. E. in Electronics and Telecommunication Engineering, 2002

Work Experience:

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|---|--------------------|
| • Assistant Professor, The University of Texas at Austin, TX | August'17- Present |
| • Senior Staff Research Scientist, Intel Labs, Hillsboro, OR | May'09 – July'17 |
| • Research Assistant, Purdue University, W. Lafayette, IN | Jul'05 – Apr'09 |
| • Graduate Intern, Circuit Research Lab, Intel, Hillsboro, OR | May'08 – Aug'08 |
| • Graduate Intern, Technology Manufacturing Group, Intel, Hillsboro, OR | May'07 – Aug'07 |
| • Design Engineer, Cypress Semiconductor, Bangalore, India | Jul'04 – May'05 |
| • Graduate Researcher, Indian Institute of Science, Bangalore, India | Jul'02 – May'05 |
| • Graduate Intern, Texas Instruments, Bangalore, India | Jan'04 – May'04 |
| • Undergraduate intern, Cirrus Logic, Pune, India | Jan'01 – Apr'02 |

Honors and Awards:

1. Fellow of Silicon Labs chair in Electrical Engineering, University of Texas at Austin (Fall 2020-)
2. Fellow of AMD chair in Computer Engineering, University of Texas at Austin (2017-present)
3. Micron Foundation Faculty Awards (2019, 2020)
4. Industrial Distinguished Lecturer for IEEE Circuits and Systems (CAS) Society (2017)
5. SRC Mahboob Khan Outstanding Industry Liaison Award (2015)
6. IEEE Transactions on VLSI Systems Best Paper Award (2015)
7. IEEE Senior Member (2015)
8. Intel Corporation- 7 Divisional Recognition Awards (2009-2017)

9. Intel Corporation- 4 Patent Recognition Awards (2009-2017)
10. Outstanding Doctoral Dissertation Award by Purdue University's School of ECE (2010)
11. Intel Foundation Ph.D. Fellowship Award (2008-09)
12. Two SRC Inventor Recognition Awards (2008)
13. Best paper in session Award at SRC TECHCON (2008)
14. ISLPED Design Contest Award (2008)
15. Best M.Tech Student Award, CEDT Design Medal by IISc Bangalore (2004)
16. Pune University Junior and Senior Year Top-5 (Summa Cum Laude) Award (2001, 2002)
17. National Talent Search (NTS) Scholarship by the Government of India (1996-2002)

Professional Activities:

1. Chair, IEEE CASS/SSCS Central Texas Chapter (2020-present), Vice-chair (2018-19)
2. Associate Editor, IEEE Solid State Circuits Letters, (2018-present)
3. Associate Editor, IEEE Transactions on VLSI systems, (2015-present)
4. Guest Editor, IEEE Micro, Special Issue on Circuits November/December 2020
5. Member of IEEE CAS Society – VLSI systems and applications technical committee (2015-present)
6. Senior Member – IEEE, Solid State Circuits, Circuits and Systems, and Electron Device Society
7. Member- ACM, Special Interest Group on Design Automation (SIGDA)
8. IEEE Conference Organization –
 - General Co-chair, 2018, International Symposium on Low Power Electronics Design (ISLPED)
 - Technical program co-chair, 2017 International Symposium on Low Power Electronics Design
9. IEEE Conference Technical Program Committee Member –
 - AI Circuits and Systems Conference (AICAS, 2020)
 - Custom Integrated Circuits Conference (CICC, 2019-present)
 - International Conference on Computer-Aided Design (ICCAD, 2018-present)
 - Design Automation Conference (DAC, 2018-2019)
 - International Conference on VLSI Design (VLSID, 2019)
 - Dallas Circuits and Systems Conference (DCAS, 2018)
 - International Symposium on Quality Electronics Design (ISQED, 2019)
 - Asian Solid State Circuits Conference (A-SSCC, 2014-2017)
 - International Conference on Computer Design (ICCD, 2017)
 - International Symposium on Circuits and Systems (ISCAS, 2016)
 - International Symposium on Low Power Electronics Design (ISLPED, 2013-2016)
 - Asian Symposium on Quality Electronics Design (ASQED, 2010-13)
10. IEEE Conference Service:
 - Best paper award committee member, AI Circuits and Systems Conference, 2020
 - Best paper award committee member, Custom Integrated Circuits Conference, 2020
 - Best paper award committee member, VLSI Design Conference, India 2018
11. Industrial Liaison/Associate (2009-2017)–
 - Stanford - SystemX Alliance, Non-volatile Memory Technology Research Initiative (NMTRI)

- Semiconductor Research Corporation (SRC) – Integrated Circuits and Systems Track
- NSF program on Visual Cortex on Silicon (Penn State, MIT, USC, UCSD, UCLA, Stanford, Notre Dame, Univ. of Pittsburgh, York College)
- STARnet Research - Systems On Nanoscale Information fabriCs Center (SONIC); Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN); Center for Low Energy Systems Technology (LEAST)
- Technical Champion, Intel Academic Research Office program on “Post-CMOS Circuits and Architectures”
- Reviewer: IEEE Journal of Solid State Circuits, IEEE Transactions on Circuits and Systems – I and II, IEEE Transactions on VLSI Systems, VLSI Circuit Symposium, IEEE Micro, IEEE ISCA, IEEE Transactions on Computers, IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, ACM Journal on Emerging Technologies in Computing

Current students:

Ph.D.

1. Can Ni (Joined Spring'2020-)
2. Shanshan Xie (Joined Spring'2019-)
3. Rishabh Sehgal (Joined Fall'2019-)
4. Stafford Hutchins (Joined Fall'2019-)
5. Rahul Mathur (Joined Fall'2018-)
6. Jacob Rohan (Joined Fall'2018-)
7. Meizhi Wang (Joined Fall'2018-)
8. Sai Subrahma Nibhanupudi (joined Fall'2017-) (Co-advised by Prof. Banerjee)

M.S.

9. Siddhartha Raman Sundara Raman (Joined Fall'2019-)
10. Kashyap Mattoo (Joined Fall'2019-)
11. Yunfei Sun (Joined Fall'2019-)

Graduated students:

Ph.D.

1. Aseem Sayal, Ph.D., Spring 2020 (Co-advisor: Prof. S.V. Sreenivasan), Thesis Title: “Energy-Efficient Machine Learning Accelerators on Reconfigurable Design Platforms”

M.S.

1. Shirin Fatima, M.S. Spring 2019, Thesis Title: “All-Digital Time-Domain CNN Engine for Energy Efficient Edge Computing”
2. Naman Maheshwari, M.S. Spring 2019, Thesis Title: “Estimating the Minimum Bit-Width Precision for Stable Deep Neural Networks Utilizing Numerical Linear Algebra”
3. Wei Li, M.S. Spring 2019, Thesis Title: “An Energy Efficient Compute-in-Memory SRAM for Low Power CNN based Machine Learning Application”

Thesis Committee Membership

UT Austin:

1. Paras Ajay, Ph.D. Mechanical Engineering Graduation: Fall 2019
2. Heechai Kang, Ph.D., Electrical and Computer Engineering, Graduation: Fall 2019
3. Crystal Baker, Ph.D., Mechanical Engineering, Expected Graduation: 2020
4. Xin Zhao, Ph.D., Electrical and Computer Engineering, Spring 2020

Outside of UT Austin:

5. Ankit Sharma, Ph.D. ECE, Purdue University, March 2018
6. Kenneth Ramclam, M.S. CSE, University of South Florida, March 2015

Thesis Examiner

7. Sukarn Agarwal, Ph.D., Indian Institute of Technology (IIT) Guwahati, India, Fall 2019
8. Vanita Agarwal, Ph.D., Savitribai Phule Pune University, India, Spring 2020
9. Amit Kumar Khade, Ph.D., Savitribai Phule Pune University, India, Spring 2020
10. Satyajit Mohapatra, Ph.D., Indian Institute of Technology (IIT) Gandhinagar, India, Summer 2020

Teaching:

1. EE 316, Digital Logic Design, Fall 2020 (Under Graduate required course)
2. EE 382.8M, VLSI-II, Spring 2020 (Graduate course)
 - Students Enrolled: 15, Instructor rating: 4.6/5, course rating: 4.6/5
3. EE 316, Digital Logic Design, Fall 2019 (Under Graduate required course)
 - Students Enrolled: 93, Instructor rating: 3.7/5, course rating: 3.5/5
4. EE 382.8M, VLSI-II, Spring 2019 (Graduate course)
 - Students Enrolled: 26, Instructor rating: 4.8/5, course rating: 4.6/5
5. EE 382.8M, VLSI-II, Spring 2018 (Graduate course)
 - Students Enrolled: 22, Instructor rating: 4.3/5, course rating: 4.0/5
6. EE 464, Senior Design project, Fall 2017-Fall 2018, Spring 2019, Fall 2019

University Service:

1. Selection Panellist for UT competition sponsored by Office of Vice President for Research, 2019
2. Junior faculty hiring committee, ECE Department, UT Austin, 2018-2020
3. Colloquium Series committee, ECE Department, UT Austin, 2019-2020
4. Integrated Circuits and Systems graduate admissions committee, 2017-present

Student Engagement:

1. Career panel presentation on faculty job preparation, Graduate Engineering Council (GEC), Cockrell School of Engineering, Fall 2019
2. Co-ordinator for the Integrated circuits area for incoming graduate student site visit, Spring 2019
3. Student technical area advising, HKN Technical Area night, Spring 2018

K-12 student mentoring:

1. Parth Shroff, LASA High School, Austin (Fall'2018-2019)

Invited Seminars, Keynotes, Short Course, and Tutorials:

- T1. **Workshop**, “Analog Computing Technologies and Circuits for Efficient Machine Learning Hardware”, VLSI Symposia on Technology and Circuits, June 2020
- T2. “All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy-Efficient Edge Computing” Silicon Labs, Austin, TX, November 2019
- T3. **Invited Talk**, “High Density Non-Volatile SRAM using RRAM and Selector as Technology Assist”, IEEE Non-Volatile Memory Technology Symposium (NVMTS), Durham, NC, October 2019
- T4. “All-Digital Time-Domain CNN Engine Using Bi-Directional Memory Delay Lines for Energy-Efficient Edge Computing” Qualcomm, Raleigh, NC, October 2019
- T5. **Keynote Talk** “Energy Efficient Embedded Memories in Advanced CMOS: Trends and Prospects”, VLSI Design and Test Conference, Indian Institute of Technology (IIT), Indore, India, July 2019
- T6. **Invited Talk** “Embedded Memories in Advanced CMOS: Trends and Opportunities in ML/AI Accelerators”, Indian Institute of Technology (IIT) Bombay, India, July 2019
- T7. “Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators” Samsung R&D Institute, Bangalore, India, July 2019
- T8. “Embedded memories in advanced CMOS: Trends and Prospects” Qualcomm Bangalore, India, July 2019
- T9. “Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators” ARM, Bangalore, India, July 2019
- T10. **Invited Talk** “Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators”, IEEE Chapter University Visvesvaraya College of Engineering (UVCE), Bangalore, India, July 2019
- T11. **Invited Talk** “Threshold switching selector devices for energy efficient integrated circuits”, IEEE EDS/SSCS Bangalore Chapter, Indian Institute of Science (IISc), Bangalore, India, July 2019
- T12. **Keynote Talk** “Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators”, IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, India, July 2019
- T13. **Invited Talk** “Embedded memories in advanced CMOS: Trends and Opportunities in ML/AI Accelerators”, College of Engineering Pune (COEP), India, July 2019
- T14. **Invited short course**, “Circuit Technologies for efficient in-memory computing” at International Memory Workshop (IMW), Monterey, CA, May 2019
- T15. **Invited Talk**, “Phase transition material assisted energy efficient CMOS design” Workshop on microelectronics and Electron Devices (WMED), IEEE Boise Chapter, Boise, ID, April 2019
- T16. “Phase transition material assisted energy efficient CMOS design” Silicon Labs, Austin, TX, August 2018
- T17. “Phase transition material assisted energy efficient CMOS design” Intel, Hillsboro, OR, July 2018
- T18. “Energy Efficient memories design for the compute continuum and beyond” Cirrus Logic, Austin, TX June 2018
- T19. “Phase transition material assisted energy efficient SRAM design” Texas Instruments, Dallas, TX, May 2018

- T20. "Energy Efficient memories design for the compute continuum and beyond" AMD, Austin, TX April 2018
- T21. "Energy Efficient memories design for the compute continuum and beyond" ARM, Austin, TX February 2018
- T22. "Energy Efficient memories for ultra-low power IoT applications", Silicon Labs, Austin, TX, November 2017
- T23. "Energy Efficient memory design for the compute continuum and beyond" UT Austin ECE Colloquium, November 2017
- T24. "Energy Efficient memory design for the compute continuum and beyond" IEEE Santa Clara Valley Circuits and Systems Society, May 2017
- T25. "Energy Efficient Memory Circuits: From IoT to Exascale Systems and Beyond", University of Southern California, April 2016
- T26. "Embedded Memory Design for Future Technologies: Challenges, Solutions and Applications" Tutorial at Design, Automation and Test Conference (DATE), March 2015
- T27. "Process Adaptive Sub-Threshold Design", Defense Advanced Research Projects Agency (DARPA), Washington D.C., October 2008
- T28. "Write Current Reduction in MRAMs using Tiny Spiral Inductors", 2008 International Solid State Circuits Conference (ISSCC), Student Forum, February 2008
- T29. "Process Variation Tolerant SRAM Design for Ultra-Low Voltage Applications", Indian Institute of Science, Bangalore, January 2008
- T30. "Low-Power Robust CMOS Circuits for Scaled Technologies", SRC Integrated Circuits and Systems Sciences, University of Massachusetts, Amherst, October 2007

Panels:

- PN1. "Security and Trust as New Dimensions in Analog / RF Design Space Exploration" TxACE STARS: TxACE Workshop on Secure and Trusted Analog/RF Systems, UT Dallas, May 2018
- PN2. "Magnetics, Logic and Memories Proposal Panel", NSF, Washington D.C., March 2018

Patents:

- P1. S.V. Sreenivasan, A. Mallavarapu, **J. P. Kulkarni**, S. Banerjee and M. Watts, "Three-dimensional SRAM architectures using catalyst influenced chemical etching" filed USPTO
- P2. S.V. Sreenivasan, P. Ajay, A. Sayal, M. McDermott, **J. Kulkarni**, "Novel nanofabrication and design techniques for 3D ICs, and Configurable ASICs" filed USPTO
- P3. S.V. Sreenivasan, P. Ajay, A. Sayal, A. Ovadia, M. McDermott, **J. Kulkarni**, and S. Shrawan, "Nanoscale aligned 3D stacked integrated circuit" filed USPTO 17/62609891, PCT/ WO2019126769A1
- P4. A. Mora, **J. Kulkarni**, A. Thaploo, M. Khellah, "Current steering level-shifter", US patent 10666259
- P5. A. Bonetti, **J. P. Kulkarni**, C. Tokunaga, M. Cho, P. Meinerzhagen, and M. Khellah, "Voltage level shifter monitor with tunable voltage level shifter replica circuit" US patent 10,243,563
- P6. **J. P. Kulkarni**, V. De and M. Khellah, "Aging aware dynamic keeper apparatus and associated method", US Patent 10,269,419

- P7. **J. P. Kulkarni**, and M. Khellah, "Low swing bitline for sensing arrays" US Patent 10,199,080
- P8. M. Cho, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, and J. Tschanz "Adaptive voltage system for aging guard-band reduction" US Patent 10,199, 091
- P9. M. Cho, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, and J. Tschanz "Retention minimum voltage determination techniques" USPTO 15373048
- P10. A. Thaploo, **J. Kulkarni**, B. Borole, A. Appu, A. Koker, K. Sinha, W. Fu, "System, apparatus and method for reducing voltage swing on an interconnect" filed, USPTO 15/488,673
- P11. **J. P. Kulkarni**, Y. Shim, and P. Meinerzhagen, "Apparatus and method for reducing di/dt" filed USPTO 15/163,494
- P12. **J. P. Kulkarni**, Y. Shim, P. Meinerzhagen, M. Khellah "Bi-directional, multi-mode charge pump" US Patent 10,014,767
- P13. **J. P. Kulkarni**, I. Rajwani, and E. Donkoh, "Reduced swing bitline apparatus and method" US Patent 9,947,388
- P14. F. Sheikh, A. Sharma, and **J. P. Kulkarni**, "Fast Fourier transform architecture" filed PCT/US2015/66963
- P15. H. Bonakdar, **J.P. Kulkarni**, "Register files including distributed capacitor circuit blocks", US Patent 9767858
- P16. Y. Shim, **J. P. Kulkarni**, P. Meinerzhagen, and M. Khellah, "di/dt reduction technique during primary power gate wake-up", US Patent 9755631
- P17. **J. P. Kulkarni**, "Memory device including encoded data-line multiplexer" US Patent 9905278
- P18. **J. P. Kulkarni**, P. Kolar, A. Sharma, S. Chatterjee, K. Subramanian, F. Sheikh, W. H. Ma, "Capacitive wordline boosting" filed USPTO 14/752464
- P19. **J. P. Kulkarni**, A. Ravi, D. Somasekhar, G. Balamurugan, S. Shekhar, T. Musah, and T.-C. Hsueh "Digitally trimmable integrated resistors using resistive memory devices" US Patent 9589615
- P20. A. Trivedi, **J. P. Kulkarni**, D. Somasekhar, M. Khellah, C. Tokunaga, J. Tschanz, "Current Steering Level Shifter" US Patent 9621163
- P21. A. Trivedi, **J. P. Kulkarni**, C. Tokunaga, M. Khellah, J. Tschanz, "Voltage level shifter circuit" US Patent 9385722
- P22. **J. P. Kulkarni**, A. Thaploo, I. Rajwani, K. Koo, E. Karl, M. Khellah, "Assist circuit for memory" US Patent 9355694
- P23. **J. P. Kulkarni**, P. Meinerzhagen, D. Somasekhar, J. Tschanz, and V. De "Apparatus for charge recovery during low power mode" US Patent 9948179
- P24. **J. P. Kulkarni**, B. Geuskens, J. Tschanz, V. De and M. Khellah "Methods and systems to selectively boost an operating voltage of, and controls to an 8T bit-cell array and/or other logic blocks" US Patent 9,633,716
- P25. **J. P. Kulkarni**, K. Bowman, J. Tschanz and V. De "Resilient register file circuit for dynamic variation tolerance and method of operating the same" US Patent 9329918
- P26. J. Nasrullah, K. Kwan, **J. P. Kulkarni** and M. Khellah "Method and systems for energy efficiency and energy efficiency and energy conservation including entry and exit latency reduction for low power states", US Patent 9665144

- P27. I. Rajwani, S. Damaraju, N. Cooray, M. Khellah and **J. P. Kulkarni** "Memory array with extended write operation" USPTO/12642444
- P28. P. Meinerzhagen, **J. P. Kulkarni**, M. Khellah, C. Dray, D. Somasekhar, J. Tschanz and V. De "Apparatus for dual purpose charge pump" US Patent 9,230,636
- P29. **J. P. Kulkarni**, M. Khellah, J. Tschanz, B. Geuskens, and V. De "Apparatus for reducing write minimum supply voltage for memory" US patent 9,153,304
- P30. A. Raychowdhury, **J. P. Kulkarni**, and J. Tschanz "Multi-supply sequential logic unit" US patent 8,901,819
- P31. **J. P. Kulkarni**, D. Somasekhar "Low voltage swing repeater" US patent 8,847,633
- P32. C. Wilkerson, A. Alameldeen, and **J. P. Kulkarni**, "Adaptive self-repairing cache" US patent 8,719,502
- P33. **J. P. Kulkarni**, D. Somasekhar, J. Tschanz and V. De "Circuits and methods for memory" US patent 8488390
- P34. **J. P. Kulkarni**, M. Khellah, B. Geuskens, A. Raychowdhury, T. Karnik and V. De "Memory write operation methods and circuits" US patent 8467263
- P35. **J. P. Kulkarni** and K. Roy "Static random access memory cell and devices using the same", US patent 7952912
- P36. **J. P. Kulkarni** and K. Roy "Memory cell with built-in process variation tolerance" US patent 7672152

Publications:

h-index = 22, total citations = 3046 (Google Scholar, 20th August 2020)

Book / Book Chapters:

- B1. **J. P. Kulkarni**, J. Tschanz and V. De, "Energy-Efficient Volatile Memory Circuits" in Enabling the Internet of Things - from Circuits to Networks, Editor: Prof. Massimo Alioto, Springer, New York, ISBN: 978-3-319-51480-2
- B2. **J. P. Kulkarni** and K. Roy, "Technology/Circuit Co-design for III-V FETs" pp. 423-442, in Fundamentals of III-V Semiconductor MOSFETs, Springer, New-York 2010, ISBN: 978-1-4419-1546-7

Journal Papers:

- J1. A. Sayal, P. Ajay, M. McDermott, S.V. Sreenivasan and **J. P. Kulkarni**, "M2A2: Microscale Modular Assembled ASICs for High-Mix, Low-Volume, Heterogeneously Integrated Designs" IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (**TCAD**) (accepted, preprint available on IEEExplore)
- J2. A. Sayal, S. Fatima, S. S. Teja Nibhanupudi, and **J. P. Kulkarni**, "A 12.08 TOPS/W All-Digital Time-Domain CNN engine using Bi-directional Memory Delay Lines for Energy Efficient Edge Computing", IEEE Journal of Solid State Circuits (**JSSC**), pp. 60-75, Vol. 55, No. 1, January 2020, Invited paper for Special issue on ISSCC 2019
- J3. P. Meinerzhagen, C. Tokunaga, A. Malavasi, V. Vaidya, A. Mendon, D. Mathaikutty, **J. Kulkarni**, C. Augustine, M. Cho, S. Kim, G. Matthew, R. Jain, J. Ryan, C.-C. Peng, S. Paul, S. Vangal, B. P. Esparza, L. Cuellar, M. Woodman, B. Iyer, S. Maiyuran, G. Chinya, X. Zou, Y. Liao, K. Ravichandran, H. Wong, M. Khellah, J. Tschanz, and V. De, "An Energy-Efficient Graphics Processor in 14nm Tri-Gate CMOS Featuring Integrated Voltage Regulators for Fine-Grain DVFS,

Retentive Sleep, and V_{MIN} Optimization” invited to IEEE Journal of Solid State Circuits (**JSSC**) Special issue on ISSCC 2018, pp. 144-157, Vol. 54, No. 1, January 2019

- J4. S. Motaman, S. Ghosh, and **J. Kulkarni**, “VFAB: A Novel 2-Stage STT RAM Sensing Using Voltage Feedback and Boosting” IEEE Transactions on Circuits and Systems-I (**TCAS-I**), pp. 1919-1928, Vol. 65, issue-6, June 2018
- J5. S. Motaman, S. Ghosh, and **J. Kulkarni**; “Impact of Process Variation on Self-Reference Sensing Scheme and Adaptive Current Modulation for Robust STT RAM Sensing” ACM Journal on Emerging Technologies in Computing Systems (**JETC**), pp. 1-17, Vol. 14, issue-1, October 2017
- J6. **J. P. Kulkarni**, J. Keane, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, “5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology” IEEE Journal of Solid State Circuits (**JSSC**) (special issue on ISSCC 2016), pp. 229-239, Vol. 52, No. 1, January 2017
- J7. M. Cho, S. Kim, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, V. De, “Post-Silicon Voltage Guard-Band Reduction in a 22nm Graphics Execution Core Using Adaptive Voltage Scaling and Dynamic Power Gating” accepted to IEEE Journal of Solid State Circuits (**JSSC**), (special issue on ISSCC 2016), pp. 50 – 63, Vol. 52, No. 1, January 2017
- J8. S. Srinivasa, A. Aziz, N. Shukla, X. Li, J. Sampson, S. Datta, J. P. Kulkarni, V. Narayanan, and S. Gupta, “Correlated Material Enhanced SRAMs with Robust Low Power Operation” IEEE Transactions on Electron Devices (**TED**), pp. 4744- 4752 Vol. 63, No. 12, December 2016
- J9. A. Sharma, A. A. Goud, J. P. Kulkarni, and K. Roy, “Source-underlapped GaSb-InAs TFETs with applications to Gain Cell Embedded DRAMs” IEEE Transactions on Electron Devices (**TED**), pp. 2563-2569, Vol 63, No. 6, June 2016
- J10. **J. P. Kulkarni**, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De, “A 409 GOPS/W Adaptive & Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin & Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature & Aging, IEEE Journal of Solid State Circuits (**JSSC**), pp. 117-129, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015
- J11. S. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. Ryan, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, and V. De, “Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally Controlled Fully Integrated Voltage Regulator” IEEE Journal of Solid State Circuits (**JSSC**), pp. 18-30, Vol. 51, No. 1, January 2016 Special issue on ISSCC 2015
- J12. R. Jain, B. Geuskens, M. Khellah, S. Kim, **J. Kulkarni**, J. Tschanz and V. De, “A 0.45-1V Fully Reconfigurable Switched Capacitor step down DC-DC converter with High Density MIM Capacitor in 22nm Tri-gate CMOS” IEEE Journal of Solid State Circuits (**JSSC**), pp. 1-11, vol. 49, No. 4, April 2014
- J13. R. Pandey, V. Saripalli, **J. P. Kulkarni**, S. Datta, “Impact of Single Trap Random Telegraph Noise on Heterojunction TFET SRAM Stability”, IEEE Electron Device Letters (**EDL**), pp. 393-395, Vol 35, No. 3, March 2014
- J14. S. Gupta, **J.P. Kulkarni**, and K. Roy, “Tri-Mode Independent Gate FinFET based SRAM with Pass Gate Feedback: Technology-Circuit Co-design for Enhanced Cell Stability”, IEEE Transactions on Electron Devices (**TED**), pp. 3696-3704, vol. 60, No. 11, November 2013
- J15. A. R. Alameldeen, N.S. Kim, S. M. Khan, H. R. Ghasemi, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, “Improving memory reliability power and performance using mixed cell designs” Intel Technology Journal (**ITJ**), pp. 36-53, vol. 17, issue 1, 2013

- J16. S. Gupta, **J.P. Kulkarni**, S. Datta and K. Roy, "Heterojunction Intra-band Tunnel (HIBT) FETs for Low Voltage SRAMs", IEEE Transactions on Electron Devices (**TED**), pp. 3533-3542, vol. 59, No. 12, December 2012
- J17. **J. P. Kulkarni** and K. Roy, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design" IEEE Transactions on VLSI systems (**TVLSI**), pp. 319-332, vol. 20, No. 2, February 2012 (**2015 IEEE TVLSI best paper award, Top-25 most downloaded TVLSI manuscript for the year 2012**)
- J18. **J. P. Kulkarni**, A. Goel, P. Ndai and K. Roy, "Read-Disturb-Free, Differential Sensing 1R/1W Port 8T Bitcell Array" IEEE Transactions on VLSI systems (**TVLSI**), pp. 1727-1730, Vol. 19, Issue: 9, September 2011
- J19. M. Meterelliyoz, P. Song, F. Stellari, **J. P. Kulkarni** and K. Roy, "Characterization of Random Process Variations using Ultra Low Power High Sensitivity, Bias Free Sub-threshold Process Sensor" IEEE Transactions on Circuits and Systems-I (**TCAS-I**), pp. 1838-1847, Vol. 57, Issue:8, August 2010
- J20. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits" IEEE Transactions on Magnetics (**TMAG**), pp. 1898-1901, vol. 46, No. 6, June 2010
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- J22. **J. P. Kulkarni** and K. Roy, "Technology Circuit Co-design for Ultra-Fast InSb Quantum Well Transistors", IEEE Transactions on Electron Devices (**TED**), pp. 2537-2545, Vol. 55, October 2008
- J23. Q. Cao, H.-S. Kim, N. Pimparkar, **J. P. Kulkarni**, C. Wang, M. Shim, K. Roy, M. A. Alam and J. A. Rogers, "Medium Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates" pp. 495-500, **Nature**, vol. 454, 24th July 2008
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- J25. S. Kibey, **J. P. Kulkarni** and P. Sarode "A fast LSF search algorithm based on inter-frame correlation in G.723.1" EURASIP Journal of Applied Signal Processing, Vol. 11, July 2004

Conference Papers:

- C1. **J. P. Kulkarni**, A. Malavasi, C. Augustine, C. Tokunaga, J. Tschanz, M. M. Khellah, V. De, "Low Swing and Column Multiplexed Bitline Techniques for Low-Vmin, Noise-Tolerant, High-Density, 1R1W 8T-bitcell SRAM in 10nm FinFET CMOS", VLSI Circuit Symposium 2020, (**VLSI Symposium**), June 2020
- C2. R. Mathur, X. Xu, A. Chao, P. Chandupatla, S. Hung, N. Tadeipalli, S. Sinha, and **J. Kulkarni**, "Thermal Analysis of a 3D Stacked High-Performance Commercial Microprocessor using Face-to-Face Wafer Bonding Technology", 70th Electronic Components and Technology Conference (**ECTC**), June 2020
- C3. **J. P. Kulkarni**, A. Sayal, S. S. Teja Nibhanupudi, and S. Fatima, "All-Digital Time-Domain CNN engine using Bi-directional Memory Delay Lines" Government Microelectronic Conference (**GOMACTech**), March 2020
- C4. **J. P. Kulkarni**, and S. S. Teja Nibhanupudi, "Non-volatile SRAM leveraging novel materials" Government Microelectronic Conference (**GOMACTech**), March 2020

- C5. J. N. Rohan, P. Zhuang, S. S. Teja Nibhanupudi, S. K. Banerjee, and **J. P. Kulkarni**, "Machine Learning Assisted Compact Modeling of Cycle-to-cycle Variations in 2-D h-BN based RRAM devices" Government Microelectronic Conference (**GOMACTech**), March 2020
- C6. D. Prasad, S. S. Teja Nibhanupudi, S. Das, O. Zografos, B. Chehab, S. Sarkar, R. Baert, A. Robinson, A. Spessot, P. Debacker, D. Verkest, **J. Kulkarni**, B. Cline and S. Sinha, "Buried Power Rails and Back-side Power Grids: Arm® CPU Power Delivery Network Design Beyond 5nm", IEEE International Electron Device Meeting (**IEDM**), pp. 446-449, December 2019
- C7. J. N. Rohan, P. Zhuang, S. S. Teja Nibhanupudi, S. K. Banerjee, and **J. P. Kulkarni**, "Neural network assisted compact model for accurate characterization of Cycle-to-cycle variations in 2-D h-BN based RRAM devices" Device Research Conference (**DRC**), June 2019
- C8. S. S. Teja Nibhanupudi, and **J.P. Kulkarni**, "High density NV-SRAM using memristor and selector as technology assist" IEEE International Symposium on VLSI Technology, Systems and Applications (**VLSI-TSA**), April 2019 (**Best Student Paper Nomination**)
- C9. **J. P. Kulkarni**, and S. Teja, "Radiation Hardened Memory and Logic Design using Phase Transition Material" Government Microelectronic Conference (**GOMACTech**), March 2019
- C10. **J. P. Kulkarni**, A. Sayal, P. Ajay, M. McDermott, and S. V. Sreenivasan; "A Design Methodology for High-Mix, Low-Volume, Heterogeneously Integrated ASICs" Government Microelectronic Conference (**GOMACTech**), March 2019
- C11. A. Sayal, S. Fatima, S. S. Teja Nibhanupudi, and **J. P. Kulkarni**, "All-Digital Time-Domain CNN engine using Bi-directional Memory Delay Lines for Energy Efficient Edge Computing", International Solid State Circuits Conference (**ISSCC**), pp. 228-229, February 2019
- C12. S. Teja, A. Rai, A. Roy, S. Banerjee, and **J.P. Kulkarni**, "Memory and Logic soft error improvement using phase transition material assisted transistors" IEEE International Conference on Emerging Electronics (**ICEE**), December 2018
- C13. S. Teja, and **J.P. Kulkarni**, "Soft-FET: Phase transition material assisted Soft switching Field Effect Transistor for supply voltage droop mitigation" Design Automation Conference (**DAC**), June 2018
- C14. S. Teja, and **J.P. Kulkarni**, "Phase Transition Material assisted circuits for improved soft error tolerance" Silicon Errors in Logic – System Effects Workshop (**SELSE**), March 2018
- C15. P. Meinerzhagen, C. Tokunaga, A. Malavasi, V. Vaidya, A. Mendon, D. Mathaikutty, J. Kulkarni, C. Augustine, M. Cho, S. Kim, G. Matthew, R. Jain, J. Ryan, C.-C. Peng, S. Paul, S. Vangal, B. P. Esparza, L. Cuellar, M. Woodman, B. Iyer, S. Maiyuran, G. Chinya, X. Zou, Y. Liao, K. Ravichandran, H. Wong, M. Khellah, J. Tschanz, and V. De, "An Energy-Efficient Graphics Processor Featuring Fine-Grain DVFS with Integrated Voltage Regulators, Execution-Unit Turbo, and Retentive Sleep in 14nm Tri-Gate CMOS" International Solid State Circuits Conference (**ISSCC**), pp. 38-39, February 2018
- C16. **J. P. Kulkarni**, C. Tokunaga, M. Cho, M. M. Khellah, J. W. Tschanz, and V. K. De "F_{MAX} / V_{MIN} and noise margin impacts of aging on domino read, static write, and retention of 8T 1R1W SRAM arrays in 22nm high-k/metal-gate tri-gate CMOS" VLSI Circuit Symposium (**VLSI Symposium**), pp. 116-117, June 2017
- C17. **J. P. Kulkarni**, C. Tokunaga, C. Augustine, M. Khellah, J. Tschanz and V. De, "Adaptive and resilient high-performance memory design for dynamic variation tolerance" VLSI Test Symposium, April 2017 (**Invited paper**)
- C18. J. Keane, **J. Kulkarni**, K.-H Koo, S. Nalam, Z. Guo, E. Karl, and K. Zhang, "5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology" International Solid State Circuits Conference (**ISSCC**), pp. 308-309, Feb. 2016

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- C20. **J. P. Kulkarni**, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De, "A 409 GOPS/W Adaptive & Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin & Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature & Aging" International Solid State Circuits Conference (**ISSCC**), pp. 82-83, February 2015
- C21. S. Kim, Y.-C. Shih, K. Mazumdar, R. Jain, J. Ryan, C. Tokunaga, C. Augustine, **J. Kulkarni**, K. Ravichandran, J. Tschanz, M. Khellah, and V. De, "Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally-Controlled Hybrid LDO/Switched-Capacitor VR with Fast Droop Mitigation" International Solid State Circuits Conference (**ISSCC**), pp. 154-155, February 2015
- C22. S. Motaman, S. Ghosh, and **J. Kulkarni**, "A Novel Slope Detection Technique for Robust STTRAM Sensing" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 7-12, July 2015
- C23. C. Tokunaga, J. Ryan, C. Augustine, **J. Kulkarni**, Y. Shih, S. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. Khellah, J. Tschanz, V. De, "A 22nm Graphics Execution Core with Wide Voltage Range and 40% Higher Peak GFLOPS/W via Adaptive Clocking, Selective Boosting, and State-Retentive Sleep" International Solid State Circuits Conference (**ISSCC**), pp. 108-109, February 2014
- C24. **J.P. Kulkarni**, M. Khellah, J. Tschanz, B. Geuskens, R. Jain, S. Kim and V. De, "Dual-V_{cc} 8T-bitcell SRAM Array in 22nm Tri-gate CMOS for energy efficient operation across wide dynamic voltage range" VLSI Circuit Symposium (**VLSI Symp**), pp. C126-C127, June 2013, (**Conference highlight paper**)
- C25. R. Jain, B. Geuskens, M. Khellah, S. Kim, **J. Kulkarni**, J. Tschanz and V. De, "A 0.45-1V Fully Reconfigurable Switched Capacitor step down DC-DC converter with High Density MIM Capacitor in 22nm Tri-gate CMOS" VLSI Circuit Symposium (**VLSI Symp**), pp. C174-C175, June 2013 (**Conference highlight paper**)
- C26. S. M. Khan, A. R. Alameldeen, C. Wilkerson, **J. Kulkarni**, D. A. Jimenez, "Improving Multi-Core Performance Using Mixed-Cell Cache Architecture", International Symposium on High Performance Computer Architecture (**HPCA**), pp. 229-230, February 2013
- C27. **J. Kulkarni**, B. Geuskens, T. Karnik, M. Khellah, J. Tschanz and V. De, "Capacitive-Coupling Wordline Boosting with Self-Induced V_{cc} Collapse for Write V_{MIN} Reduction in 22-nm 8T SRAM" International Solid State Circuits Conference (**ISSCC**), pp. 234-235, February 2012
- C28. M. Nicolaidis, L. Anghel, N. Zergainoh, Y. Zorian T. Karnik, J. Tschanz, **J. Kulkarni**, K. Bowman, M. Khellah, A. Raychowdhury, C. Tokunaga, S-L Lu, and V. De, "Design for test and reliability in ultimate CMOS" Design Automation and Test in Europe (**DATE**), March 2012 (invited paper)
- C29. S. Gupta, **J.P. Kulkarni**, S. Datta and K. Roy, "Dopant Straggle-free Heterojunction Intra-band Tunneling (HIBT) FETs with Abrupt Source/Drain Junctions, Low Drain-induced Barrier Lowering/Thinning and Reduced Variation in OFF current" 2012 Device Research Conference (**DRC**), June 2012
- C30. V. Saripalli, S. Datta, V. Narayanan, and **J.P. Kulkarni**, "Variation-Tolerant Ultra low-power Heterojunction Tunnel FET SRAM Design" 7th International Symposium on Nanoscale Architectures (**NANOARCH**), pp. 45-52, June 2011
- C31. B. Geuskens, M. Khellah, **J. Kulkarni**, T. Karnik and V. De "Opportunities for PMOS Read and Write Ports in Low Voltage Dual-Port 8T Bit-Cell Arrays" Custom Integrated Circuits Conference (**CICC**), pp. 1-4, September 2010

- C32. A. Raychowdhury, B. Geuskens, **J. Kulkarni**, J. Tschanz, K. Bowman, T. Karnik, S.-L. Lu, V. De and M. Khellah, "PVT & Aging Adaptive Word-Line Boosting for 8T SRAM Power reduction" International Solid State Circuits Conference (**ISSCC**), pp. 352-353, February 2010
- C33. M. Meterelliyozy, A. Goel, **J. P. Kulkarni** and K. Roy, "Accurate Characterization of Random Process Variations Using a Robust Low-Voltage High-Sensitivity Sensor Featuring Replica-Bias Circuit" International Solid State Circuits Conference (**ISSCC**), pp. 186-187, February 2010
- C34. J. Tschanz, K. Bowman, M. Khellah, C. Wilkerson, B. Geuskens, D. Somasekhar, A. Raychowdhury, **J. Kulkarni**, C. Tokunaga, S.-L. Lu, T. Karnik, V. De, "Resilient Design in Scaled CMOS for Energy Efficiency" Asia Pacific Design Automation Conference (**ASP-DAC**), pp. 625-625, January 2010 (Invited paper)
- C35. K. Roy, **J. Kulkarni** and M.E. Hwang, "Low Voltage Process Adaptive Logic and Memory Arrays for Ultra-low Power Sensor Nodes" 8th IEEE **Sensors** Conference, pp. 185-188, October 2009 (Invited paper)
- C36. A. Goel, P. Ndai, **J. P. Kulkarni** and K. Roy, "Read/Access-Preferred (REAP) SRAM – Architecture-Aware Bit Cell Design for Improved Yield and Lower V_{min} " Custom Integrated Circuits Conference (**CICC**), September 2009
- C37. K. Roy, **J.P. Kulkarni**, S. Gupta, "Device/Circuit Interactions at 22nm Technology node" Design Automation Conference (**DAC**), pp.97-102, July 2009
- C38. M. Meterolliyez, P. Song, F. Stellari, **J. P. Kulkarni** and K. Roy, "A High Sensitivity Process Variation Sensor utilizing Sub-threshold operation" Custom Integrated Circuits conference (**CICC**), pp. 125-128, September 2008
- C39. K. Roy, **J.P. Kulkarni** and M.E. Hwang, "Process Adaptive Digital Sub-threshold Logic and Memory" 16th International Conference on Very Large Scale Integration (**VLSI-SOC**), pp. 42-45, October 2008 (Invited paper)
- C40. **J. P. Kulkarni**, K. Kim, S. Park and K. Roy, "Process Variation Tolerant SRAM Array for Ultra Low Voltage Applications" Design Automation Conference (**DAC**), pp. 108-113, June 2008
- C41. K. Roy, **J.P. Kulkarni**, M.E. Hwang, A. Raychowdhury and K. Kim, "Process Variation Tolerant Digital Sub-threshold Design" 33rd Annual Government Microcircuit Applications and critical Technology Conference (**GOMACTech**), March 2008
- C42. K. Roy, **J.P. Kulkarni** and M.E. Hwang, "Process Tolerant Ultra-Low Voltage Digital Sub-threshold Design" 8th topical meeting on silicon monolithic integrated circuits in RF systems, (**SIRF**), pp.42-45 January 2008 (Invited paper)
- C43. M. Meterolliyez, **J. P. Kulkarni** and K. Roy, "Thermal Analysis of 8-T SRAM for Nano-scaled Technologies" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 123-128, August 2008
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- C45. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Fully Differential Robust Schmitt Trigger based Sub-threshold SRAM" International Symposium on Low Power Electronics Design, (**ISLPED**), pp. 171-176, August 2007
- C46. **J. P. Kulkarni** and K. Roy "A High Performance Scalable Multiplexed Keeper Technique" 2007 International Symposium on Quality Electronics Design (**ISQED**), pp. 545-549, March 2007
- C47. **J. P. Kulkarni** and N. Bhat, "Effect of Poly-Si Gate Depletion on Tuning Range of MOS Varactors" Device Research Conference (**DRC**), pp. 81-82, June 2006

- C48. **J. P. Kulkarni** and N. Bhat, "Process Technique for Improving Tuning range in MOS Varactors" Proceedings of the IEEE **INDICON**, pp. 534-537, 2004
- C49. A. Pugalia, **J. P. Kulkarni**, N. Bhargava and N. Bhat "Single pocket Halo Sensitivity in 100nm Analog Transistor Design" Intl. Workshop on Physics of Semiconductor Devices (**IWPSD**), pp. 611-613, December 2003

Conference Presentations Without Proceedings

- C50. A. Sayal, S. Fathima, S. S. T. Nibhanupudi and J. P. Kulkarni, "All-Digital Time-Domain CNN Engine Using Bidirectional Memory Delay Lines for Energy-Efficient Edge Computing," **ARM Research Summit**, September 2019
- C51. S. S. Teja Nibhanupudi, and **J.P. Kulkarni**, "High Density NV-SRAM using Memristor and Selector as Technology Assist" **ARM Research Summit**, September 2019
- C52. S. S. Teja Nibhanupudi, and **J.P. Kulkarni**, "High Density NV-SRAM using Memristor and Selector as Technology Assist" **SRC TECHCON**, September 2019
- C53. A. Sayal and J. P. Kulkarni, "All-Digital Time-Domain CNN Engine for Energy Efficient Edge Computing," in ACM SIGDA and IEEE CEDA Ph.D. Forum at IEEE Design Automation Conference (**DAC**), June 2019
- C54. **J. P. Kulkarni**, C. Augustine, B. Jung and K. Roy, "Nano-Spiral Inductors for Low Power Digital Spintronic Circuits" International Magnetism Conference (**INTERMAG**), January 2010
- C55. **J. P. Kulkarni** and K. Roy, "Process Variation Tolerant SRAM Design for Ultra Low Voltage Applications" **SRC TECHCON**, November 2008 (Best paper in session Award)
- C56. **J. P. Kulkarni**, K. Kim and K. Roy, "A 160mV Fully Differential Robust Schmitt Trigger based Sub-threshold SRAM" **SRC TECHCON** 2007
- C57. **J. P. Kulkarni** and N. Bhat, "Process Technique for Improving Tuning range in Varactors using Poly-Silicon Depletion effect" Asia Pacific Microwave Conference (**APMC**), December 2004