JVST B
Journal of Vacuum Science & Technology B

Controlling the etch selectivity of silicon using low-RF power HBr reactive ion etching

Cite as: J. Vac. Sci. Technol. B **40**, 062802 (2022); https://doi.org/10.1116/6.0002109
Submitted: 26 July 2022 • Accepted: 12 September 2022 • Published Online: 24 October 2022

Kun-Chieh Chien and Chih-Hao Chang

COLLECTIONS

Paper published as part of the special topic on Papers from the 65th International Conference on Electron, Ion, And Photon Beam Technology and Nanofabrication (EIPBN 2022)

View Online Export Citation CrossMark

ARTICLES YOU MAY BE INTERESTED IN

Evolution of lithography-to-etch bias in multi-patterning processes
Journal of Vacuum Science & Technology B **40**, 062601 (2022); https://doi.org/10.1116/6.0002059

SiO_2 etching and surface evolution using combined exposure to CF_4/O_2 remote plasma and electron beam
Journal of Vacuum Science & Technology A **40**, 063004 (2022); https://doi.org/10.1116/6.0002038

Dependence of electron emission current density on excitation power density from Cs/O-activated negative electron affinity InGaN photocathode
Journal of Vacuum Science & Technology B **40**, 062202 (2022); https://doi.org/10.1116/6.0002124

JVST B
Journal of Vacuum Science & Technology B

ARTICLE

avs.scitation.org/journal/jvb

Controlling the etch selectivity of silicon using low-RF power HBr reactive ion etching

Cite as: J. Vac. Sci. Technol. B **40**, 062802 (2022); doi: 10.1116/6.0002109
Submitted: 26 July 2022 · Accepted: 12 September 2022 ·
Published Online: 24 October 2022

View Online Export Citation CrossMark

Kun-Chieh Chien and Chih-Hao Chang[a)]

AFFILIATIONS

Walker Department of Mechanical Engineering, The University of Texas at Austin, Austin, Texas 78712, USA

Note: This paper is part of the Special Topic Collection: Papers from the 65th International Conference on Electron, Ion, And Photon Beam Technology and Nanofabrication (EIPBN 2022).

[a)] **Author to whom correspondence should be addressed:** chichang@utexas.edu

ABSTRACT

Silicon nanostructures with high aspect-ratio (AR) features have played an important role in many fields. In this study, we report the fabrication of high AR silicon nanostructures using an inductively coupled plasma reactive ion etching (ICP-RIE) process by controlling the voltage bias at the substrate. The results show that by reducing the radio frequency (RF) bias power to 10 W, the etch selectivity of silicon to photoresist can be enhanced up to 36 times. Using the photoresist as a mask, this process can fabricate 300 nm-period one-dimensional (1D) grating structures with a height up to 807 nm, an improvement of 3.75-fold compared with structures fabricated by normal bias power. Furthermore, the analysis of the etch rate shows that the etch rate decreases over time in 1D gratings but remains constant in 2D pillar arrays, which can be attributed to the removal of the sidewall passivation. By including an O_2 ICP-RIE step to remove the remaining polymer mask, the highest AR of 2D pillar structures that can be achieved is 8.8. The optical characterization of the fabricated structures demonstrates effective antireflection properties, where the measurements show that the reflectivity can be suppressed from 35% to 0.01% near normal incidence and 35% to 2.4% at 65° incident angle. The demonstrated low-RF power ICP-RIE process can create high AR nanostructures without the need for an inorganic mask and can find applications in integrated circuits, photonics, and functional nanostructures.

I. INTRODUCTION

Silicon has played an important role in many fields, such as integrated circuits,[1–5] microelectromechanical system,[6–9] and nanophotonics[10–14] due to its superior characteristics. Silicon nanostructures with high aspect-ratio (AR) features have a high surface area to volume ratio and can lead to improved device performance in biosensing,[15–19] photovoltaics,[20–22] and microfluidics.[23] To create high AR silicon nanostructures, several techniques have been introduced in the past. The most renowned techniques are the Bosch process or deep reactive ion etching[24,25] and metal-assisted chemical etching (MACE).[26–29] In the Bosch process, sulfur hexafluoride (SF_6) is used for silicon etching, and octafluorocyclobutane (C_4F_8) helps deposit a chemically inert passivation layer on the etched surface. By alternating the two gasses in a cyclic process, silicon gratings with an ultrahigh AR of 60 have been demonstrated.[30] MACE is a wet etching process using a noble or base metal as a catalyst to enhance the dissolution of silicon near its surface, which has demonstrated nanostructures with an ultrahigh AR up to over 20.[29] Furthermore, other techniques using a multilayer etching mask to etch sapphire[31,41] might be able to provide inspiration for fabricating high AR silicon nanostructures. However, those techniques generally include many steps and are process intensive. For instance, the Bosch process repeatedly switches between the standard plasma etching and sidewall passivation to achieve high AR structures.[32] MACE requires a metal mask that can diffuse into silicon and must be completely removed after the process. An alternative approach is RIE with an appropriate selection of etch chemistry, such as HBr and Cl_2, which is relatively simple and can achieve silicon structures with a high AR of 7.[33] However, these processes require the use of hard masks such as silicon oxide to achieve such etch depth.

In this study, we present a simple one-step etching process that can fabricate periodic silicon nanostructure with an AR of 9 using a polymer mask. This approach utilizes inductively coupled plasma reactive ion etching (ICP-RIE) with low radio frequency (RF) bias voltage to enhance the etching selectivity of silicon to photoresist (PR). It is known that in ICP-RIE that the etch mechanism can be made to favor chemical etching as opposed to physical and ion-assisted etching by reducing the bias voltage at the substrate,[34] which has been shown to improve etch selectivity and anisotropy. By limiting the silicon etching to chemical etching and promoting sidewall passivation, the process allows deeper etch into the substrate without degrading the polymer masks. The etch rates, etch selectivity, and structure profiles of the proposed process are studied using periodic 1D and 2D photoresist nanostructure patterns. Using this process, 2D pillar array with 300 nm period and 700 nm height has been fabricated, achieving an AR of 8.8. The optical properties of the fabricated structures have been characterized and demonstrate excellent antireflection properties. The nanostructures fabricated by the proposed method have potential values for various applications in functional nanostructures such as antireflection[35–39,42] and self-cleaning.[40,43]

II. EXPERIMENT

The process steps of the proposed fabrication technique are illustrated in Fig. 1. Initially, a 100 nm antireflection coating (ARC, i-con-7, Brewer Science) is spin-coated on the silicon substrate, which is designed to minimize the amount of light reflected into the PR to result in standing wave and sidewall waviness. A 200 nm PR (PFI-88A2, Sumitomo) is then spin-coated on the ARC layer. The PR is exposed using Lloyd's mirror interference lithography[44,45,48] to form 1D or 2D patterns with a period of 300 nm in the PR layer, as shown in Fig. 1(a). The spatial period Λ is controlled by the angle of incidence of two laser beams, which is set by rotating the stage that holds the mirror and chuck as determined by:

$$\Lambda = \frac{\lambda}{2\,\sin\theta}, \tag{1}$$

where λ is the wavelength of the laser and θ is half of the angle between the two interfering beams as well as the rotating angle of the stage holding the mirror and the chuck. A 325 nm HeCd laser with transverse electric (TE) mode is used for this technique. The 1D grating patterns are obtained by a single exposure, and the 2D periodic pillar arrays are obtained by two orthogonal exposures. This technique can fabricate nanostructures on a large scale, which makes potential applications more practical and feasible.

The patterned 1D or 2D PR structures are then transferred to the underlying substrate using ICP-RIE (Oxford 100), as illustrated in Fig. 1(b). To transfer the PR pattern into ARC, O_2 gas is used for the etching process (130 s etch time, RF power 60 W, ICP power 0 W, pressure 13 mTorr, flow rate 25 SCCM). The residual PR and ARC then form the polymer mask for the subsequent etch into the silicon substrate using HBr. The RF power setting for the HBr ICP-RIE is varied to examine the effects of the voltage bias, while other process conditions are kept constant (ICP power 200 W, pressure 8 mTorr, flow rate 30 SCCM). Due to the tool limitation, the lowest RF power for the ICP-RIE etcher is 10 W. Therefore, six RF power settings, namely, 10, 15, 30, 60, 120, and 250 W, are used to control the etch regime during the HBr ICP-RIE. After completing the ICP-RIE process, the remaining PR and ARC above the silicon nanostructures are cleaned via wet or dry cleaning processes such as RCA Clean or O_2 ICP-RIE.

The effect of different RF powers on the silicon etch rate and the etch selectivity will be studied, the latter is defined as

$$Etch\ selectivity = \frac{Etch\ rate\ of\ silicon}{Etch\ rate\ of\ the\ polymer\ mask\ (PR + ARC)}. \tag{2}$$

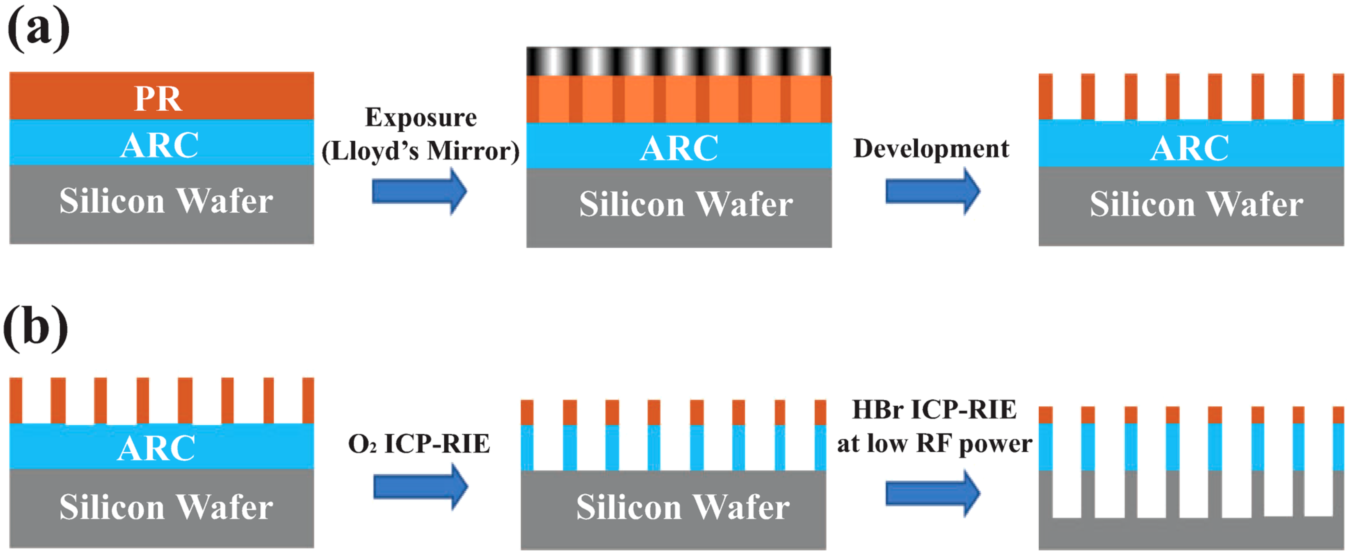

FIG. 1. Fabrication processes of proposed technique. (a) The exposure and development. (b) Etching.

III. RESULTS AND DISCUSSION

A. HBr ICP-RIE at low RF power

Before examining the influence caused by different RF powers, 1D gratings etched by the normal RF power, which is 250 W, are shown in Fig. 2. Figure 2(a) shows the cross-sectional scanning electron micrograph (SEM) images of 1D gratings after pattern transfer into the ARC layer using O_2 ICP-RIE, resulting in a polymer mask consisting of PR and ARC layers with around 215 nm thickness. Figures 2(b)–2(d) show the structures after 3, 5, and 10 min of HBr ICP-RIE with an RF power of 250 W, respectively. All three gratings have a similar height, which is 215 nm, and without any polymer left on the top of the structures. For the process conditions in this experiment, the etch rate of silicon on the etcher is around 80 nm/min and the etch selectivity of silicon to the polymer mask is close to 1. At this etch rate, 3 min etch time is sufficient to completely remove all the polymer mask. Additional etching after 3 min would result in etching of bare silicon structures, resulting in the same etch rate on the top and bottom of the gratings structures. As a result, the silicon gratings with 3, 5, and 10 min etch time in Figs. 2(b)–2(d) have a similar height and an AR of around 1.8, which is calculated by using the middle waist of the gratings as the width.

The effect of lower RF power on the structure profile can be observed in the SEM images shown in Fig. 3. In these experiments, the 1D gratings are etched using various RF power and etching times, namely, 60 W with 12 min, 30 W with 24 min, 15 W with 48 min, and 10 W with 70 min for Figs. 3(a)–3(d), respectively. Since reducing the RF power reduces the silicon etch rate, longer etch times are used to achieve a similar etch depth. The measured structure heights are around 415 nm for the 60 W sample, 690 nm for the 30 W sample, and around 720 nm for both 15 and 10 W samples. For all cases, the polymer mask remains on the structures, as indicated by white dashed lines in the figure. These results indicate that reducing the RF power reduces the polymer etch rate, which increases the etch selectivity of silicon to polymer. These gratings also have slightly different profiles and can be categorized into two groups: with and without V-shaped trenches at the bottom of the gratings. Gratings that are etched at 60 and 30 W have a microtrenching effect at the edges of the valley, which indicates the reflection and focusing of ions from the sidewall.[46] On the other hand, the gratings that are etched at 15 and 10 W have a positive taper near the valley to yield the V-shaped profile, as a result of less ion energy and the reaction favoring chemical etching at low RF power. It is also interesting to note that the etch maintains anisotropy, which can be attributed to the deposition of carbon and bromine species on the sidewall during the HBr ICP-RIE.[47]

To further study the etch selectivity under different voltage biases, structures fabricated with RF power settings of 10, 15, 30, 60, 120, and 250 W are examined. Since the structure profiles fabricated using different RF powers can vary, the deepest point in the grating at the end of the etch process is used for calculating the etch rate and the etch selectivity. The etch selectivity is calculated by Eq. (2), which is defined by the etch rate of silicon divided by the etch rate of the polymer mask. The etch selectivity is plotted versus the RF power setting, as illustrated in Fig. 4, and increases exponentially as the RF power decreases. The lowest etch selectivity is 1.04 at 250 W, and the highest etch selectivity is 36.1 at 10 W RF power. The high selectivity is caused by the less energized ions induced by the lower voltage bias at the substrate, which enables the chemical etching to be dominant. This process is facilitated by the separate ICP and RF modules in ICP-RIE, which can independently control ion flux and energy. The ICP source generates a high-density plasma, and the RF voltage bias at the substrate energizes ions. Higher ion energy leads to more significant ion bombardments and physical sputtering. Therefore, reducing RF voltage bias helps favor chemical etching versus ion-assisted etching. In general, in physical sputtering, the dominant species are ions that tend to attack everything; however, in chemical etching, the

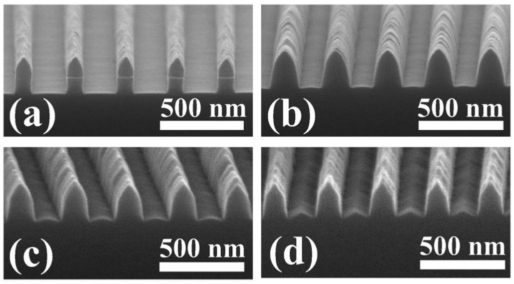

FIG. 2. 1D gratings made by (a) O_2 ICP-RIE with 130 s etch time. (b) 250 W RF power HBr ICP-RIE with 3 min etch time. (c) 250 W RF power HBr ICP-RIE with 5 min etch time. (d) 250 W RF power HBr ICP-RIE with 10 min etch time.

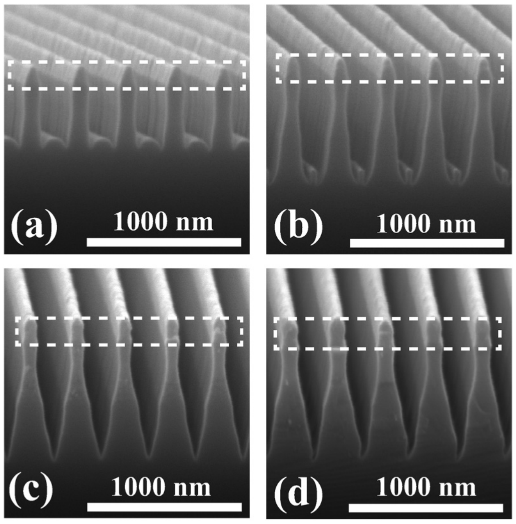

FIG. 3. Cross-sectional SEM images of grating structures etched using various RF power and etch times in HBr ICP-RIE. The process conditions are (a) 60 W with 12 min etch time, (b) 30 W with 24 min etch time, (c) 15 W with 48 min etch time, and (d) 10 W with 70 min etch time. The white dash frames indicate the location of the polymer mask in the structures.

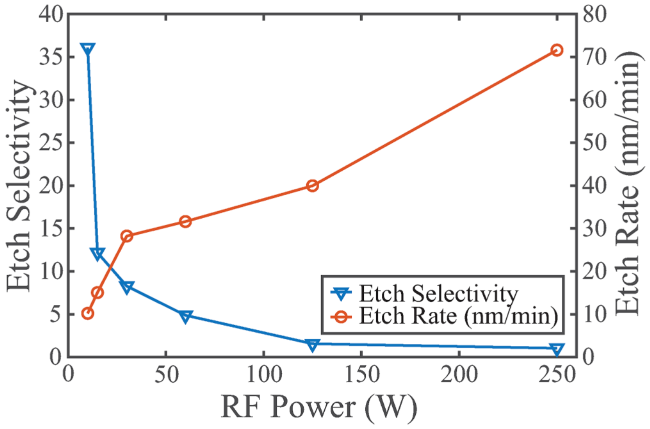

FIG. 4. Etch selectivity (line with triangle markers) of silicon over the polymer mask and the etch rate (line with circle markers) of silicon at different RF power settings. Each point represents a single experiment.

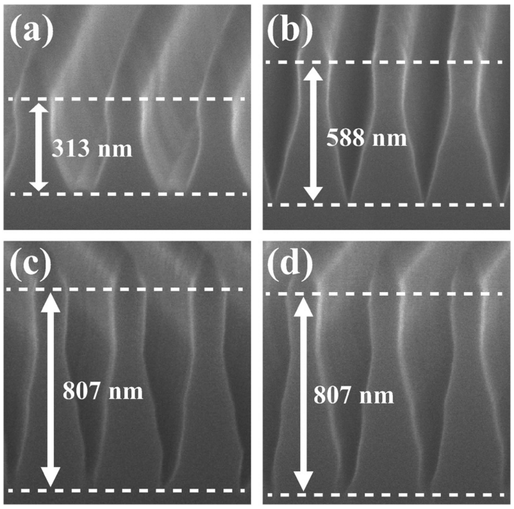

FIG. 5. Fabricated 1D gratings using 15 W RF power HBr ICP-RIE with (a) 20, (b) 40, (c) 60, and (d) 80 min etch times. White double arrow lines indicate the height of silicon gratings. All gratings have a residual polymer mask left on the top of the structures.

dominant species are radicals that favor reacting with target materials. As a result, as the process tends to chemical etching by reducing the RF voltage bias, the etch selectivity increases and higher nanostructures can be obtained when using the same thickness of the mask.

One important observation is that a low RF power will also lead to a low silicon etch rate, which leads to longer etch times. The etch rate of silicon is also plotted versus the RF power in Fig. 4 and decreases significantly at a lower RF power. The highest etch rate is 71.6 nm/min at 250 W RF power, and the lowest one is 10.2 nm/min at 10 W RF power. It is important to note that since the silicon etch rates decrease at a lower RF power, the increase in etch selectivity is solely due to the more dramatic decrease in the polymer etch rate. This result indicates that to achieve nanostructures with the same height, etching at 10 W requires roughly 7 times longer etch time when compared with etching at 250 W RF power. The converse is also true, which is that etching with 250 W RF power can be 7 times shorter but given the low selectivity, the polymer mask needs to be 36 times thicker compared with performing the etch using the 10 W RF power. Such a thick polymer mask is not feasible due to the collapse of high AR resist patterns, which then requires the use of inorganic masks such as SiO_2 to improve selectivity.

The previous experiments indicate that the silicon etch selectivity can be improved using low-RF power HBr ICP-RIE. To identify the limit of the etch depth and examine the evolution of the structure profile, cross-sectional SEM images of gratings fabricated using 15 W RF power and 20–80 min etch times are shown in Fig. 5. The corresponding heights of silicon gratings are 314, 589, 807, and 807 nm for 20, 40, 60, and 80 min etch times, respectively. It can be noted that all gratings have polymer masks left even after 80 min of etching due to the low polymer etch rate. However, after etching for 60 min, the gratings depth does not increase. The average etch rate of each duration, namely, from 0 to 20 min, 20 to 40 min, 40 to 60 min, and 60 to 80 min, is calculated and shown in Fig. 6. The data indicate that the etch rate decreases almost linearly before 60 min from 15.7 to 13.8 to 10.9 nm/min and then abruptly goes to 0 after 60 min. The reason for this phenomenon might be due to the difficulty in removing the sidewall passivation in the deep V-shaped trenches. In the low bias etching process, ions help remove the sidewall passivation layer and allow the free radicals to etch the silicon. However, once steep sidewall forms in the V-shape profile, ions can reflect from the sidewalls instead of removing the passivation layer. Although the reflected ions can be focused at the bottom of the V-shape trench, they do not have enough energy to etch into silicon due to the low RF power and the energy loss from the reflection. Furthermore, the narrow and deep V-shape trenches hinder sufficient radicals from flowing into the nanostructures. As a result, the etch process slows and eventually stops. The measurements of the angles of the V-shaped trenches further validate this inference. In Fig. 5(a), the sidewalls transition from vertical to a slight positive taper, but the V-shaped trench has not formed, so the ions are able to remove the redeposition at the valley to enable etching. Figures 5(b)–5(d) indicate that the V-shaped trenches form after 40 min etching, and the angles of trenches are 25.6°, 21.6°, and 21.4°, respectively. That is, the sidewall angles decrease at longer etch times, and the trenches become narrower. The formation of the V-shaped trench at low angles makes the sidewall deposition of polymer species difficult to remove. As a result, the height of the gratings is limited by the formation of the V-trenches even though polymer masks remain on the top of the gratings.

In addition to 1D gratings, we also examined the fabrication of 2D pillar array using low-RF power HBr ICP-RIE, as shown in Fig. 7. The pillar arrays have 300 nm period as patterned by interference lithography and are etched by 15 W RF power with 50 and 80 min etch time, as shown in Figs. 8(a) and 8(b), respectively. Here, the structures are cleaned by a standard RCA clean process

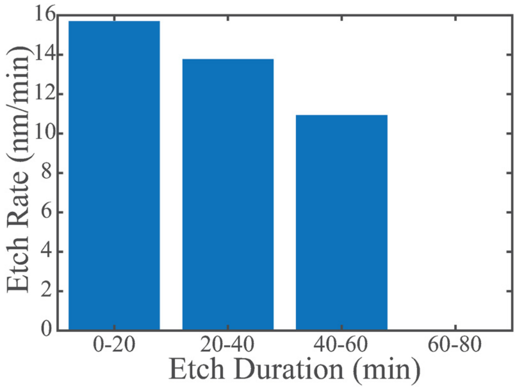

FIG. 6. Average etch rates of silicon vs the etch time using 15 W RF power.

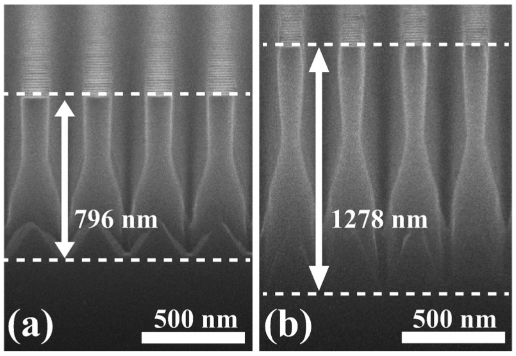

FIG. 7. 2D pillar arrays fabricated using 15 W RF power HBr ICP-RIE with (a) 50 and (b) 80 min etch time. The height of silicon pillars is noted by the white arrows. The polymer mask on the top of the pillar arrays is removed by a standard RCA clean.

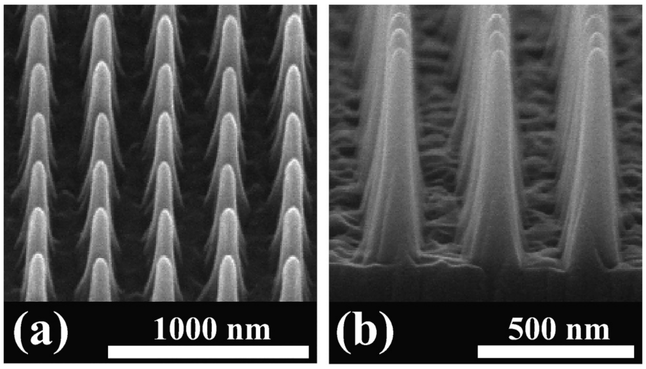

FIG. 8. SEM images of fabricated 2D silicon pillar arrays viewed at (a) 45 tilt angle and (b) cross section. The structures are fabricated using 15 W RF power HBr ICP-RIE with 48 min etch time and cleaned by O_2 ICP-RIE for 7 min.

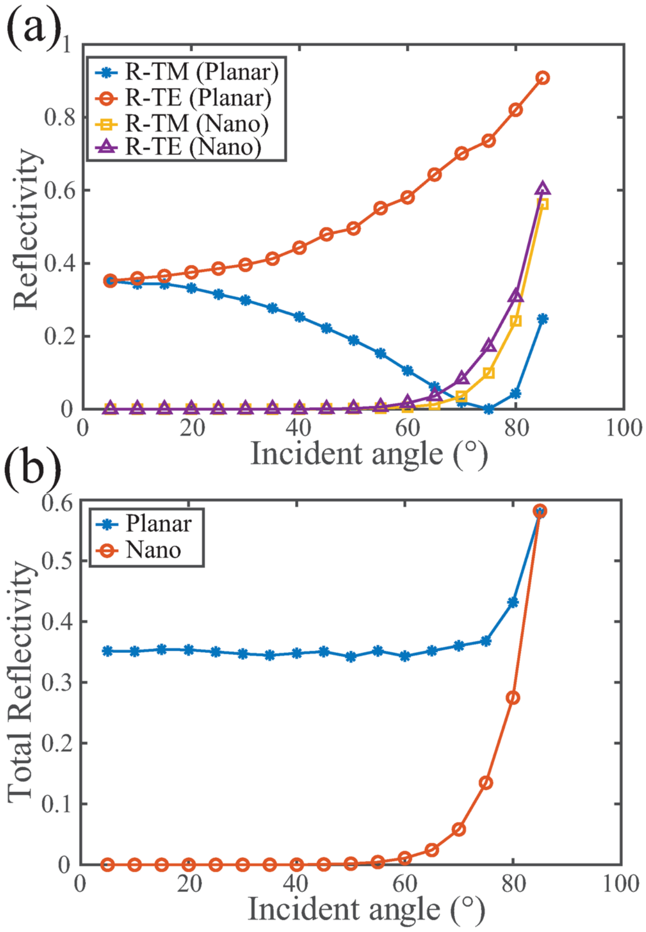

FIG. 9. Reflectivity at different incident angles of a planar silicon wafer and 2D silicon pillar arrays by using a 633 nm laser. (a) Reflectivity in TE and TM directions of two samples, and (b) total reflectivity of two samples.

(5:1:1 solution of deionized water:NH_4OH:H_2O_2) to remove the remaining polymer mask. The heights of structures are 796 and 1278 nm for 50 and 80 min etch time, respectively, which both result in etch rates of around 15.9 nm/min. Compared with the etch rate versus etch time of 1D gratings, the etch rate of 2D pillars is constant for the etch times tested. This observation can be attributed to the 2D pillar arrays having less confined sidewalls at the bottom of the base compared to the 1D trenches, allowing the ion-assisted removal of the sidewall passivation layers and sufficient radicals to flow into the bottom structure to continue the chemical reaction.

B. Application of fabricating nanostructures

High AR nanostructures can modify the physical properties of the surface and bring benefits to many applications. One example is high AR nanostructures with a tapered profile can lead to antireflection, which can be used to reduce substrate reflection by suppressing Fresnel reflection via index matching.[35–39,42] Using the low-RF power HBr ICP-RIE process, a 2D pillar array with 300 nm period and 700 nm height was fabricated, as shown in Fig. 8. The structures are etched using 15 W RF power HBr ICP-RIE for 48 min etch time and then cleaned by O_2 ICP-RIE for 7 min (RF power 200 W, ICP power 1000 W, pressure 13 mTorr, flow rate 40 SCCM) to remove residual polymer and redeposition. The structure AR is around 8.8 calculated by using the middle waist of the pillar as the width.

The optical characterization is performed by the specular reflectivity measurements at different incident angles using a 633 nm laser for transverse-magnetic (TM) direction and TE polarizations. The reflectivity of the 2D silicon pillar arrays at different incident angles using a 633 nm laser is shown in Fig. 9(a). The TE data indicate that the reflectivity can be reduced to 0.02% from 35% for a planar substrate at normal incidence. The antireflection effects are maintained at a high incident angle of 65°, where the reflectivity is 3.6% for the silicon nanostructures and 64% for the planar silicon substrate. The TM reflectivity data for the planar silicon show a dip at 75°, which is characteristic of Brewster's angle effect. Furthermore, the reflectivity of 2D silicon pillar arrays at different angles in both TE and TM directions is similar. The total reflectivity for nonpolarized light is calculated by averaging TM and TE reflections and plotted in Fig. 9(b). The results demonstrate that the reflectivity is reduced for all values below 85° incident angle. Furthermore, the reflectivity is well suppressed from 0.035 to below 0.025 from 5° to 65° incident angles. The structures can potentially operate for longer wavelengths given the high ARs, which will be examined further in future work.

IV. SUMMARY AND CONCLUSIONS

The proposed approach demonstrates a single-step fabrication process to obtain silicon nanostructures using low-power ICP-RIE with an AR up to 9 while using a polymer mask. This technique is enabled by controlling the RF power during HBr ICP-RIE of silicon, which can favor chemical etching over ion-assisted etching. The experimental results indicate that the silicon to polymer etch selectivity can be as high as 36.1 at 10 W RF power, an enhancement of up to 36 times when compared with 250 W RF power. The etch rate decreases simultaneously at a lower RF power, which requires the use of longer etch times. Also, the study of the etch rate over time shows that the etch rate decreases when the etch duration increases for 1D gratings, but the etch rate over time remains constant for 2D pillar arrays. We have successfully demonstrated the fabrication of 2D silicon pillar arrays with 300 nm period and an AR of 8.8. The fabricated nanostructures demonstrate excellent antireflection properties, with measurement reflectivity for nonpolarized light suppressed to 0.01% at near normal incidence and 2.4% at 65° incident angle. The proposed low-RF power HBr ICP-RIE process is a facile method to create nanostructures with high AR and can find applications in nanostructured surfaces, photonics, and other integrated devices.

ACKNOWLEDGMENTS

This work was performed at UT Austin Texas Materials Institute (TMI), the Nanomanufacturing System for Mobile Computing and Energy Technologies (NASCENT), and Texas Nanofabrication Facilities, which is supported by the National Science Foundation (NSF) as part of the National Nanotechnology Coordinated Infrastructure (NNCI) under Grant No. NNCI-2025227. This work is funded by the NSF under Grant No. CMMI#1552424.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Kun-Chieh Chien: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Project administration (lead); Software (lead); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Chih-Hao Chang:** Conceptualization (equal); Funding acquisition (lead); Project administration (supporting); Resources (lead); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] H. Iwai and S. Ohmi, Microelectron. Reliab. **42**, 465 (2002).
[2] A. S. Oates, in *Reliability Characterisation of Electrical and Electronic Systems*, edited by J. Swingler (Woodhead Publishing, Oxford, 2015), pp. 115–141.
[3] R. W. Dutton, IEEE Trans. Electron Devices **30**, 968 (1983).
[4] G. Roelkens, D. Vermeulen, S. Selvaraja, R. Halir, W. Bogaerts, and D. Van Thourhout, IEEE J. Sel. Top. Quantum Electron. **17**, 571 (2011).
[5] W.-W. Shen and K.-N. Chen, Nanoscale Res. Lett. **12**, 56 (2017).
[6] M. Tilli, M. Paulasto-Krockel, M. Petzold, H. Theuss, T. Motooka, and V. Lindroos, *Handbook of Silicon Based MEMS Materials and Technologies* (Elsevier, New York, 2020).
[7] A. M. Hynes, H. Ashraf, J. K. Bhardwaj, J. Hopkins, I. Johnston, and J. N. Shepherd, Sens. Actuators, A **74**, 13 (1999).
[8] P. Ruther, S. Herwik, S. Kisban, K. Seidl, and O. Paul, IEEJ Trans. Electr. Electron. Eng. **5**, 505 (2010).
[9] G. Zhanshe, C. Fucheng, L. Boyu, C. Le, L. Chao, and S. Ke, Microsyst. Technol. **21**, 2053 (2015).
[10] G. T. Reed and A. P. Knights, *Silicon Photonics: An Introduction* (John Wiley & Sons, New York, 2004).
[11] B. Jalali and S. Fathpour, J. Lightwave Technol. **24**, 4600 (2006).
[12] R. Soref, IEEE J. Sel. Top. Quantum Electron. **12**, 1678 (2006).
[13] J. Leuthold, C. Koos, and W. Freude, Nat. Photonics **4**, 535 (2010).
[14] D. Thomson *et al.*, J. Opt. **18**, 073003 (2016).
[15] L. Ann Bauer, N. S. Birenbaum, and G. J. Meyer, J. Mater. Chem. **14**, 517 (2004).
[16] S. Merlo, G. Barillaro, F. Carpignano, S. Surdo, L. M. Strambini, A. Montecucco, V. Leva, and G. Mazzini, IEEE J. Sel. Top. Quantum Electron. **18**, 1215 (2012).
[17] F. A. Harraz, Sens. Actuators, B **202**, 897 (2014).
[18] D. Brodoceanu, R. Elnathan, B. Prieto-Simón, B. Delalat, T. Guinan, E. Kroner, N. H. Voelcker, and T. Kraus, ACS Appl. Mater. Interfaces **7**, 1160 (2015).

[19] A. Irrera *et al.*, ACS Photonics **5**, 471 (2018).
[20] X. Li, Curr. Opin. Solid State Mater. Sci. **16**, 71 (2012).
[21] S.-H. Baek, H. S. Jang, and J. H. Kim, Curr. Appl. Phys. **11**, S30 (2011).
[22] J. R. Maiolo, B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, H. A. Atwater, and N. S. Lewis, J. Am. Chem. Soc. **129**, 12346 (2007).
[23] S. Yadavali, D. Lee, and D. Issadore, Sci. Rep. **9**, 12213 (2019).
[24] F. Laermer and A. Schilp, US5501893A (26 March 1996).
[25] F. Laermer and A. Urban, Microelectron. Eng. **67-68**, 349 (2003).
[26] D. Dimova-Malinovska, M. Sendova-Vassileva, N. Tzenov, and M. Kamenova, Thin Solid Films **297**, 9 (1997).
[27] X. Li and P. W. Bohn, Appl. Phys. Lett. **77**, 2572 (2000).
[28] Z. Huang, N. Geyer, P. Werner, J. de Boor, and U. Gösele, Adv. Mater. **23**, 285 (2011).
[29] A. Mallavarapu, P. Ajay, and S. V. Sreenivasan, Nano Lett. **20**, 7896 (2020).
[30] A. R. Bruccoleri, R. K. Heilmann, and M. L. Schattenburg, J. Vac. Sci. Technol. B **34**, 06KD02 (2016).
[31] Y.-A. Chen, I.-T. Chen, and C.-H. Chang, J. Vac. Sci. Technol. B **37**, 061606 (2019).
[32] M. A. Blauw, T. Zijlstra, and E. van der Drift, J. Vac. Sci. Technol. B **19**, 2930 (2001).
[33] M. A. Vyvoda, H. Lee, M. V. Malyshev, F. P. Klemens, M. Cerullo, V. M. Donnelly, D. B. Graves, A. Kornblit, and J. T. C. Lee, J. Vac. Sci. Technol. A **16**, 3247 (1998).
[34] L. Xie, T. X. Zhou, R. J. Stöhr, and A. Yacoby, Adv. Mater. **30**, 1705501 (2018).
[35] P. Vukusic and J. R. Sambles, Nature **424**, 852 (2003).
[36] Y. Kanamori, M. Sasaki, and K. Hane, Opt. Lett. **24**, 1422 (1999).
[37] P. Lalanne and G. M. Morris, Nanotechnology **8**, 53 (1997).
[38] K.-C. Park, H. J. Choi, C.-H. Chang, R. E. Cohen, G. H. McKinley, and G. Barbastathis, ACS Nano **6**, 3789 (2012).
[39] Q. Yang, X. A. Zhang, A. Bagal, W. Guo, and C.-H. Chang, Nanotechnology **24**, 235202 (2013).
[40] A. R. Parker and C. R. Lawrence, Nature **414**, 33 (2001).
[41] Y.-A. Chen, K.-C. Chien, I.-T. Chen, and C.-H. Chang, Micro Nano Eng. **14**, 100115 (2022).
[42] Y.-A. Chen, S. V. Naidu, Z. Luo, and C.-H. Chang, J. Appl. Phys. **126**, 063101 (2019).
[43] A. Lafuma and D. Quéré, Nat. Mater. **2**, 457 (2003).
[44] A. Bagal and C.-H. Chang, Opt. Lett. **38**, 2531 (2013).
[45] I. Wathuthanthri, W. Mao, and C.-H. Choi, Opt. Lett. **36**, 1593 (2011).
[46] R. J. Hoekstra, M. J. Kushner, V. Sukharev, and P. Schoenborn, J. Vac. Sci. Technol. B **16**, 2102 (1998).
[47] A. P. Mahorowala and H. H. Sawin, J. Vac. Sci. Technol. B **20**, 1055 (2002).
[48] H. I. Smith, Physica E **11**, 104 (2001).