Integrated WDM-based Optical Comparator for High-speed Computing

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Abstract: We propose and experimentally demonstrate a 2-bit wavelength-division-multiplexing (WDM) based optical comparator using microdisk modulators operating at 10 Gb/s. The proposed comparator has advantages of higher speed and lower power consumption compared to electronic counterparts.
OCIS codes: (200.4660) Optical logic; (250.3750) Optical logic devices; (130.3120) Integrated optics devices

1. Introduction

As the continuation of Moore's law has become problematic, researchers have been seeking alternatives such as integrated optical circuits to replace electric circuits to do computation. It is promising to use integrated photonics to process information thanks to the key features of light, which are low latency, high bandwidth, and low power consumption. On the other hand, current fabrication technologies allow photonics components and transistors to be integrated on the same chip, which paves the way for inner-chip communications between electronic modules and photonics modules to realize some complex computing modules [1].

Various fundamental optical computing modules have been proposed in recent works [2]. For example, high-speed multiple-bit full adders have been experimentally demonstrated recently [3][4], revealing that photonic computing modules are capable of doing large bit-size computation while their performances outperform electronic counterparts in speed and energy consumption. More and more functions in an arithmetic logic unit (ALU) are expected to be implemented via integrated photonics circuits.

In this paper, we devise a novel scheme to realize an N-bit WDM-based electronic-photonic digital comparator using microdisk modulators as electrooptic (EO) logic gates for high-speed and energy-efficient computation. WDM is used to optimize the number of logic gates as well as the other performances. A 2-bit OCMP operating at 10 Gbit/s is experimentally demonstrated, which is the fastest proposed optical comparator to our best knowledge.

2. Theory

Figure 1 shows the general architecture of an EO comparator, where two wavelengths are used to implement functions of subtractor and equality comparator independently. The subtractor determines the larger of two binary numbers A and B by computing $B-A=B+\overline{A}+1$, which can be realized by any adder architecture. If there is a carry out, then we will have $A \le B$;otherwise, $A > B$. The equality comparator determines if A=B, which can be done simply with XOR/XNOR gates and ones/zeros detector. The logic expression of them can then be summarized by:

$$C_k = (\overline{a_k} \oplus b_k)\cdot C_{k-1} + \overline{a_k}\cdot b_k = p_k \cdot C_{k-1} + g_k \tag{1}$$

$$Z = (a_1 \otimes b_1)\cdot(a_2 \otimes b_2)\cdot\ldots(a_n \otimes b_n) = p_1 p_2 \ldots p_n \tag{2}$$

where $C_0 = 1$, $p_k = \overline{a_k} \oplus b_k = a_k \otimes b_k$ (propagate) and $g_k = \overline{a_k}\cdot b_k$ (generate). The p and g signals will be applied to the EO modulators simultaneously, while lights of different wavelengths will propagate the EO comparator and do the computation with the help of active and passive components, such as modulators and combiners (Fig. 1(b)).

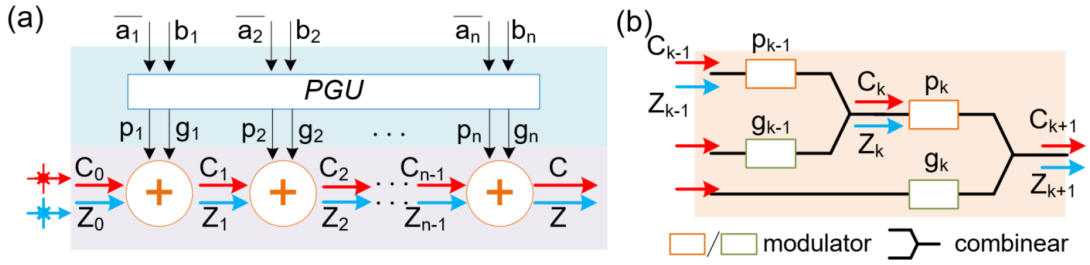
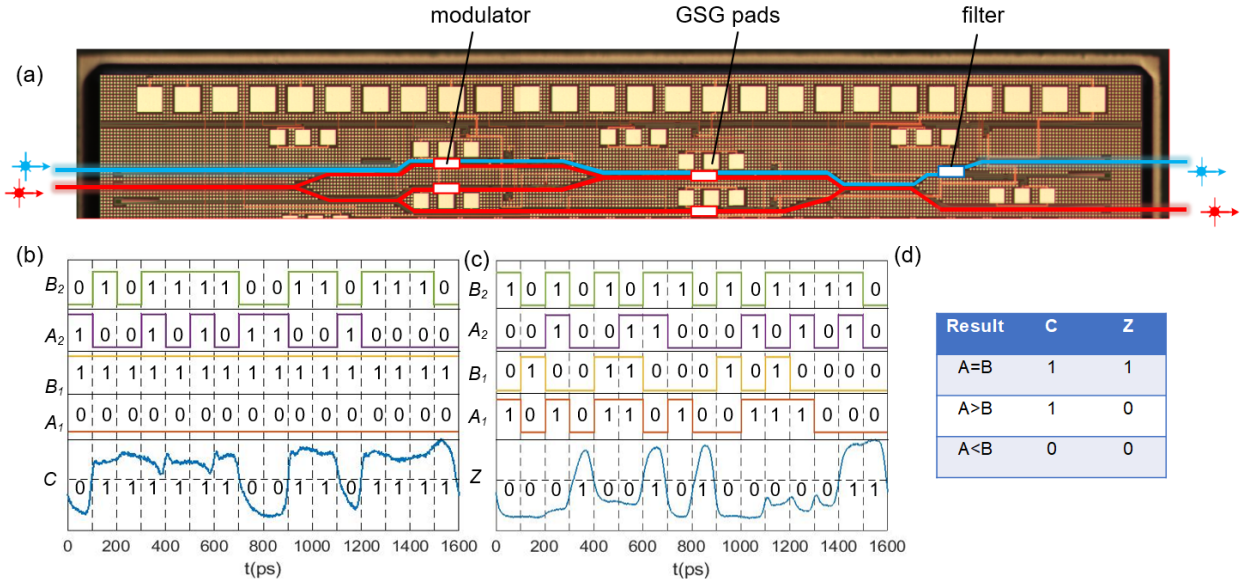


Fig. 1. (a) General schematic of (a) the EO comparator, (b) optical components and the optical paths of C and Z in the EO comparator.

Compared to transistor-based comparators, the critical path of our EO comparator is replaced by optical routes, which is one or two orders of magnitude faster than electrical counterparts. The performance of the entire module is determined by EO modulators, which can achieve high speed, small footprint, and ultralow energy consumption shown in previous works [5]. Furthermore, lights conveying results of the equality comparator and the subtractor transmit independently in the same waveguide and share a portion of EO logic gates, which reduces the number of logic gates and energy consumption as well.

3. Results

Figure 2(a) shows a micrograph of the optical comparator chip fabricated in the AIM foundry. Four high-speed microdisk modulators function as EO logic gates. High-speed pseudorandom non-return-to-zero (NRZ) signals are injected through GSG probes. The input lights with different wavelengths are generated by a tunable laser, which will convey the results of the equality comparator and the subtractor, respectively. An add-drop microdisk filter will separate these two lights at the output, where on-chip Ge photodetectors are deployed for next stage computation. Some portion of the light is coupled out and received by an oscilloscope. Part of the results at 10 Gbit/s operating speed is shown in Figure 2(b)(c), which fits well with the truth table shown in Fig. 2(d). More data at higher operating speed along with performance comparison with transistors-based circuits will be shown in the presentation.



Result	C	Z
A=B	1	1
A>B	1	0
A<B	0	0

Fig. 2. (a) Micrograph of the fabricated chip, (b) Testing results of the carry out *C*, operating wavelength is ~1542nm. (c) Testing results of the equality comparator *Z*, operating wavelength is ~1567 nm. (d) The truth table of the output signals of the EO comparator.

In conclusion, we have proposed a 2-bit optical comparator and demonstrated at 10 Gbit/s in experiments using high-speed microdisk modulators. WDM is introduced to optimize the number of EO modulators. We believe this design could contribute to future ultracompact optical computing with low power consumption and high computation speed.

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