Design of Tunneling Field-Effect Transistors Based on Staggered Heterojunctions for Ultralow-Power Applications

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***Abstract*—This letter presents the design of a tunneling FET with III-V-based tunnel heterojunctions for operation in digital circuits with supply voltages as low as 0.3 V. A representative implementation is predicted to achieve an ON-state current drive of 0.4 mA/μm with an OFF-state current of 50 nA/μm. Comparison with homojunction counterparts reveals that the hetero-tunnel-junction implementations may address better the design tradeoff between ON-state drive and OFF-state leakage.**

***Index Terms*—Staggered heterojunction, tunneling FET.**

I. Introduction

As MOSFET devices become aggressively scaled, the increasing OFF-state leakage has become an important concern in addition to the ON-state current drive. The non-scaling property of the OFF-state current in a conventional MOSFET device stems from thermionic injection at the source–channel junction. The resulting minimum 60-mV/dec subthreshold slope (SS) fundamentally limits the reduction of OFF-state current [1]. To overcome this barrier, novel transistor structures incorporating a tunneling junction between the source and the channel have been proposed [2]–[5] and experimentally demonstrated [6] to exhibit a sub-60-mV/dec SS. Tunneling field-effect transistors (TFETs) using type-II staggered heterojunctions have also been proposed in the strained Si/strained Ge material system [5]. In this letter, we propose an implementation utilizing III-V staggered heterojunctions for the source–channel junction to enable ultralow-voltage operation without compromising leakage. The flexibility of the heterointegration of diverse III-V materials allows a good balance between power consumption and performance. For the representative device design shown in this letter, indicated by simulations, the TFET is capable of working with a 0.3-V voltage supply with a 50-nA/μm OFF-state leakage and a 0.4-mA/μm ON-state current, due to the extremely steep turn-on enabled by the tunneling injection mechanism.

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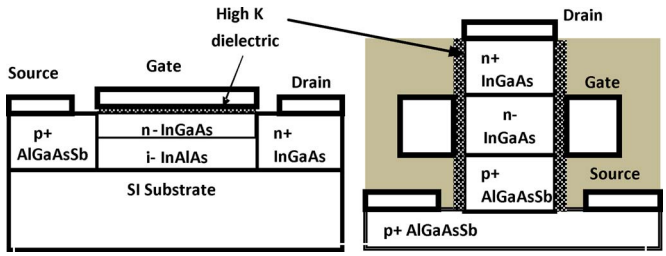

Fig. 1. Schematic drawing of the prototype TFET device with planar and multigate embodiments (not to scale).

In this letter, we first present a representative device design and its I–V characteristics; we then discuss the underlying device physics, illustrating why the staggered-heterojunction implementation is beneficial for ultralow-power applications.

II. Design of TFET Device

The layer structure of a representative TFET is schematically shown in Fig. 1. The device employs a high-k dielectric as the gate oxide (e.g., Al_2O_3), a 20-nm (thickness) $p^+(2 \times 10^{19}$ cm$^{-3})$ $Al_{0.5}Ga_{0.5}As_{0.3}Sb_{0.7}$ as source, a 10-nm $n^-(5 \times 10^{16}$ cm$^{-3})$ $In_{0.8}Ga_{0.2}As$ as channel, and a 20-nm $n^+(5 \times 10^{19}$ cm$^{-3})$ $In_{0.8}Ga_{0.2}As$ as drain. The barrier layer underneath the channel consists of undoped $In_{0.8}Al_{0.2}As$. We choose lattice-matched materials here to avoid the complicated stress and strain effects along both the transverse and the longitudinal directions. However, further design optimization may be achieved with the non-lattice-matched configurations. Embodiments of the planar device configuration shown in Fig. 1 may be implemented with the recently developed selective regrowth technique [7]. The presence of mixed group V materials in the AlGaAsSb compound may introduce challenges to the growth; however, this has been successfully demonstrated previously [8]. Another possible implementation may utilize a nanowire gate-all-around structure, which allows for more design flexibility (e.g., composition grading along the growth direction) as well as a scaled gate length in its fully depleted mode. It may also utilize technologies developed for FinFET or nanowire gate-all-around structures [9], [10]. The choice of the InGaAs/AlGaAsSb system is based on three considerations. First, a wide range of band lineup configurations can be provided, including a staggered lineup. Second, the band lineup can be varied over a wide energy range by tuning the material composition. A representative case is shown in Fig. 2. Third, lattice matching can be accomplished with a wide range of alloy compositions.

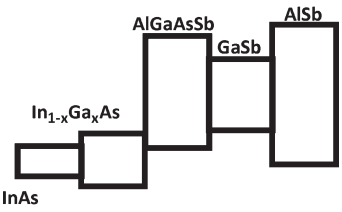

Fig. 2. Approximate band lineup for selected semiconductors.

TABLE I
MATERIAL PROPERTIES OF TFET MATERIAL
(PARAMETERS FROM [11] AND [12])

	Electron Affinity	m_{lh}/m_0	m_e/m_0	Lattice Constant	Eg (eV)
$Al_{0.5}Ga_{0.5}As_{0.3}Sb_{0.7}$	*3.6 eV*	*0.11*	*0.09*	*5.98 Å*	*1.36*
$In_{0.8}Ga_{0.2}As$	*4.73 eV*	*0.034*	*0.036*	*5.98 Å*	*0.50*

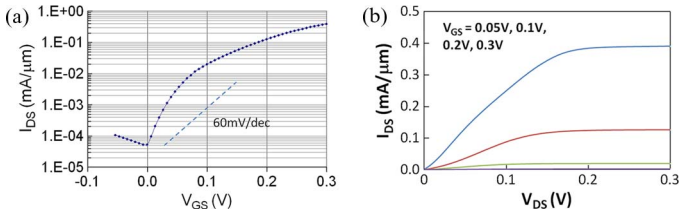

Fig. 3. (a) Transfer and (b) output characteristics of a TFET with AlGaAsSb p^+ source and InGaAs n^- channel.

The tunneling junction is formed between the AlGaAsSb source and the InGaAs channel. For this particular design, the gate length is 100 nm and is assumed to be perfectly aligned to the metallurgical junction. Material parameters are listed in Table I [11], [12]. The simulation of this device is carried out using Synopsis Sentaurus at 300 K; a two-band model is enabled for the band-to-band (BTB) tunneling computation [13]. Quantization along the transverse direction was not included in the simulation as the threshold voltage shift due to this effect may be compensated by proper material choice.

Shown in Fig. 3 are the representative transfer and output characteristics of this device design. The device is biased with $V_{\rm dd} = 0.3$ V for ultralow-power applications. A metal work function of 4.61 eV is assumed, which provides the appropriate threshold voltage. The Sentaurus modeling parameters were validated by the analysis of the two-band BTB direct-tunneling process (discussed in the next section), using the physical parameters listed in Table I. A sub-60-mV/dec SS is exhibited over several decades of current, giving the device a very sharp turn-on. The expected ambipolar turn-on characteristics are also shown in the negative bias range. For reference purposes, the best possible conventional FET turn-on characteristics (60 mV/dec) are also shown in the figure. With the use of a gate dielectric of 0.6-nm EOT, this device provides an ON-state current drive of 0.4 mA/μm at an OFF-state current of 50 nA/μm and therefore achieves an on–off current ratio $\sim 10^4$, over a small voltage swing of 0.3 V. It is also noted that,

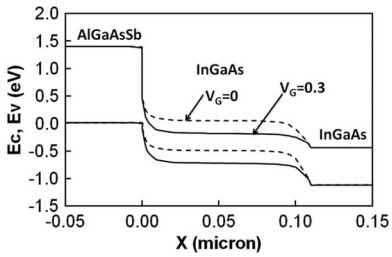

Fig. 4. Representative energy-band diagram under OFF state (zero gate bias) and ON state (0.3-V gate bias), both with 0.3-V drain bias. A source quasi-Fermi level is used as reference ($E_{\rm fs} = 0$).

for the output characteristic, the simulation predicts a super-linear I–V behavior in the triode regime, which is a combined result of nonlinear dependence of tunneling probability on $V_{\rm DS}$ and a changing balance between the tunneling currents along the forward and backward directions as $V_{\rm DS}$ is varied.

III. DEVICE PHYSICS OF TFET

The energy-band diagrams of the TFET under different bias conditions are shown in Fig. 4, under zero gate bias (OFF state) and high gate bias (ON state) and both with high drain bias. The band bending in the source (a few millielectronvolts) is not visible on this scale. As shown, BTB tunneling is suppressed in the OFF state due to lack of final states at appropriate energies, while it is enabled with high gate bias. Both heavy and light holes are involved in this BTB process; however, light holes contribute to the majority of the current due to their higher tunneling probabilities under low-bias condition.

For a TFET design to be useful for ultralow-power applications, high ON-state current and low OFF-state leakage must be simultaneously achieved. To obtain high ON-state current, a significant tunneling probability is needed at a relatively low electric field at the tunneling junction limited by the small gate-to-source bias. To understand the implication of this criterion on material choice, we first examine homojunction embodiments with different materials.

The tunneling probability is obtained with a two-band model [15] and WKB approximation, where the evanescent wave vector and the tunneling probability are given by (1), shown at the bottom of the page, and

$$T = \exp\left(-2\int_0^{d_{\rm tunnel}} \kappa dx\right) \tag{2}$$

where E is the electron energy with respect to the local valence band energy, m is the electron mass, $d_{\rm tunnel}$ is the tunneling distance, and P is the matrix element of the momentum operator between the conduction band and light-hole band Bloch functions ($P = \langle u_{0,v}|\hat{p}|u_{0,c}\rangle$) and may be readily obtained via $m/m_c* = [1 + 2P^2/(mE_g)]$, where m_c^* is the conduction band effective mass.

$$\kappa = \mathrm{Im}(k) = \frac{\sqrt{2m}}{\hbar}\sqrt{\sqrt{\left(E - \frac{1}{2}E_g + \frac{P^2}{m}\right)^2 + E(E_g - E)} - \left(E - \frac{1}{2}E_g + \frac{P^2}{m}\right)} \tag{1}$$

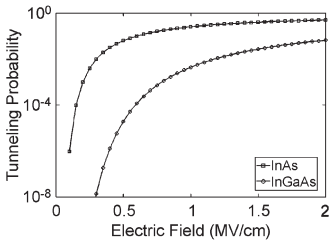

Fig. 5. BTB tunneling probability versus electric field for $In_{0.47}Ga_{0.53}As$ and InAs materials.

Shown in Fig. 5 is a comparison of the tunneling probability of a band-edge electron ($k_{//} = 0$) as a function of the electric field between wide-bandgap ($In_{0.47}Ga_{0.53}As$, $E_g = 0.75$ eV) and narrow-bandgap (InAs, $E_g = 0.36$ eV) materials. The result shows that a small E_c, E_v separation is needed at the tunneling junction to achieve a high tunneling probability. This point is physically intuitive: The smaller the spacing between E_c and E_v at the tunneling junction, the smaller the magnitude of evanescent wave vector (1) and, thus, the larger the tunneling probability (2). For homojunction embodiments, the requirement of a significant tunneling probability limits the material choice to narrow-bandgap semiconductors.

However, homojunction embodiment using a narrow bandgap may have difficulties satisfying a low OFF-state leakage criterion. As pointed out in [4], although BTB tunneling may be sufficiently suppressed, leakage current due to thermal generation, which is proportional to $\exp(-E_g/nkT)$, may indeed dominate the OFF-state current and limit the on–off ratio to a few hundreds due to the small E_g used.

Given these considerations, we employ a staggered heterojunction as the source–channel junction in our TFET design. The E_c, E_v separation at the tunneling junction is chosen to be 0.23 eV, while the energy bandgaps for the individual materials are greater than 0.5 eV. With such configuration, a high tunneling probability may be achieved at a relatively low electric field (0.23-eV E_c, E_v separation), whereas the thermal generation issue is alleviated as individual energy bandgaps may be chosen to have greater values. The design conflict between high ON-state current and low OFF-state leakage seen in the homojunction implementation is greatly relaxed.

To illustrate the improvement, we compare the tunneling current densities of reverse-biased p^+-n junctions using staggered heterojunction (same as in the TFET design) and homojunction ($In_{0.8}Ga_{0.2}As$) implementations. The tunneling current, in the spirit of Landauer's formalism [14], may be expressed as

$$J = q \int v_x(k_x, k_{//}) \bullet g_{\rm sd}(k_{//}) \bullet T(k_x, k_{//}) \bullet \left[f_s(\vec{k}, E_{\rm fs}) - f_d(\vec{k}, E_{\rm fd}) \right] \bullet d\vec{k} \quad (3)$$

where k_x and $k_{//}$ are the transport-direction and in-plane wave vectors, respectively, $T(k_x, k_{//})$ is the tunneling probability, and $g_{\rm sd}$ is the joint density of states. At a given bias voltage, the potential profile is computed using depletion approximation. The current is obtained with the potential profile by integrating through all states within the p^+ source.

Shown in Fig. 6 is a computed result of the tunneling current density for various implementations using a two-band model for tunneling probability. Also, shown in the figure is the Sentaurus simulation result for the same structure. The Sentaurus parameters are validated to reflect the tunneling property of the staggered heterojunction. It is seen that a staggered heterojunction offers ~100 times enhancement in the tunneling current if the generation current were to be kept about the same (by having the same minimum bandgap).

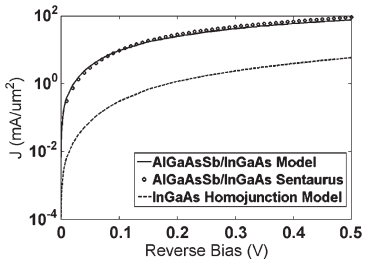

Fig. 6. BTB tunneling current for reverse biased p^+-n junctions using a staggered heterojunction and homojunction. The symbol is the Sentaurus simulation result for the same staggered-heterojunction embodiment.

IV. Conclusion

In this letter, we present a design of a TFET based on staggered heterojunctions that is suitable for ultralow-power-supply applications. For a representative design, with a 0.3-V supply voltage, the device is predicted to be capable of delivering a 0.4-mA/μm current at ON state with an OFF-state current of 50 nA/μm. Analysis suggests that the staggered-heterojunction embodiment of the TFET may offer a better design compromise in terms of performance and power consumption than its homojunction TFET counterpart.

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