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Integrated One Diode–One Resistor Architecture in Nanopillar SiO_x Resistive Switching Memory by Nanosphere Lithography

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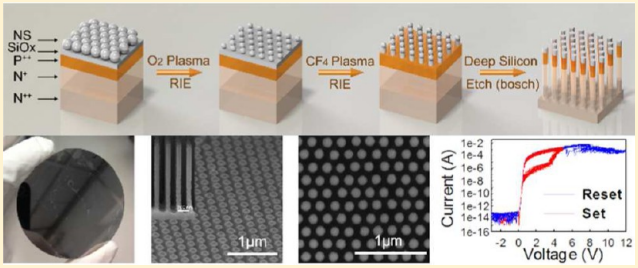
Supporting Information

ABSTRACT: We report on a highly compact, one diode–one resistor (1D–1R) nanopillar device architecture for SiO_x-based ReRAM fabricated using nanosphere lithography (NSL). The intrinsic SiO_x-based resistive switching element and Si diode are self-aligned on an epitaxial silicon wafer using NSL and a deep-Si-etch process without conventional photolithography. AC-pulse response in 50 ns regime, multibit operation, and good reliability are demonstrated. The NSL process provides a fast and economical approach to large-scale patterning of high-density 1D–1R ReRAM with good potential for use in future applications.



KEYWORDS: *1D–1R, ReRAM, Nanosphere Lithography, SiO_x, nanopillar*

In recent years, resistive random access memory (ReRAM) has drawn much interest as a promising candidate for next generation nonvolatile memory due to its potential scalability beyond 10 nm feature size using a crossbar structure, fast switching speed, low operating power, and good reliability.[1−3] Traditional charge-based nonvolatile memory (NVM) typically includes a charge "trapping layer" within a transistor configuration that requires a high thermal budget and large footprint (typically $6F^2$, where F = minimum feature size).[4,5] Resistive switching (RS) memory operates by controlling device resistance with an external electrical manipulation,[6−9] leading to better electrical performance, smaller design area ($4F^2$), and excellent cycling endurance.[10] Resistive-based memories are a new class of devices compatible with applications that go beyond traditional electronics configurations, for example, three-dimension (3D) stacking, nano-battery, neuro-electronics and Boolean logic operations.[11,12,13,14−17]

There have been many studies of binary-metal oxide resistance switching characteristics,[17,18] which can have operating instability issues due to difficulty in controlling stoichiometric compositions.[19,20] Therefore, a simple process that is compatible with conventional CMOS fabrication allows multilayer compositional engineering and provides good electrical stability and high yield are critical requirements for ReRAM commercialization.[21] Silicon oxide (SiO_x) has long been used as gate dielectrics for metal–oxide–semiconductor field-effect transistors. In addition to its excellent insulating properties, SiO_x-based resistive switching phenomena have been observed as early as 1962 by Hickmott and 1967 by Simmons and Verderber and have further been modeled by Dearnaley in the 1970s.[22−24] They observed that a simple M–I–M structure (ex. Au/SiO_x/Al) can form an active device based on its repeatable negative resistance phenomenon. Recently, Yao et al. have reported SiO_x-based resistive switching behaviors in vacuum (1R), indicating that this traditionally passive material can be converted to an active memory element and controlled by external electrical activation.[25−27] Furthermore, G. Wang et al. report an integrated Schottky diode-1R configuration that demonstrates high performance and low power in a 1k-bit array for potential circuit-level applications.[28] However, considering the static power consumption and sneak-path issues in large-scale, crossbar array designs,[29−31] a Schottky-diode is not suitable for portable electronics due to its high reverse-bias leakage current and relatively low reverse-bias breakdown voltage as compared to a Si-based PN-diode or transistor.[32−34] For example, the reverse leakage current of Schottky diodes can increase dramatically with temperature to the point of a

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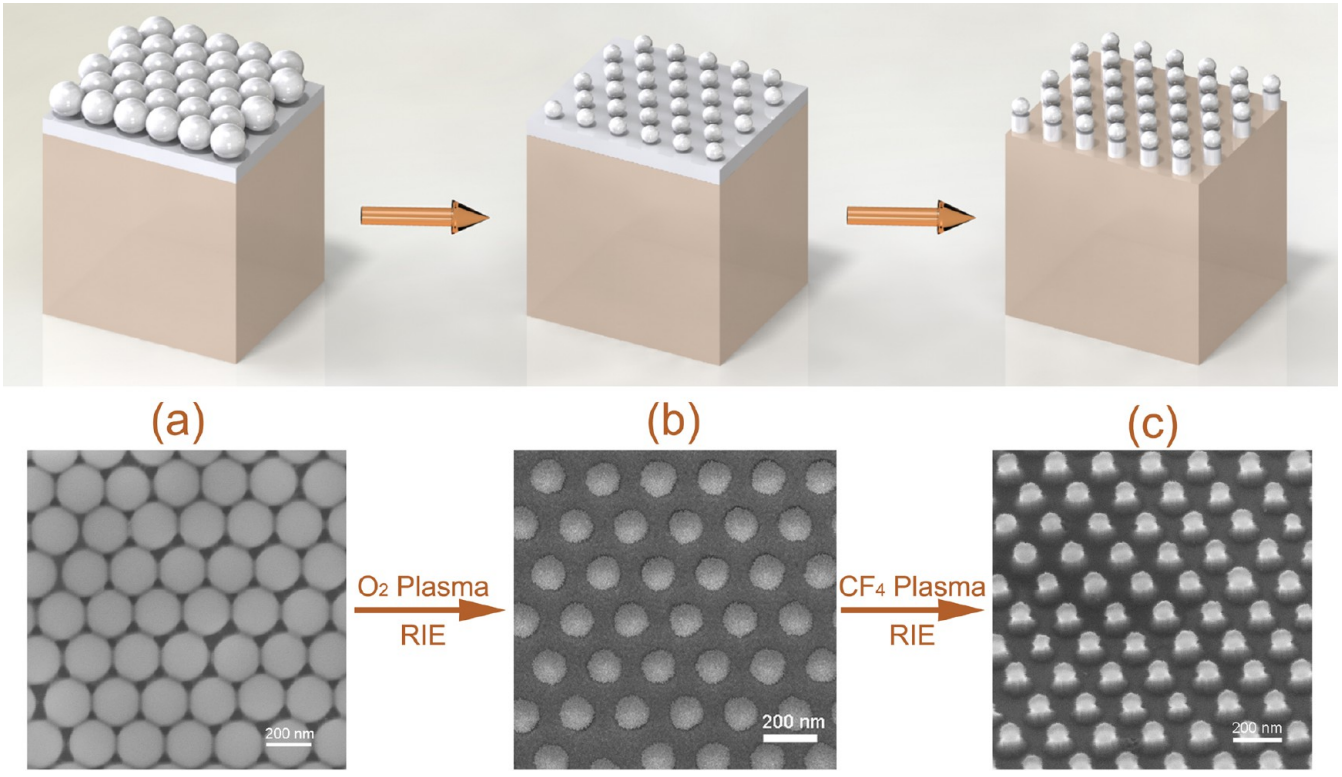

Figure 1. The 1R process flow using nanosphere (NS) lithography: (a) NS deposition on 60 nm thick SiO_x and N^{2+} Si substrate as a bottom electrode. (b) RIE oxygen plasma shrinks the diameter of polystyrene NSs. (c) The 1R array is formed by SiO_x RIE to transfer the NS pattern into the SiO_x layer to complete 1R formation.

thermal-runaway situation,[35] potentially resulting in instability issues and readout failures.

In this work, a Si diode (1D) with low reverse-bias current is integrated with a SiO_x-based memory element (1R) using nanosphere lithography (NS lithography, or NSL) and deep-Si-etching (DES) to pattern a $P^{2+}/N^{+}/N^{2+}$ epitaxial Si wafer. The self-aligned process forms a high density, large-scale nanopillar (NP) array architecture. Compared with conventional photolithography or direct-writing methods (such as electron beam lithography or focused ion beam milling), NSL has emerged as a low-cost (maskless), high-throughput alternative technique to pattern large areas.[36−39] The nanostructures fabricated using NSL can be well-controlled in shape, size, and interpillar spacing through direct assembly of polymer nanospheres on the wafer-scale. Performance of 1R and 1D−1R structures are characterized and show that the integrated nanopillar 1D−1R configuration offers low static-power for suppression of sneak-path issues. The work reported here provides an efficient fabrication process and low reverse-bias current in a SiO_x-based 1D−1R configuration for potential use in future ultralarge-scale NVM applications.

Experiment. Figure 1 illustrates the process flow for a 1R SiO_x-based ReRAM with sequential scanning electron microscope images (Zeiss Neon 40 SEM) of the evolving structures. The detailed procedure of 1R SiO_x-based ReRAM array fabrication begins with e-beam evaporation (PVD, CHA Industries) of 60 nm of SiO_x (measured by ellipsometer) on a N^{2+} (100) Si substrate ($1-7 \times 10^{19}$ cm^{-3}, resistivity of 0.001−0.005 ohm-cm) used as a bottom electrode. The SiO_x acts as the 1R element and as a hardmask for self-aligned 1D nanopillar fabrication (as describe further below). Next, the PVD-SiO_x layer is treated in an oxygen plasma reactor to obtain a hydrophilic surface. 18 MΩ DI water and 200 nm polystyrene nanospheres (Polysciences, Inc.) were used for nanosphere mask preparation. The 200 nm nanosphere was chosen due to a trade-off between minimum feature size and larger-scale uniformity as described in Supporting Information Figure S1. Polystyrene nanosphere solution was dropped on top of microscope coverslips. This was then introduced to air−water interface in a Petri dish filled with 18MΩ DI water. The polystyrene solution spreads out at the air−water interface forming a monolayer. Prior to monolayer formation, a prepared silicon substrate with SiO_x coating was immersed at the bottom of a Petri dish. The monolayer was then transferred to an immersed substrate by slightly lifting the substrate. Then the sample was dried in air. The diameter of each NS in the monolayer was reduced by reactive ion etching (Oxford 80 RIE) in oxygen-plasma (80 sccm O_2; power 60 W; pressure 100 mT; 1 min). The power, partial pressure, and time of etching were optimized to obtain the desired size (Figure 1b and Supporting Information Figure S2). The 1R array is formed by RIE (5 sccm Ar + 5 sccm O_2 + 80 sccm CF_4; power 100 W; pressure: 200 mT) to transfer the treated NS pattern into the SiO_x layer (Figure 1c with average diameter of about 150 nm, see Supporting Information Figure S2). The NS layer was removed by bath sonication in water for 15 min. For the 1D−1R structure, a $P^{2+}/N^{+}/N^{2+}$ epitaxial Si wafer is used as the substrate (P^{2+}, thickness 0.3 um, boron (B), concentration 5×10^{19} cm^{-3}; N^{+}, thickness 0.6 um, arsenic (As), concentration 5×10^{16} cm^{-3}; N^{2+}, substrate, phosphorus (P), concentration $1-7 \times 10^{19}$ cm^{-3}). On the basis of the 1R array, nanopillars are obtained via Bosch deep silicon etch process (Versaline Deep Silicon Etch System, Plasma-Therm Inc.) as shown in Supporting Information Figure S3. A tungsten (W) probe tip

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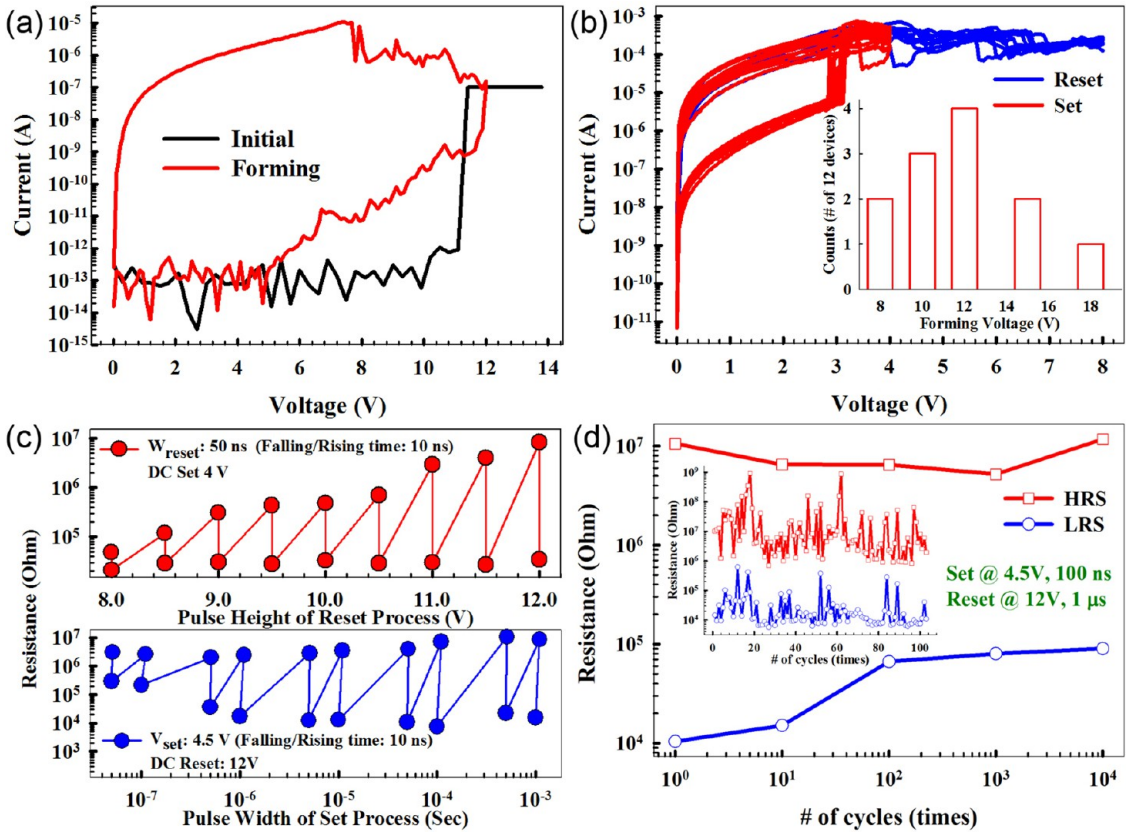

Figure 2. DC sweep resistive switching behaviors and ac pulsed response of 1R element: (a) Electrical soft-breakdown process with 100 nA compliance current limit, and forward/backward voltage sweep electroforming process. (b) Ten $I-V$ resistive switching set/reset cycles. The inset shows the measured electroforming voltage distribution. (c) The ac pulsed switching properties with fixed reset pulse width (dc Set) and fixed set pulse height conditions (dc Reset). (d) HRS and LRS endurance data during ac voltage cycling. At least a one-order-of-magnitude resistance ratio is maintained after 10^4 cycles.

(~10 um radius) was used as a top electrode, and a Lake Shore Cryotronics vacuum probe chamber (<1 mTorr) and Agilent B1500A device analyzer were used for electrical test. $I-V$ data were collected using AC pulse and forward/reverse DC sweeps: the Set process programs the device to a conductive, low-resistive state (LRS); the Reset process programs each device to a low-conductance, high-resistive state (HRS) having lower conductance as reset stop voltage is increased.

Results and Discussions. Figure 2 shows $I-V$ characteristics of direct current (dc) sweep and alternating current (ac) pulse response for SiO_x-based 1R array fabricated by NSL. Voltage was applied to the top electrode (W probe tip) with bottom electrode (N^{2+} Si substrate) at ground. All testing was done in vacuum. To establish reversible switching in these devices, a two-step electroforming process was used: (1) a current-limited voltage sweep to induce soft breakdown; and (2) a forward/backward voltage sweep to electroform the device. The soft-breakdown process is done by sweeping the voltage until current dramatically increases to a compliance current limit (CCL), typically 100 nA in this work. Generally, this process avoids hard breakdown and increases electroforming yield in most types of ReRAM devices.[8,17] For the SiO_x-based ReRAM devices used here, a second electroforming step was done using a forward/backward voltage sweep (Figure 2a), where current fluctuations are observed to increase to above the CCL during the forward voltage sweep. Electroforming is completed during the backward voltage sweep from the forming voltage (about 8–18 V within 12 devices, inset of Figure 1b) to 0 V, resulting in a LRS. After the electroformation, resistive switching performance is stabilized by cycling the device multiple times using voltage sweeps (Figure 2b). The Set process is a 4 V forward/reverse sweep without any CCL to program the device to the LRS. The Reset process is done by sweeping the voltage to 8 V, where the current decreases as the voltage is swept from about 5 to 8 V and the device is programmed into an HRS. The HRS/LRS resistance ratio is at least ~50 at 1 V bias, which satisfies sensing requirements.[3,32] Figure 2c demonstrates the ac pulse response for Set and Reset programming in the 50 ns regime where HRS and LRS resistance values are controlled by applied pulse height and pulse width, thus potentially enabling multilevel programming in a single memory cell. Figure 2d shows HRS and LRS resistance values during 10^4 switching cycles. A resistance ratio of at least 1 order of magnitude is maintained, although soft-errors were observed during the first 100 cycles (inset of Figure 2d). It may be noted that the electroforming voltages measured here (~12 V) are somewhat lower than those measured in previous work on MOSCAP device architectures[40,41] and are near the voltage used in the Reset process (8 V). This could be due to creation of electrically active defects near the SiO_x sidewall during the RIE process that may lower the soft breakdown threshold and reduce the filament formation energy during the subsequent electroforming process. Also, the reset voltage (i.e., the voltage at which LRS current begins to decrease) is always greater than or equal to the set voltage (where current increases sharply), which is a unique character-

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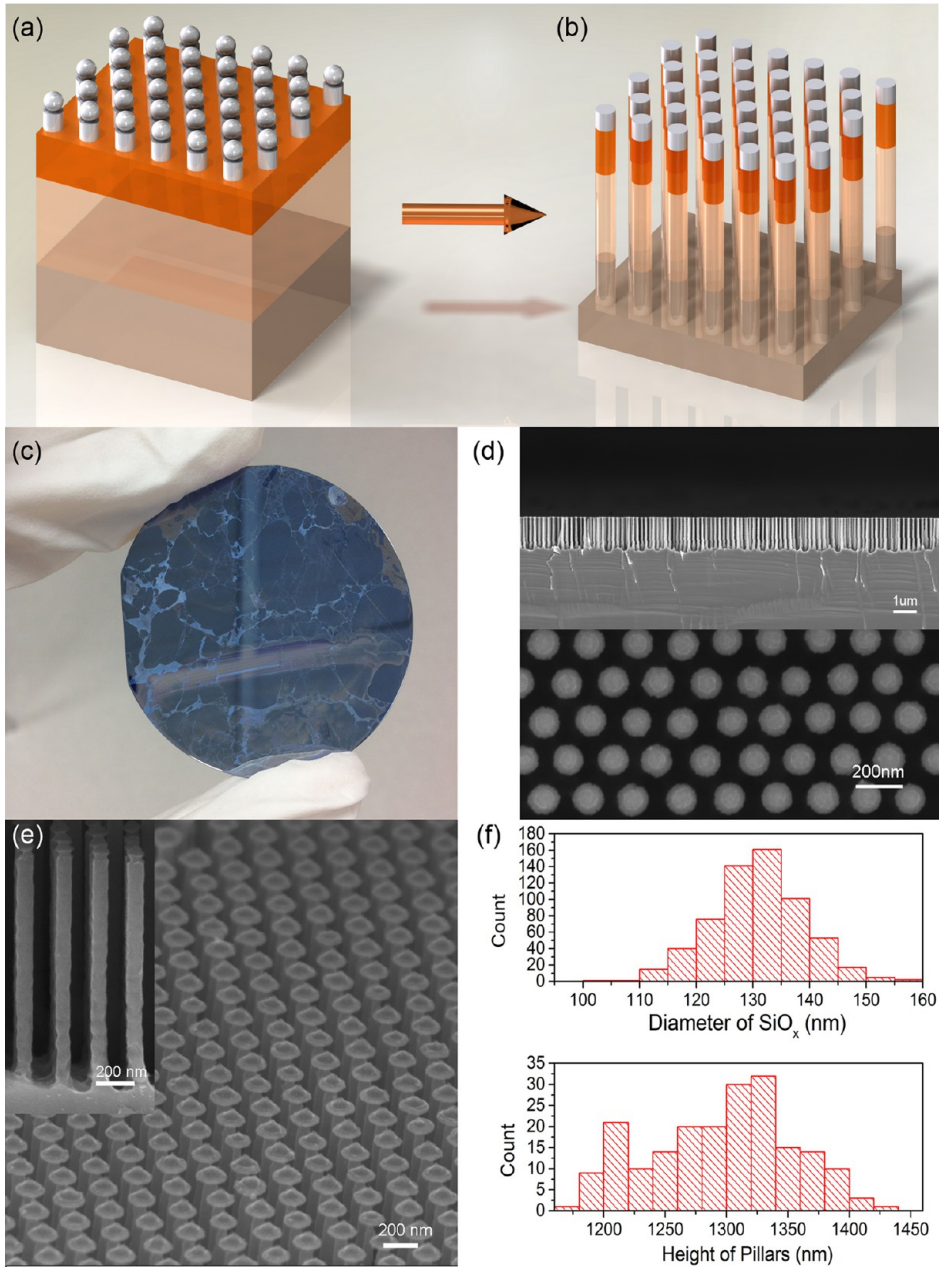

Figure 3. The 1D−1R fabrication procedure using DSE and device electrical characteristics: (a) transfer of NSL pattern to SiO_x hard-mask on epitaxial Si $P^{2+}/N^{+}/N^{2+}$ wafer. (b) DSE process in Bosch mode to form a self-aligned 1D−1R NP architecture. (c) Wafer-scale and (d,e) SEM images of 1D−1R NPs. (f) Statistical distribution of nanopillar diameter and height.

istic of SiO_x-based ReRAM as compared to other material systems.[18] The difference between reset and set voltages can potentially be controlled by optimizing the series resistance in the circuit and choice of electrode materials.[41]

Figure 3 illustrates the 1D−1R NP fabrication process and shows SEM images of a NP array. Nanopillars are formed and separated by the DSE process in Bosch mode, which contains three steps: (1) polymer deposition; (2) polymer etching; and (3) Si etching (Supporting Information Figure S3 shows the procedure in detail). The etch time and power in the Bosch process were optimized to reduce sidewall scalloping (Figure 3b and Supporting Information Figure S4). Figure 3c shows a 2 in. wafer used to demonstrate the 1D−1R fabrication process using an epitaxial 1D structure. Additional work is in progress to optimize the across-wafer uniformity of the NSL and DSE processes. The 1D−1R nanopillar SiO_x ReRAM architecture was imaged using SEM (Figure 4d−f). The average nanopillar height and diameter are 1.3 μm and 130 nm, respectively.

Figure 4a shows the $I-V$ response of 100 voltage sweeps from −3 to +3 V for a NP 1D configuration. The forward current can reach 100 mA at 3 V, which indicates a forward current level high enough to support the Reset process. The reverse current is below 1×10^{-12} A at −3 V. As mentioned previously, compared with Schottky diodes, the advantages of Si-based PN diodes are low reverse-current, high reverse-bias breakdown voltage, and fewer stability issues. The reverse current level is reduced by at least three-orders of magnitude compared with a previous report while maintaining good reliability.[28] The simulation fitting results indicate that the defect concentration is about 1×10^{-15} cm^{-3} (using a simple

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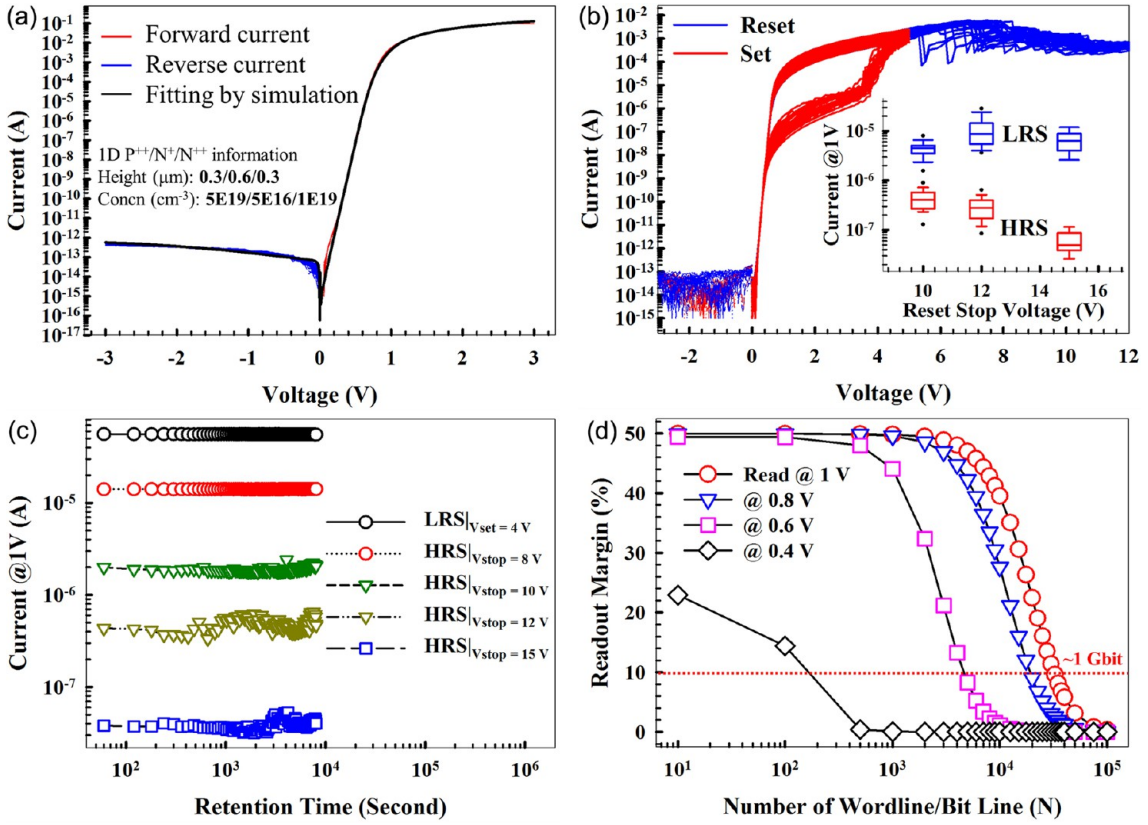

Figure 4. The 1D−1R electrical characteristics when using NSL and DSE. (a) On hundred measurement cycles of diode *I*−*V* behavior and simulation results of 1D structure. (b) Thirty resistive switching *I*−*V* cycles in 1D−1R structure. The inset shows the readout current in LRS and HRS at 1 V as a function of reset stop voltage. (c) Retention measurement results of multistate programming obtained by controlling the reset stop voltage. (d) Normalized readout margin as a function of the number of word/bit lines for different readout voltage in NP 1D−1R configuration.

assumption of midgap traps), which is expected due to the epitaxial quality of each layer. The quality of 1D stacked layers (epitaxy, diffusion, or implantation) can dramatically affect diode reverse or forward current characteristics, as well as power consumption and readout margin issues (described below). Also, the chosen $P^{2+}/N^{+}/N^{2+}$ configuration has high reverse breakdown voltage (>30 V), which is important for SiO_x-based ReRAM operation. The concentration of each epitaxial layer strongly affects diode *I*−*V* characteristics due to the carrier injection characteristics, whereas NP height and diameter have minor effects. Figure 4b shows *I*−*V* curves of 30 switching cycles for a SiO_x-based 1D−1R NP structure. The required forming voltage is similar to the 1R structure. However, the switching voltage values for Set and Reset processes in 1D−1R are larger than in 1R, and the current transition at the switching point is more gradual, possibly due to the series connection of 1D and 1R elements. By controlling the reset stop voltage, the HRS level can be controlled and the potential for multibit operation can be demonstrated for NP SiO_x-based ReRAM (inset of Figure 4b and Supporting Information Figure S5). Compared to our previous studies, the HRS current here is significantly larger than in simple MOS ($TaN-SiO_x-N^{2+}$ Si wafer) structures (shown in Supporting Information Figure S6), possibly due to plasma-etching-induced defect formation in the SiO_x layer.[40−42] Plasma etching processes (RIE or DSE) can result in a more defective insulator causing increased leakage current in the 1R element. It should be emphasized that a W probe tip is used as the top electrode for the 1D−1R structures. As a result, the probe tip contacts ~7800 nanopillars based on the deposited NS pitch (200 nm) and probe tip radius of 10 μm. Because we expect that only a single filament is activated during the electroforming process, the large HRS current is possibly due to the multiple parallel leakage paths in the NP array. Additional investigations by controlling RIE process, the oxygen content of SiO_x, and measuring an individual NP 1D−1R structure are ongoing and will be described in future reports. Changing the oxygen-content of the 1R element by controlling oxygen flow during sputtered deposition of the SiO_x layer can possibly enlarge the HRS/LRS ratio and stabilize switching characteristics.[42] Figure 4c shows multilevel retention performance of SiO_x-based 1D−1R NP arrays obtained by controlling the stop reset voltage from 8 to 15 V. The readout current of LRS and HRS is measured at 1 V for every 60 s after each Set and Reset programming operation. The retention reliability test shows stable multilevel operation, and no degradation is observed for more than 10^4 s, confirming the nonvolatile nature of the SiO_x-based 1D−1R NP devices. For circuit-level applications, low reverse current, larger HRS/LRS resistance ratio, and low readout current are desirable for large-scale ReRAM production. Low reverse-current can reduce the sneak-path leakage issue and provide larger readout margin, especially in large arrays.[30,31,33,34] Large HRS/LRS ratio provides the potential for multibit operation with a small-footprint cell ($<4F^2$) and reduces the chance for soft-errors. Nonlinear current response (e.g., one selector and one resistor configuration, 1S−1R) is preferred for low-power applications.[32] In our case, a 10% readout-margin can support a 1Gbit

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array due to the low reverse-biased diode current and large LRS/reverse-current ratio (Figure 4d). The results demonstrated here provide significant benefits by simplifying the ReRAM fabrication process and potentially enabling compatibility with high-volume CMOS manufacturing.

Summary. In summary, we have demonstrated high-density, wafer-scale 1D−1R nanopillar SiO_x-based ReRAM fabricated by nanosphere lithography. Excellent resistive switching characteristics and reliability are observed, the AC pulsed switching speed is in the 50 ns regime and multibit operation is demonstrated. The Si-based epitaxial 1D NP structure was formed by using a deep-Si-etch process. Low reverse-bias diode current and nonlinear $I-V$ characteristics help reduce sneak-path issues and further improve the readout margin in practical large-scale array designs up to 1 Gbit in size. The demonstrated technology has great potential not only for maskless electronics but also provides a fast and economical solution for wafer-scale manufacturing of high-density 1D−1R ReRAM arrays.

■ ASSOCIATED CONTENT

Supporting Information

Materials and methods, Bosch process flow, and electrical properties. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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