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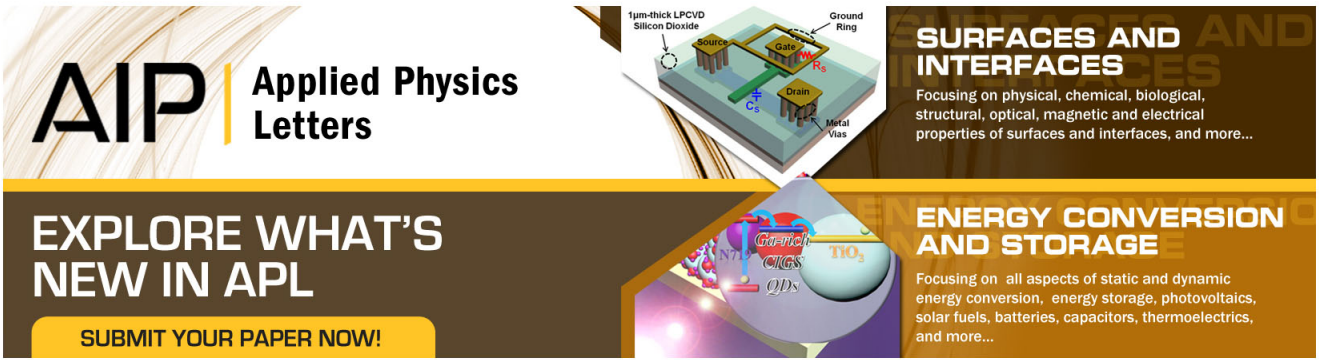

Direct measurement and characterization of n^+ superhalo implants in a 120 nm gate-length Si metal–oxide–semiconductor field-effect transistor using cross-sectional scanning capacitance microscopy

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We have directly measured nanoscale electronic features associated with a 120 nm physical gate length *p*-channel silicon metal–oxide–semiconductor field-effect transistor device structure including n^+ superhalo implants using cross-sectional scanning capacitance microscopy (SCM). A dc bias-dependent voltage series of SCM images representing nine bias conditions from 2 to -2 V in 0.5 V steps was obtained. The SCM contrast observed varies with the ac and dc bias applied to the sample and allows delineation of the device features, including the p^+ source and drain contacts, p^+ source and drain extensions, p^+ polycrystalline silicon gate, electrical $p-n$ junction, *n*-well, and n^+ superhalo implants. It is demonstrated that the superhalo implant features are imaged only under specific SCM bias conditions. Detailed analysis of the resulting SCM contrast indicates an apparent channel length of 73 ± 11 nm, and reveals clear asymmetry in the individual lobes of the n^+ superhalo implant features. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1522819]

As scaling of silicon metal–oxide–semiconductor devices extends to gate lengths of 0.1 μm and below, fundamental limitations in gate oxide thickness and supply voltage nonscaling issues become apparent.[1,2] Recently, advances have focused on channel engineering utilizing superhalo ion implantation, which results in both vertically and laterally nonuniform two-dimensional (2-D) profiles to overcome short channel effects.[3,4] Cross-sectional scanning capacitance microscopy (SCM)[5] and spectroscopy[6] have been used as powerful metrology tools in actual Si device structures. We have used SCM imaging, over a range of applied sample bias voltages, to clearly delineate the individual device regions in a deep-submicron *p*-channel Si metal–oxide–semiconductor field-effect transistor (*p*-MOSFET), including n^+ superhalo implants. The contrast obtained allows us to image the n^+ superhalo implants and to demonstrate direct measurement of apparent channel length in Si device structures with complex 2-D channel doping profile.

SCM imaging was performed using a Digital Instruments Dimension 3100 atomic force microscope (AFM) with SCM capacitance sensor electronics. The basic concepts of cross-sectional SCM imaging have been described elsewhere.[5,6] The ac bias (V_{ac}, typically 1 V peak-to-peak, applied at frequency 90 kHz) and dc bias (V_{dc}) were applied to the sample (tip is grounded), and the imaging was performed in standard dC/dV open loop magnitude-mode,[5,7] employing commercially available CoCr-coated silicon AFM tips. The sample topography is simultaneously obtained using conventional contact mode AFM.

A schematic of the *p*-MOSFET sample employed is shown in Fig. 1(a). The device gate width is 10 μm, and cross-sectional scanning electron microscopy (SEM) reveals the fabricated physical gate length to be approximately 0.12 μm. Following the *n*-well implant and p^+ poly-Si gate patterning, the n^+ superhalo implants were formed using large tilt angle arsenic implantation. Boron source and drain extensions were then implanted followed by oxide sidewall spacer patterning, boron source and drain contact implants, and silicide formation. Additional details of the device fabrication process are described elsewhere.[3,4]

The sample was prepared for imaging using established SCM cross-sectional sample preparation techniques.[6,7] The 10 μm device gate width hinders the fabrication of a metal contact to the cross-sectional surface to ground all device

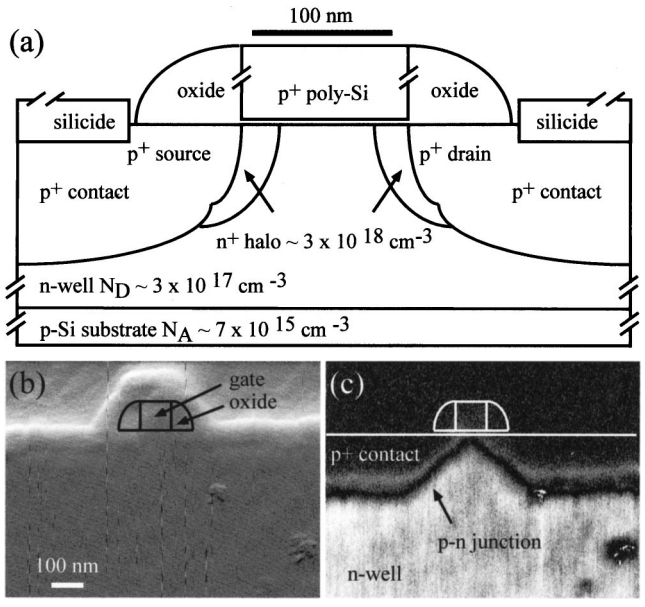

FIG. 1. (a) Schematic diagram of the *p*-MOSFET superhalo structure. (b) Cross-sectional topography (deflection data, gray scale = 0.01 V). (c) Corresponding SCM image with $V_{ac}=1$ V (peak-to-peak) and $V_{dc}=0$ V. The gray scale is 5 V. In (b) and (c) the locations of the poly-Si gate and oxide spacers are indicated, and in (c) the Si surface is indicated by a solid line.

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regions.[6,8] Instead, the sample substrate was thinned and an 800 nm Al layer was deposited on the back plane before mounting the device for mechanical polishing. The final surface preparation consisted of a colloidal silica polish followed by a low-temperature UV ozone oxidation.[6,9]

The cross-sectional sample topography (deflection data) of the p-MOSFET device is shown in Fig. 1(b). The trapezoidal feature comprises the transistor poly-Si gate, oxide sidewall spacers, and oxide/nitride layer. This feature allows the transistor active device region to be located in cross section. No additional topographic features are regularly visible.

The corresponding magnitude-mode SCM image under bias conditions $V_{ac}=1$ V and $V_{dc}=0$ V is shown in Fig. 1(c). The SCM features reveal the basic device structure and reflect the free carrier concentration in each device region. The electrical $p-n$ junction is evident as the dark nodal line traversing the image. The p^+ contact and source/drain extensions are displayed as the graded light band, located above and parallel to the $p-n$ junction. The dark gray area under the top silicon surface (p^+ contact region) corresponds to the metallic silicide layers and heavily doped p^+ contact region.

To further delineate the active device region of the p-MOSFET a V_{dc} bias-dependent voltage series of magnitude-mode SCM images was acquired. These data were obtained sequentially after the data presented in Figs. 1(b) and 1(c), utilizing the same AFM tip. This series of images was obtained with V_{ac} held constant at 1 V while V_{dc} was swept from 2 to -2 V in 0.5 V steps with an SCM image acquired at each voltage step. The V_{dc} bias-dependent voltage series therefore represents nine individual bias conditions. For dc bias voltages outside of this range ($V_{dc}>2$ V or $V_{dc}<-2$ V), we observed anomalous topographic features and corresponding SCM features, presumably due to charge injection into the oxide. Once present, these features persist and can obscure the device features of interest, preventing meaningful subsequent imaging. The bias voltage series exhibits the V_{dc} bias dependence and evolution of dC/dV contrast expected based on modeling of the tip-sample system as an MOS capacitor (MOS-C).[6,10,11]

Figure 2 shows a subset of the nine SCM images from the V_{dc} bias-dependent voltage series, at four specific bias voltages ($V_{dc}=0$, -0.5, -1.0, and -1.5 V) that demonstrate the SCM conditions necessary for the n^+ superhalo implants to be imaged. The simultaneously obtained topographic images were similar to that shown in Fig. 1(b). At $V_{dc}=0$ V [Fig. 2(a)] the transistor structure is evident. The p^+ poly-Si gate appears as the bright rectangular feature near the top of the image, and provides an additional direct measure of the fabricated gate length. The n-type channel region immediately under the poly-Si gate exhibits graded SCM contrast (in the vertical direction) from zero near the oxide–Si interface, increasing through the depletion region and leveling off within the n-well. No significant additional features are present in this region, which under these bias conditions would suggest similar dopant concentration in the channel and n-well regions. As the dc bias is decreased [Figs 2(b)–2(d)] the device structure becomes less visible, as the p^+ contact and p^+ poly-Si gate regions are biased near inversion and therefore exhibit essentially zero dC/dV signal. As a result, these features are not distinguishable from the electrical $p-n$ junction and device dielectric layers (dark gray region) in the SCM contrast. For $V_{dc}=-1.5$ V [Fig. 2(d)], additional contrast in the n-type channel region is revealed. The defined channel region between the $p-n$ junctions in Fig. 2(a) is no longer apparent and instead this region now exhibits detailed SCM contrast due to the n^+ superhalo implants. The dark features in the channel region correspond to a lower-magnitude SCM signal, indicating a localized region of increased carrier concentration relative to the n-well,[6,11] as expected for the n^+ superhalo implants. Subsequent polarity-mode[5,7] SCM imaging was performed and the contrast obtained verified the correct carrier type for the localized n^+ regions. The area in the dashed box in Fig. 2(d) is displayed with enhanced contrast in Fig. 2(e). It is clear that the dark SCM feature appears in the shape of two lobes.

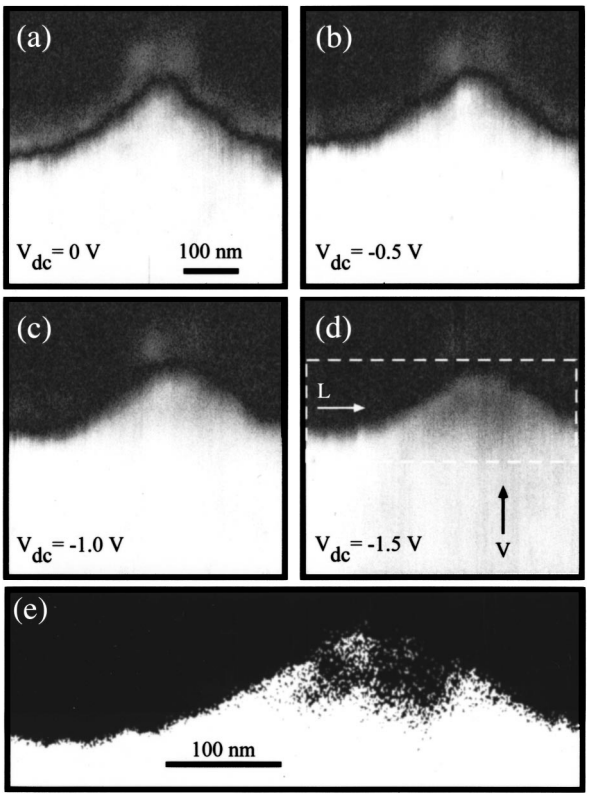

FIG. 2. (a)–(d) Subset of SCM images from the V_{dc} bias-dependent voltage series showing four specific bias voltage conditions required for n^+ superhalo implant imaging. The complete series of images was obtained with V_{ac} held constant at 1 V, while V_{dc} was swept from 2 to -2 V in 0.5 V steps. The gray scale is 5 V. (e) Enhanced contrast of the area in the dashed box in (d), showing the double-lobed superhalo implant features.

Figure 3 shows averaged line scans of the SCM data in Figs. 2(a) and 2(d), in both the vertical [Fig. 3(a)] and lateral [Fig. 3(b)] directions. The line scans presented in Fig. 3(a) were taken for each bias condition at the position indicated by the vertical arrow in Fig. 2(d) (marked "V"). The line scans presented in Fig. 3(b) were taken for each bias condition at the position indicated by the horizontal arrow in Fig. 2(d) (marked "L"). In Fig. 3(a), the n-well device region is on the left side and the device top layers are on the right, while Fig. 3(b) has the same orientation as Figs. 2(a)–2(d). The line scans were taken from raw data and averaged over 10 pixels in the orthogonal direction. The data were then averaged along the line, over 5 pixels (~5 nm) in order to reduce signal noise. In the vertical line scans presented in

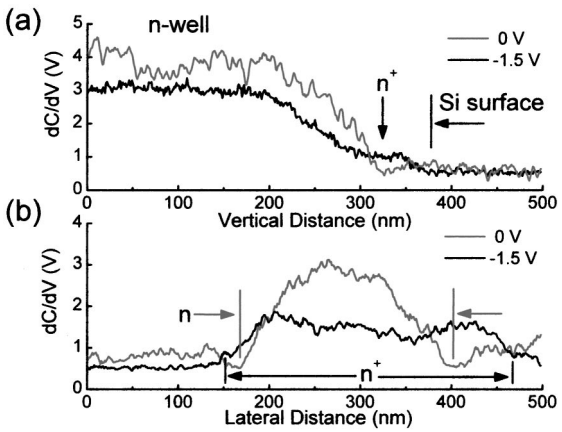

FIG. 3. Averaged line scans taken in the (a) vertical direction, through the drain-side of the channel region, and (b) lateral direction, from the SCM data in Figs. 2(a) ($V_{dc}=0$ V) and 2(d) ($V_{dc}=-1.5$ V). The device positions from which line scans were taken are indicated in Fig. 2(d).

Fig. 3(a), the n^+ superhalo feature appears in the $V_{dc}=-1.5$ V data (black line) as a shoulder, or plateau, prominent in the transition between the lightly doped *n*-well region and p^+ contact and top layer regions, where the SCM contrast approaches zero. No corresponding feature is present in the data for $V_{dc}=0$ V (gray line).

The lateral line scans presented in Fig. 3(b) highlight additional detail in the SCM contrast due to the n^+ superhalo implants. For the $V_{dc}=0$ V data (gray line), the prominent SCM feature (located from ~175 to ~400 nm, indicated by arrows marked ''n'') shows relatively constant doping at this bias condition. The corresponding SCM feature at $V_{dc}=-1.5$ V (black line, indicated by arrows marked ''n^+'') shows increased detail with two shallow depressions in the SCM signal located immediately under the gate region centered at ~250 and ~350 nm (corresponding to the two n^+ superhalo lobes) and a region of larger signal (lower doping) in between. This lateral variation is confirmation that the SCM signal features are not induced by proximity to the gate oxide and poly-Si gate, which are constant across the channel length. Further, in Figs. 2(d) and 2(e) there are bright features above the dark superhalo features, showing that the n^+ regions in the channel are resolved independent of the device features located above. In addition, a significant asymmetry in the two lobes is evident. The source-side lobe exhibits a narrower feature with greater magnitude SCM signal, indicating a more localized implant of lower doping as compared to the drain-side lobe [also demonstrated by the relative size difference between the two lobes in the enhanced contrast image in Fig. 2(e)]. Such asymmetric doping could arise from a lower implant dose on the source side, which upon subsequent thermal processing would result in the observed asymmetric doping.

Electrical characterization of deep-submicron devices currently includes application of the shift-and-ratio method[12] to extract an effective channel length (L_{eff}). L_{eff} describes the quantity of gate-controlled current a short-channel device delivers in reference to the long-channel device, and is not a physical parameter.[13] While accurate for measuring L_{eff} in deep-submicron devices *without* superhalo implants, the shift-and-ratio method yields artificially large values (130%–175%) for devices *with* superhalo implants, presumably due to the decreased effective carrier mobility in the channel region. The SCM technique allows for direct, physical imaging of device structures. We have measured an apparent channel length, L_{app}, as the minimum channel distance between source and drain $p-n$ junctions. Based on detailed analysis of our SCM data for the bias conditions shown in Fig. 2(a), we have measured L_{app} to be 73 ± 11 nm. Analysis of the V_{dc} bias-dependent SCM data indicates that, for this device structure, determination of L_{app} based on SCM imaging is largely independent of bias voltage for $-0.5\text{ V}\leqslant V_{dc}\leqslant 0.5$ V, in contrast to results of previous studies in which simulations of SCM contrast for devices with conventional channel doping showed a substantial dependence of L_{app} on V_{dc}.[11]

In conclusion, we have used cross-sectional SCM to directly image the n^+ superhalo implants, and measure L_{app} in a 120 nm gate length Si *p*-MOSFET with complex 2-D channel doping profile. A series of dc bias-dependent SCM images allows us to delineate the individual device regions. We have demonstrated the specific SCM bias conditions necessary for imaging the n^+ superhalo implants and shown data indicating clear asymmetry in the individual lobes. We estimate L_{app} in this device to be 73 ± 11 nm.

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