With $\omega = 2\frac{\pi}{T_{osc}}$, C_E known and $R_E = \frac{kT_0}{qI_{B0}} + R_s$ known for any given bias, eqn. 6 gives the thermal time constant $\tau_{th} = R_\theta C_\theta = R_{th} \cdot C_{th} = 1.62$ms.

The conditions in eqn. 4, along with $T_A = 0$, can then be used to compute the thermal resistance and capacitance which are found to be $C_{\theta J} = 0.25$mJ/K and $R_{\theta JC} = 6.5$K/W

Conclusion: Autonomous electro-thermal oscillations can arise from fast thermal and electrical dynamic coupling. We have shown that a simple one-pole model for the fast thermal section enables this behaviour to be accounted for, which has been confirmed by experimental evidence. The thermal resistance extracted under high voltage biasing conditions is greater than that reported in the technical data; this confirms the results presented in [3]. Applicability of this resonance measurement to other high voltage power devices (i.e. IGBTs) could be possible and will be investigated.

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Fabrication and characterisation of enhanced barrier AlGaN/GaN HFET

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An AlGaN/GaN HFET incorporating a piezoelectrically enhanced two-layer barrier structure has been fabricated and characterised. The gate leakage current was observed to be suppressed by one order of magnitude, compared to that in a conventional AlGaN/GaN HFET. Breakdown voltages in the piezoelectrically enhanced and conventional HFET structures are ~100V and have positive temperature coefficients.

III-V nitride heterostructure field-effect transistors (HFETs) have emerged as highly attractive candidates for high-voltage, high-power operation at microwave frequencies. The suppression of gate leakage current is of significant importance in improving transistor characteristics [1]. The gate leakage current can be reduced by increasing the gate Schottky barrier height or by increasing the barrier layer thickness. However, in a conventional AlGaN/GaN HFET, increasing the gate Schottky barrier by increasing Al concentration poses limitations on the source and drain contacts; increasing the barrier layer thickness will decrease the gate capacitance and, consequently, transconductance. Previously, we proposed a new approach to enhance the effective Schottky barrier height by utilising a two-layer GaN/AlGaN barrier, within which the piezoelectrically induced polarisation charge acts to increase the barrier height [2]. Using this barrier structure, the gate leakage current is expected to be reduced with no increase in the total barrier layer thickness and consequently little or no change in gate capacitance.

The enhanced barrier HFET structure and a conventional control HFET structure were grown on c-plane (0001) sapphire substrates by low-pressure metal organic vapour phase epitaxy (MOVPE). For the enhanced-barrier HFET, a 225Å nominally undoped $Al_{0.25}Ga_{0.75}N$ layer followed by a 75Å nominally undoped GaN layer were grown on a 3μm highly resistive GaN layer. The conventional HFET control structure consisted of a 300Å nominally undoped $Al_{0.25}Ga_{0.75}N$ barrier layer grown on a 3μm highly resistive GaN layer. In both structures, a two-dimensional electron gas (2-DEG) is formed at the lower AlGaN/GaN interface due to the piezoelectric effect [3] and background doping in the AlGaN layer. In the enhanced-barrier structure, the effective barrier height is increased due to the negative piezoelectric charge at the upper AlGaN/GaN interface. Photocurrent measurements have shown that the effective Schottky barrier heights are 1.89 and 1.52eV for the enhanced-barrier and conventional structures, respectively [2]. Hall mobilities of 620 and 800cm²/Vs were measured at room temperature for the enhanced-barrier and control structures, respectively. Capacitance-voltage measurements yielded sheet carrier concentrations of 4.5×10^{12} and 5.0×10^{12}cm^{-2} for the enhanced-barrier and control structures, respectively.

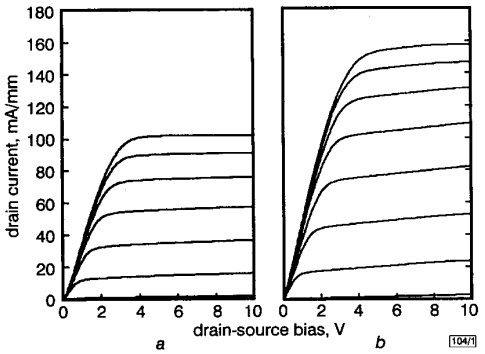

Fig. 1 *Drain current-voltage characteristics of enhanced barrier HFET and conventional HFET*

Devices have 3μm source-drain spacing, 1μm gate length and 50μm gate width; top trace: $V_{GS} = 0.5$V step : –0.5V
a Enhanced-barrier HFET
b Conventional HFET

Transistors with gate length of 1μm, gate widths of 25 and 50μm, source-drain spacing of 3μm, and gate-drain spacing of 1μm were fabricated from both epitaxial layer structures. The source and drain Ohmic contacts were made by evaporating Ti/Al and annealing at 950°C for 30s. The gate Schottky contact was made from Ni/Au. Device isolation was accomplished by ion implantation using phosphorus and helium [4].

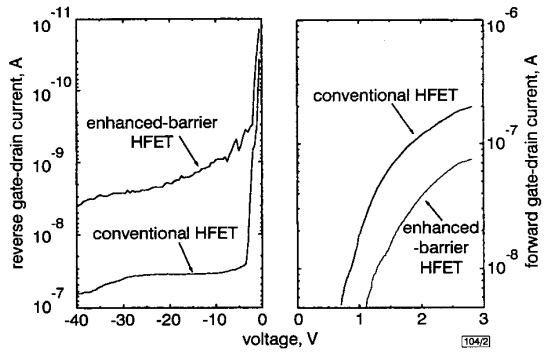

Fig. 2 *Gate-to-drain current-voltage characteristics of enhanced barrier HFET and conventional HFET*

Gate width: 50μm, gate length: 1μm

Fig. 1 shows the drain current-voltage characteristics of HFETs fabricated from each epitaxial structure. The pinch-off voltages are –2.6 and –3.7V for the enhanced-barrier and conventional HFET, respectively. The slightly smaller drain current in the enhanced-barrier HFET is a consequence of the lower mobility and lower carrier concentration in this device. The peak transconductances are 45 and 50mS/mm for the enhanced-barrier and conventional HFET, respectively. Fig. 2 shows the typical gate-drain diode current characteristics. The forward turn-on voltage is

increased in the enhanced-barrier HFET by more than 0.3V. The gate leakage current for the enhanced-barrier HFET is 80pA/μm² at V_{GD} = –40V; under the same conditions the leakage current for the conventional HFET is 1200pA/μm². The significant increase in forward turn-on voltage and suppression of gate leakage current result from the piezoelectrically enhanced effective barrier height in the two-layer barrier structure.

Another possible benefit of the enhanced barrier is an improvement in breakdown voltage that should occur if gate tunnelling is the dominant device breakdown mechanism [5]. The three-terminal breakdown voltages, defined at a current level of 1mA/mm, were measured to be 98 and 100V for the enhanced-barrier HFET and conventional HFET, respectively.

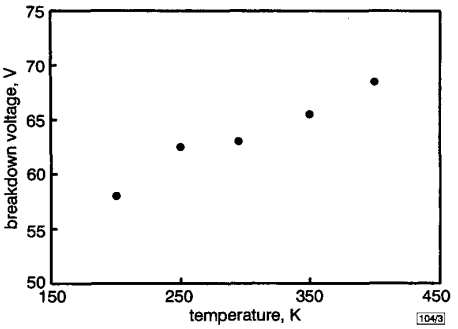

Fig. 3 *Temperature dependence of breakdown voltage for enhanced barrier HFET*

The breakdown mechanism was investigated by measuring breakdown voltage as a function of temperature. A drain current injection measurement [6] was performed with a low injected current of 40μA/mm to avoid permanent degradation of the device so that reliable results can be extracted from repeated measurements. The temperature dependence of the breakdown voltage is shown in Fig. 3 for the enhanced-barrier FIFET. The breakdown voltage is observed to increase with increasing temperature; the same behaviour was observed in the conventional HFET. These results suggest that impact ionisation in the channel, rather than gate tunnelling, is the dominant breakdown mechanism in both structures [7]. This is consistent with the observation of comparable breakdown voltages in the enhanced-barrier and conventional HFET structures. The principal benefit of the barrier-height enhancement is therefore the marked reduction in gate leakage current, with improvements in breakdown voltage more likely to result from engineering of device geometry or channel layer structure and continued improvements in material quality.

In conclusion, we have demonstrated a strong suppression of gate leakage current in AlGaN/GaN HFETs using a two-layer enhanced barrier structure. Breakdown voltages were largely unaffected by the increase in barrier height, and an observed increase in breakdown voltage with increasing temperature suggests that impact ionisation rather than gate tunnelling is the dominant breakdown mechanism in both structures.

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Fabrication technology of polysilicon resistors using novel mixed process for analogue CMOS applications

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A new mixed doping technology, in which arsenic ions were implanted into a phosphorus-doped polysilicon film, has been developed to obtain extremely low temperature coefficient of resistance (TCR) polysilicon resistors. For the same sheet resistance (R_s) value of 75Ω/□, the TCR of the polysilicon resistor fabricated by the proposed process was ~4.3 times lower (112ppm/°C) than that of the conventional phosphorus-doped polysilicon resistor (479ppm/°C).

Introduction: In recently developed analogue/digital CMOS technologies, polysilicon films have been widely used as resistors because of their small voltage independent parasitic capacitance [1]. For the precise and reliable operation of analogue circuits, the temperature coefficient of resistance (TCR) of a polysilicon resistor should be maintained at low values over a wide range of temperatures [2]. The TCR and resistivity properties of polysilicon resistors are extremely sensitive to doping conditions [1], segregation effect [3], and thermal history. Therefore, special manufacturing techniques are required to fabricate polysilicon resistors, which have specifically desired electrical behaviours [3]. In this Letter, a new mixed doping technology is proposed which involves arsenic ion implantation into phosphorus-doped polysilicon resistors to improve the thermal stability of polysilicon resistors.

Process description: 200nm thick polysilicon films were deposited by low-pressure CVD at a temperature of 625°C and doped with $POCl_3$ at different temperatures of 825, 875, and 925°C. In turn, different arsenic ion doses of 9×10^{14}, 4×10^{15}, and 9×10^{15}cm^{-2} at 120keV were implanted into the polysilicon films in order to obtain a polysilicon resistor with an extremely low temperature coefficient.

Results and discussions: Fig. 1*a* shows the TCR and sheet resistance (R_s) variations of polysilicon resistors that were fabricated by the conventional process against $POCl_3$ doping temperatures. With increasing doping temperature, from 825 to 925°C, the TCR increased by ~45%, while the sheet resistance decreased by ~5.9%. In contrast, the arsenic implanted polysilicon resistors show negative TCR properties, as shown in Fig. 1*b*. The TCR property of a polysilicon resistor is determined by the dominant carrier conduction in grains or grain boundaries. Carrier conduction in a polysilicon film is primarily limited by thermionic emission through the energy barrier at the grain boundaries and by phonon scattering inside the grains. Thermionic emission has a negative TCR, while phonon scattering has a positive TCR [1, 4]. From the above results, it is predicted that in the phosphorus-doped sample carrier conduction is dominant in the grains, and in the arsenic-doped sample carrier conduction is dominant in the grain boundaries.