Materials Science and Engineering, R17 (1996) 147–206

R Reports: A Review Journal

Nanoscale characterization of semiconductor materials and devices using scanning probe techniques

Edward T. Yu

Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, USA

Received 14 June 1996; accepted 4 July 1996

Abstract

Scanning probe techniques are applied to a rapidly growing degree in the characterization of advanced semiconductor materials and device structures. In this review, the fundamental principles of scanning tunneling microscopy, atomic force microscopy, and other scanning probe techniques are described. The application of these techniques to the characterization of III–V and Group IV semiconductor epitaxial growth and epitaxial layer structure is discussed, with particular emphasis on the elucidation of epitaxial growth mechanisms, and on the atomic-scale characterization of interface and alloy layer structure in III–V heterostructures by cross-sectional techniques. Nanoscale characterization of buried metal–semiconductor and semiconductor–semiconductor interfaces using ballistic electron emission microscopy is also addressed. Finally, a detailed discussion is included concerning the use of scanning probe techniques for nanometer-scale characterization of ultrasubmicron Si electronic devices — a problem of central importance in ultralarge-scale integrated circuit technology for the coming decade and beyond. Throughout the review, emphasis is placed on the role of scanning probe microscopy in relation to other semiconductor characterization techniques, the influence of various atomic- to nanometer-scale material properties on semiconductor device behavior, and the importance in many instances of theoretical modeling and simulation in the interpretation of results obtained using scanning probe techniques.

Keywords: Scanning probe techniques; Semiconductor materials

1. Introduction

Since its invention in the early 1980s, scanning tunneling microscopy [1–4] (STM) and techniques such as atomic force microscopy [5] (AFM) that have evolved from it have become tools of paramount importance in fundamental studies of surfaces. In addition, an increasing amount of work has been devoted to the use of STM and related techniques — to which we refer collectively as scanning probe microscopy (SPM) — to address problems of technological interest, particularly in the area of semiconductor science and technology. In this paper, we present a description of the physical principles upon which scanning tunneling microscopy, atomic force microscopy, and other scanning probe techniques are based; an overview of the application of these techniques to a variety of technologically important problems, with particular emphasis on the atomic- to nanometer-scale characterization of semiconductor materials and devices; and a discussion of the current and potential future impact of these techniques on both fundamental science and technology development in microelectronics and related fields.

The unique and powerful advantage offered by STM and other scanning probe microscopies is the ability to perform direct studies of structural, electronic, and other properties of materials with extremely high spatial resolution. Many other techniques, such as X-ray diffraction, electron diffraction, and transmission electron microscopy, typically provide only indirect information about sample structure and, while offering the ability to probe certain structural or compositional features at the atomic scale, inevitably average these properties over substantially larger areas or volumes. In scanning

0927-796X/96/$32.00 Published by Elsevier Science S.A.
PII S0927-796X(96)00197-X

tunneling microscopy, however, direct imaging of features corresponding to individual atoms on a surface has been demonstrated for a wide range of materials. Other scanning probe microscopies, while usually providing somewhat lower spatial resolution than STM, allow greater flexibility in samples that can be studied, imaging conditions that can be tolerated, and properties that can be characterized. Rapid progress in the development of new scanning probe techniques and in the commercial availability of SPM instrumentation has led to the widespread application of these techniques to problems of both scientific and technological importance.

All scanning probe microscopies are based on the ability to position, with extremely high precision, various types of probes in very close proximity to the sample under investigation. These probes can detect electrical current flow, atomic and molecular forces, magnetic forces, electrostatic forces, or other types of interactions with the sample; these interactions can be either measured directly or used in an electronic feedback loop to control the separation between the sample and the probe tip. By scanning the probe laterally over the sample surface and performing measurements at different locations, detailed maps of surface structure, electronic properties, magnetic or electrostatic forces, optical characteristics, or other properties can be obtained. The lateral spatial resolution that can be achieved is limited primarily by factors such as the sharpness of the probe tip, the accuracy with which the probe can be positioned over the sample surface, the condition of the surface under investigation, the separation between the sample and the probe tip, and the nature of the force being detected, and can range from a few angstroms or less to tens or hundreds of nanometers.

Fundamental studies of semiconductor surfaces have figured prominently in the development of scanning probe microscopy — particularly STM — and have led to dramatic progress in our understanding of atomic-scale surface phenomena in semiconductors. One of the early triumphs of STM was the successful imaging, with atomic resolution, of the 7×7 reconstruction of the Si (111) surface [6]. Subsequent STM studies of the Si (111) surface provided detailed information about the relationship between STM images and the actual geometric arrangement of atoms for various reconstructions of the surface [7–12]. The ability of STM to provide direct images of electronic states corresponding to individual atoms on the reconstructed surface, as opposed to the indirect information provided by diffraction-based probes of surface structure, helped to resolve a long-standing controversy in surface science. Since then, extensive studies have been performed to elucidate the structural and electronic properties of numerous III–V compound and Group IV elemental semiconductor surfaces. In addition, STM and related techniques have been used to explore adsorption, bonding, and removal of atoms and molecules on semiconductor surfaces during processes such as epitaxial crystal growth, etching, and deliberate modification of surfaces via tip–sample interactions. Much of this work has also provided insights into the fundamental physics of the tunneling process.

The extremely high spatial resolution afforded by scanning probe techniques has led naturally to their application to a wide range of technological problems in semiconductor device physics. In addition to the work described above, scanning tunneling microscopy, particularly in the cross-sectional geometry, is proving to be a powerful tool in the study of atomic-scale properties of III–V semiconductor heterostructures and of nanometer-scale structure in Si microelectronic devices. Furthermore, a variety of scanning probe techniques have been applied to perform detailed characterization of structural, electronic, magnetic, optical, and other properties of materials and devices with nanometer-scale spatial resolution. The growing importance of scanning probe microscopy in semiconductor science and technology is a natural consequence of the desire to design and fabricate ever smaller structures to improve device performance or achieve new device functionality, and of the inadequacy of more traditional experimental techniques for detailed characterization at the nanometer to atomic scale.

The remainder of this paper is divided into six parts. Given the extensive (and rapidly growing) literature that now exists in this area, we have not attempted to be completely exhaustive in our review.

Specifically, we have emphasized the application of scanning probe techniques to the characterization of semiconductor materials and device structures, and therefore have not included a discussion of the rapidly growing field of scanning probe lithography [13]. Instead, we present in this article an overview of the various scanning probe techniques and discuss, in detail, several applications of particular importance in semiconductor technology. In Section 2, we provide an introduction to the basic principles upon which STM, AFM, and other scanning probe microscopies are based. Sections 3 and 4 describe the application of SPM techniques to a wide range of issues in semiconductor technology, involving both III–V compound semiconductors and Si-based materials. Section 5 discusses nanometer-scale characterization of buried metal–semiconductor and semiconductor heterojunction interfaces, and Section 6 describes the application of SPM to the characterization of ultrasubmicron Si electronic device structures. Conclusions and a discussion of some future prospects in this field are given in Section 7.

2. Basic principles of scanning probe microscopy

We begin with an overview of the instrumentation and essential physical principles upon which STM and other scanning probe techniques are based. Detailed discussions of these principles, the instrumentation required, and a variety of applications have been given in a number of review articles [14–17], edited collections [18–23], and books [24,25]. Several reviews [22,23,26,27] and books [25,28] have also been published on atomic force microscopy and other scanning probe techniques.

2.1. Scanning tunneling microscopy

2.1.1. Tunneling of electrons

In scanning tunneling microscopy, a sharp metal probe tip is scanned over the surface of a conducting or semiconducting sample, typically with a separation between the tip and sample that is in the order of several angstroms. When a bias voltage is applied between the sample and the tip, electrons tunnel through the potential energy barrier separating the sample and tip, producing an electrical tunneling current. The magnitude of this current depends primarily on three factors: the probability that an electron will tunnel through the potential energy barrier between the sample and tip, which varies exponentially with the tip–sample separation; the electronic density of states in the sample; and the electronic density of states in the tip. Because of the extreme sensitivity of the tunneling current to the tip–sample separation, an electronic feedback loop that continually adjusts the tip–sample separation is generally used to maintain a constant tunneling current. Measurement of the tip height required to maintain a constant tunneling current while scanning over the sample surface will yield a profile of the local electronic density of states on the sample surface.

The dependence of the electron tunneling probability on tip–sample separation can be understood using a simple one-dimensional model of a metal–vacuum–metal tunneling junction, shown schematically in Fig. 1. The wave function $\psi(z)$ of the electron must satisfy Schrödinger's equation

$$-\frac{\hbar^2}{2m}\frac{d^2}{dz^2}\psi(z)+U(z)\psi(z)=E\psi(z) \tag{1}$$

where m is the mass of the electron, $U(z)$ is the potential function, and E is the energy of the electron. For an electron at energy E, the wave function for $z<0$ will be of the form $\Psi(z)=\psi(0)e^{\pm ikz}$, where $k=\sqrt{2m(E-U)}/\hbar$. In the barrier region, $E<U(z)$ and the electron wave function will be of the form $\psi(z)=\psi(0)e^{\pm\kappa z}$, where $\kappa=\sqrt{2m(U-E)}/\hbar=0.512\sqrt{\phi(\text{eV})}$ Å^{-1}. For typical metals used to fabricate STM tips, the work function ϕ is roughly 4–6 eV, corresponding to $\kappa\approx 1.0$–1.25 Å^{-1} for electrons at energies close to the Fermi level. The wave function of an electron located in one of the metal layers

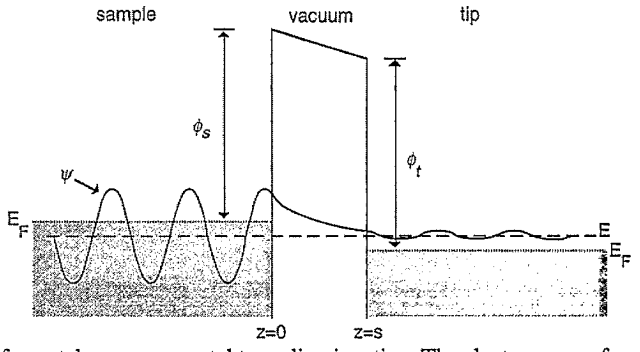

Fig. 1. Schematic diagram of a metal–vacuum–metal tunneling junction. The electron wave function decays exponentially in the vacuum barrier region, leading to a non-zero probability for electrons to tunnel across the barrier between the tip and the sample in a scanning tunneling microscope.

will therefore increase or decay exponentially in the vacuum barrier, leading to the possibility of quantum-mechanical tunneling through the classically forbidden barrier region.

The probability that an electron at energy E will tunnel from the sample through a vacuum barrier of thickness s and into the tip is given by the transmission coefficient, $T(E,V)$, where V is the bias voltage applied between sample and tip. Since the probability density of the electron is given by $|\psi(z)|^2$, it can be seen from the functional form of the wave function in the vacuum barrier that the transmission coefficient will decrease exponentially with increasing barrier thickness s:

$$T(E,V) \propto e^{-2\kappa s} \tag{2}$$

For the typical values of κ given above, the transmission coefficient, and therefore the tunneling current, will decrease by an order of magnitude for an increase in the barrier thickness of approximately 1 Å.

This exquisite sensitivity of the tunneling probability to the tip–sample separation is largely responsible for the extremely high spatial resolution attainable in STM. At the atomic level, the apex of the metal probe tip will consist of a single atom or a small cluster of atoms. Because the tunneling probability decreases exponentially with increasing tip–sample separation, the bulk of the tunneling current will be highly localized, flowing through the single atom or cluster of atoms at the apex. The tunneling current can therefore provide a highly localized probe of the electronic structure of the sample surface.

The tunneling current $I(V)$ can be calculated using a variety of theoretical methods, two of which we describe here. In one approach, developed by Tersoff and Hamann [29,30], the tunneling current is calculated from the transition rate between tip and sample states obtained using time-dependent perturbation theory. The total current arising from electrons tunneling both into and out of the sample is then given by

$$I(V) = \frac{2\pi e}{\hbar} \sum_{\mu,\nu} [f_t(E_\mu) - f_s(E_\nu + eV)] \, |M_{\mu\nu}|^2 \delta(E_\mu - E_\nu) \tag{3}$$

where f_s and f_t are the Fermi distribution functions in the sample and tip, respectively, $M_{\mu\nu}$ is the quantum-mechanical tunneling matrix element between the tip state ψ_μ and the sample state ψ_ν, E_μ and E_ν are the energies of the states ψ_μ and ψ_ν, respectively, and $\delta(E_\mu - E_\nu)$ is the Dirac delta function. The sum is taken over all unperturbed tip and sample states. If the spectrum of states in the sample and that in the tip are continuous rather than discrete, the sum in Eq. (3) can be converted to an integral over energy

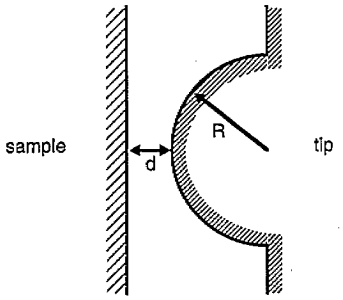

Fig. 2. Tip–sample geometry in the model of Bono and Good [33]. The tip is modeled as a hemisphere of radius R and effective area $A = \pi R^2$. Use of a free-electron model for the metal probe tip and an effective mass model for a semiconducting sample allows detailed current–voltage spectra to be calculated.

$$I(V) = \frac{4\pi e}{\hbar} \int \rho_t(E)\rho_s(E+eV)[f_t(E) - f_s(E+eV)]\,|M_{\mu\nu}|^2 dE \tag{4}$$

where ρ_t and ρ_s are the electronic densities of states in the tip and sample, respectively. From Eq. (4) we see explicitly the dependence of the tunneling current on the densities of states in the tip and sample and on the tunneling matrix element. The tunneling matrix element $M_{\mu\nu}$ was shown by Bardeen [31] to be given by

$$M_{\mu\nu} = \frac{\hbar^2}{2m} \int dS \cdot (\psi_\mu^* \nabla \psi_\nu - \psi_\nu \nabla \psi_\mu^*) \tag{5}$$

where the integral is computed over a surface contained entirely within the vacuum barrier region.

In another theoretical model, developed by Bono and Good [32,33], the metal tip is modeled as a hemisphere of radius R projecting from a plane parallel to the sample surface, as shown in Fig. 2. The probe tip is modeled as a free-electron metal, and the sample, in the case of a semiconductor, is assumed to be well described by an effective-mass model. The tunneling current for a voltage V applied to the tip is then given by [33]

$$I(V) = \frac{eA}{2\pi^2 h} \int dE[f_s(E) - f_t(E+eV)] \int d^2k_\parallel T(E_\perp) \tag{6}$$

where $A = \pi R^2$ is the effective cross-sectional area of the tip, f_s and f_t are the Fermi distribution functions in the sample and tip, respectively, $\vec{k}_\parallel$ is the wave vector parallel to the sample surface, $E_\perp$ is the energy corresponding to the wave vector component normal to the sample surface, and $T(E_\perp)$ is the transmission coefficient. The integral is computed over all energies for which the electronic densities of states in the sample and tip are both non-zero. This approach has been used to develop semiquantitative simulations of current–voltage spectra for scanning tunneling spectroscopy performed on semiconductor surfaces [34].

Theoretical models of the tunneling current, such as those described above, provide the basis for developing a detailed, quantitative understanding of the tunneling process. A comprehensive theoretical understanding of tunneling processes in STM and detailed simulations of tunneling currents for a variety of sample structures will be essential for the most effective application of STM to the characterization of semiconductor materials and devices, particularly for heterostructure materials and advanced device structures in which the composition and electronic structure of the surface under investigation are spatially inhomogeneous and highly complex.

2.1.2. Imaging and spectroscopy

The most common mode of STM operation is constant-current imaging, in which the tunneling tip is rastered across the sample surface and, at each point, the tip–sample separation is adjusted to yield a constant tunneling current. Because the tunneling current depends on both the tip–sample separation and the local electronic densities of states of the tip and the sample, a constant-current topographic image will yield information about the electronic densities of states. The density of states of the tip may often be assumed to be relatively featureless compared with that of the sample in the energy range of interest, allowing constant-current images to be interpreted as profiles of the local electronic density of states of the sample. Details of the probe tip shape and its cleanliness, however, can affect the appearance of such images, which must therefore be interpreted with appropriate caution.

Spectroscopic studies, in which the dependence of the tunneling current on tip–sample voltage, tip–sample separation, or other parameters is measured, can be used to probe the electronic properties of the tip–sample system with spatial resolution at or near the atomic scale. Detailed reviews of scanning tunneling spectroscopy can be found in Refs. [35–37]. In this review we concentrate primarily on the aspects of spectroscopy of greatest relevance to studies of semiconductor electronic structure. It should be noted that spectroscopic measurements, to an even greater degree than constant-current imaging, are particularly sensitive to probe tip structure and cleanliness [37]. For example, relatively blunt tips, while not necessarily producing the highest spatial resolution in imaging, have been found to yield very consistent and reproducible spectroscopic results [38].

The simplest extension of the constant-current imaging measurement described above is voltage-dependent imaging, in which constant-current images are obtained at different tip–sample bias voltages. Because of the dependence of the tunneling current on the tip and sample densities of states, the tunneling current at different bias voltages will be dependent on the densities of states integrated over different ranges of energies. Contrast in the corresponding constant-current images will reflect these variations in electronic structure. In particular, positive bias applied to the sample will yield images of unoccupied electronic states on the sample surface, while negative sample bias will yield filled-state images. Some early examples of this approach include atom-selective imaging of the GaAs (110) surface [39] and studies of surface chemical bonding on clean and NH_3-dosed Si (001) surfaces [40]. Fig. 3 shows images from Ref. [39] of the GaAs (110) surface obtained at positive and negative sample bias voltages. At positive sample bias, the unoccupied states corresponding to the Ga orbitals are imaged, while at negative sample bias the filled states corresponding to the As orbitals are visible.

More detailed information about the electronic density of states can be obtained using techniques such as constant-separation spectroscopy, in which the feedback loop that maintains a constant tunneling current is momentarily disconnected and the tunneling current is measured as a function of tip–sample bias voltage [8–10]. Selloni et al. [41] and Lang [42] have suggested that, for non-zero bias voltages applied between the sample and tip, the tunneling current should be given approximately by an expression of the form

$$I(V) \propto \int_0^{eV} \rho_s(E)\rho_t(E-eV)T(E,V)dE \tag{7}$$

If the electronic density of states in the tip is assumed to be constant, the conductivity is then given by

$$\frac{dI}{dV} \propto \rho_s(eV)\rho_t(0)T(eV,V) + \int_0^{V} \rho_s(E)\rho_t(E-eV)\frac{dT(E,V)}{dV}dE \tag{8}$$

The transmission coefficient in Eq. (7) and Eq. (8) depends very strongly on the tip–sample separation and the tip–sample bias voltage; these dependences can obscure features in the current–voltage spectrum $I(V)$ and the conductivity dI/dV arising from variations in the electronic density of states. Because

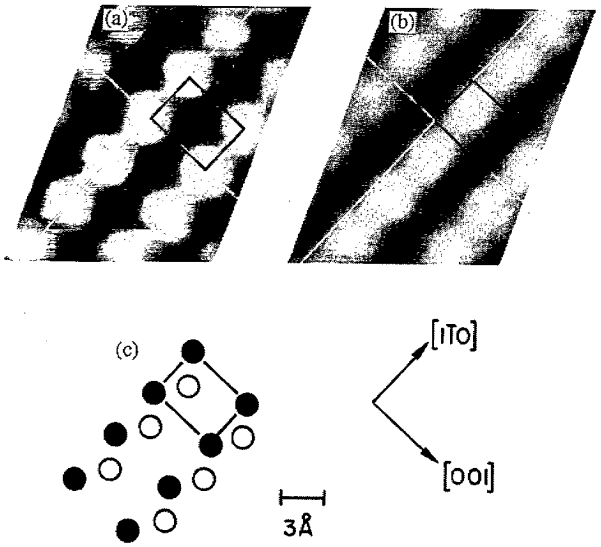

Fig. 3. Constant-current STM images of the GaAs (110) surface obtained at (a) positive sample bias voltage and (b) negative sample bias. (c) Arrangement of atomic orbitals on the (110) surface; solid and open circles represent Ga and As orbitals, respectively. At positive sample bias, the empty Ga orbitals are imaged, while at negative sample bias the filled As orbitals are visible [39].

the sample electronic density of states, $\rho_s(E)$, is most often the quantity of greatest interest, a procedure for extracting $\rho_s(E)$ from $I(V)$ and dI/dV is highly desirable.

It has been shown [10,38] that a good approximation to the surface electronic density of states can be obtained from the normalized conductivity, $(dI/dV)/(I/V)$. From Eq. (7) and Eq. (8) we can obtain an expression for the normalized conductivity:

$$\frac{dI/dV}{I/V} \propto \frac{\rho_s(eV)\rho_t(0) + \int_0^{eV} \frac{\rho_s(E)\rho_t(E-eV)}{eT(eV,V)} \frac{dT(E,V)}{dV} dE}{\frac{1}{eV}\int_0^{eV} \rho_s(E)\rho_t(E-eV)\frac{T(E,V)}{T(eV,V)} dE} \tag{9}$$

Because the transmission coefficient appears in both the numerator and the denominator of both integrands, the dependence of the normalized conductivity on separation and voltage is much weaker than that of the current $I(V)$ or the conductivity dI/dV, and the normalized conductivity can be written in the form [35]

$$\frac{dI/dV}{I/V} = \frac{\rho_s(eV)\rho_t(0) + A(V)}{B(V)} \tag{10}$$

where $A(V)$ and $B(V)$ are slowly varying functions of V. Experimental studies have confirmed that the normalized conductivity has a much weaker dependence on tip–sample separation and applied voltage than does the conductivity dI/dV, and can provide a good approximation to the local electronic density of states [10,38].

For studies of semiconductors, in which the presence of a non-zero band gap can lead to tunneling currents and conductivities ranging over several orders of magnitude, an issue of particular importance is dynamic range in the measurement of tunneling current. Wide dynamic range is especially important if features in the electronic density of states near or within the energy band gap are of interest. This

issue has been addressed most effectively by the development and application of variable separation spectroscopic techniques, in which the tunneling current is measured while both the tip–sample bias voltage V and the tip–sample separation s are varied in a controlled manner [10,38,43]. For example, a series of constant-separation current–voltage spectra can be measured at several different separations, or the separation may be varied continuously as the voltage is ramped. The variation in tip–sample separation is then accounted for by multiplication of the current by a correction factor $e^{2\kappa\Delta s}$, where κ is the tunneling decay constant and Δs is the relative separation at which the tunneling current was measured. Using this technique it is possible to measure values of the tunneling current over a limited dynamic range and, via the transformation described above, obtain the equivalent constant-separation current–voltage spectrum over a much larger range of current magnitude. A detailed discussion of variable separation tunneling spectroscopy is presented in Ref. [37].

An example of the utility of this technique is in spectroscopy performed on unpinned surfaces of heavily doped semiconductors, an application of particular relevance to the characterization of electronic device structures by STM. Unpinned surfaces, or at least surfaces that are not strongly pinned, are important for such applications because it is the electronic properties of the bulk material, rather than those arising purely from surface effects, that are of primary interest. For such surfaces, three components have been found to contribute to the tunneling current: tunneling of electrons from the tip into empty conduction-band states at large positive sample bias voltages; tunneling of electrons from filled valence-band states into empty tip states at large negative voltages; and tunneling involving dopant-induced carriers (electrons in the conduction band for n-type material or holes in the valence band for p-type) at voltages for which the Fermi level in the tip is at an energy aligned within the band gap of the sample [34]. Fig. 4 shows current–voltage characteristics for tunneling on unpinned p-type and n-type Si surfaces calculated using the expression given in Eq. (7) for the tunneling current. The three components contributing to the tunneling current can be seen clearly in each case. Experimentally, it has been found that tunneling involving dopant-induced carriers can generally be measured only for unpinned surfaces of very heavily doped material, and that observation of the dopant-induced current is a good indication that a surface is electronically unpinned. However, the dopant-induced tunneling current is much smaller in magnitude than the conduction- and valence-band components, particularly for material with a substantial energy band gap; resolving this component in spectroscopic measurements therefore requires that the tunneling current be measured over a large dynamic range.

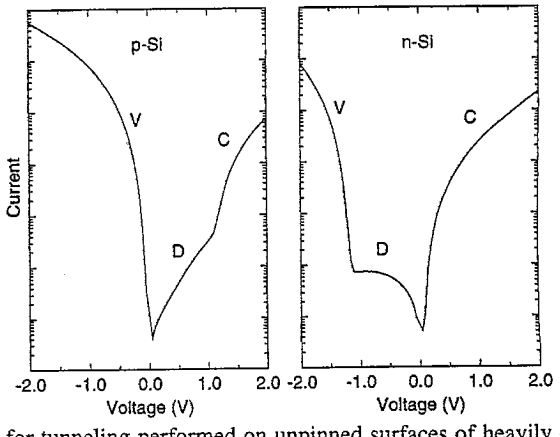

Fig. 4. Current–voltage spectra for tunneling performed on unpinned surfaces of heavily doped (1×10^{-19} cm^{-3}) p-type and n-type Si, calculated using Eq. (7). The conduction-band, valence-band, and dopant-induced components of the tunneling current, labeled C, V, and D respectively, can be seen in each case.

Feenstra [44] has performed detailed scanning tunneling spectroscopy measurements on cleaved (110) surfaces of several III–V semiconductors. III–V semiconductors are particularly well suited for such studies, as they cleave easily to yield atomically flat, and in most cases electronically unpinned, (110) surfaces ideally suited for tunneling measurements. Detailed tunneling current spectra were obtained for GaAs, InP, GaSb, InAs and InSb using variable-separation spectroscopy. In these spectra, the conduction-band and valence-band edges, L-point band edges, and features associated with surface states could be distinguished; the energies of these features were determined to within ± 0.03 eV, with shifts in energies arising from tip-induced band bending estimated to be less than 0.1 eV for dopant concentrations higher than $\sim 1 \times 10^{18}$ cm^{-3}. For samples in which the dopant concentration is substantially lower, tip-induced band bending can shift the apparent energies of the band edges by as much as several tenths of an electron volt, making accurate, quantitative interpretation of features observed in current–voltage spectra extremely difficult.

Spatially resolved spectroscopic measurements can be used to construct images that reveal atomic- to nanometer-scale variations in electronic structure on the sample surface. In one such technique, referred to as current imaging tunneling spectroscopy (CITS), a constant-current topographic scan with the current stabilized at a fixed value I_0 for a specific voltage V_0 is performed over the sample surface and, at each point, a current–voltage spectrum is measured. Variations in electronic structure across the sample surface will produce corresponding variations in the current–voltage spectra; these spatial variations can then be revealed by plotting the current measured at specific bias voltages other than V_0 – so-called 'current images'. Hamers et al. [9] first used this technique to study atomic-scale variations in the electronic structure of the 7×7 reconstruction of the Si (111) surface.

Current images cannot, however, necessarily be interpreted as direct images of particular features in the local electronic density of states. Because the tip–sample separation at each point is determined by the constant-current condition at a single bias voltage V_0, topographic and electronic information may be difficult to distinguish from each other in a CITS measurement. Contrast in current images can in fact be caused both by localized variations in electronic structure and by changes in the background of the spectrum that can arise from, for example, the dependence of the tunneling probability on separation. Hamers et al. [9] have argued that, for CITS performed with a constant-current bias voltage V_0 that produces a topographic image reflecting primarily the actual physical topography of the sample surface, constrast in current images will reflect primarily differences in electronic structure. Satisfying this condition, however, requires a detailed prior knowledge of the physical topography of the surface. Indeed, studies of the Si (111) 2×1 surface by Stroscio et al. [45,46] showed explicitly that contrast in current images can arise from topographically induced changes in the tunneling probability as well as variations in the electronic density of states; however, it was also noted that these effects could be reduced by generating images of the normalized conductivity $(\mathrm{d}I/\mathrm{d}V)/(I/V)$ rather than simply the tunneling current I.

From this discussion it should be apparent that imaging and tunneling spectroscopy are extremely powerful tools for probing the structure and electronic properties of conducting or semiconducting samples, but also that considerable care is required in performing and interpreting such measurements. Continued advances, particularly in the application of tunneling spectroscopy to advanced semiconductor materials and device structures, are likely to require further improvements in sample and probe tip preparation, continued development and implementation of advanced techniques such as variable-separation spectroscopy, and, perhaps most important, the development of a more complete understanding of the relationship between the measured tunneling current and the detailed electronic structure of the sample and tip. This is particularly true for complex, highly inhomogeneous sample structures that are likely to be encountered in technological applications.

2.1.3. *Instrumentation*

Because of the exquisite sensitivity of the tunneling current in a scanning tunneling microscope to the tip–sample separation, compactness and structural rigidity of the microscope combined with a suspension system for isolating the microscope from ambient vibrations are essential [16,47–50]. In addition to mechanisms for isolation from external vibrations, a scanning tunneling microscope comprises several basic elements, as shown schematically in Fig. 5. These include a mechanism for bringing the tip and sample into extremely close proximity, and for maintaining, with a very high degree of stability, an extremely small separation between sample and tip; electronics for positioning and scanning the tip over the sample surface, applying voltage between the sample and tip, measuring the tunneling current, and regulating the current by adjusting the tip–sample separation; and a computer for instrument control, data acquisition and display of images.

Precise positioning and raster scanning of the tip relative to the sample is accomplished using piezoelectric materials, which deform under the application of an electric field. Lead zirconate titanate (PZT) ceramics, which in appropriate geometries can yield piezoelectric responses ranging from ~ 10 Å/V to over 100 Å/V, are widely used in the construction of STM scanners. Two basic scanner designs dominate: the tripod scanner, used in the initial demonstration of scanning tunneling microscopy, and the tube scanner [51]. The tripod scanner, shown schematically in Fig. 6(a), consists of three orthogonal piezoelectric bars. Motion in three dimensions is achieved by application of independent voltages V_x, V_y, and V_z, to the piezoelectric elements. The tube scanner, shown schematically in Fig. 6(b), consists of a piezoelectric tube, metallized completely on the inner surface and in four quadrants on the outer surface. Tip motion is achieved by application of voltages $+V_x$ and $-V_x$ to opposing quadrants in the x direction, or $+V_y$ and $-V_y$ in the y direction, causing the tube to bend.

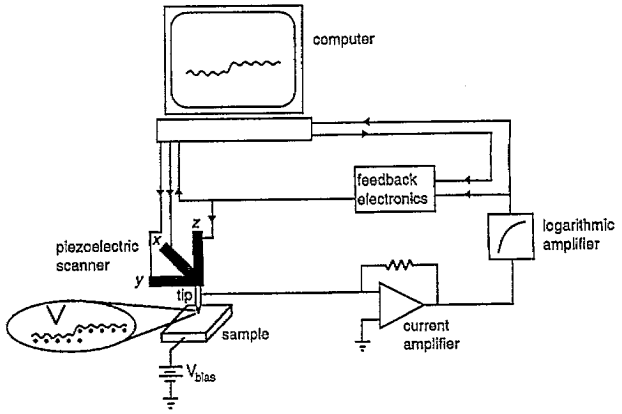

Fig. 5. Basic elements of a scanning tunneling microscope, including a piezoelectric scanner for fine-scale positioning of the tip relative to the sample, electronic components, and computer control. Not shown are mechanisms for coarse, long-range positioning of the sample and tip and for vibration isolation.

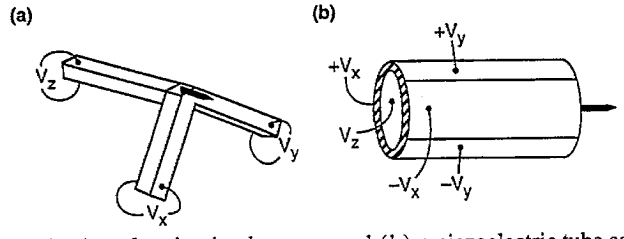

Fig. 6. Schematic diagram of (a) a piezoelectric tripod scanner and (b) a piezoelectric tube scanner. Piezoelectric scanners are used to position the probe tip in a scanning probe microscope over the sample surface with extremely high spatial resolution.

Application of a voltage V_z to the inner surface produces motion in the z direction. The relative simplicity of the tube scanner, its higher resonant vibration frequencies, and its reduced susceptibility to thermal drift compared with the tripod scanner, have led the tube scanner to eclipse the tripod design in popularity.

In addition to fine-scale positioning of the tip by the scanner, a mechanism for moving the tip and sample over distances ranging from ~ 1000 Å to several millimeters — so-called coarse positioning — is required to bring the tip and sample to within the range of motion of the scanner, and for positioning the tip over a specific area of the sample. Several designs have been implemented for coarse positioning in scanning tunneling microscopes. The piezoelectric stepper [1], or 'louse', consists of a piezoelectric plate supported by three metal feet that can be clamped in place by electrostatic, mechanical, or magnetic forces. Motion in single steps ranging in size from ~ 100 Å to ~ 1 μm is achieved by deforming the piezoelectric plate with a single foot unclamped, then clamping the feet with the plate in a new position. Coarse motion can also be achieved using a simple screw mechanism for gross positioning, and a fine-pitch screw combined with a lever, springs of different stiffness, or other mechanisms to demagnify the motion of the screw for the final approach of the tip and sample to within the range of motion of the scanner [52,53]. In a third design, the inertial stepper [54,55], a sliding block carrying the sample or tip rests on a piezoelectric element to which voltage is applied. When the voltage is changed sufficiently slowly, the block moves along with the piezoelectric element; if the voltage changes rapidly, however, the block will remain in place because of inertia. Motion can therefore be achieved by applying a sawtooth voltage, with the step size determined by the voltage amplitude. By adjusting the sawtooth voltage amplitude and frequency, both controlled motion with individual step sizes on the order of hundreds of angstroms, or more rapid motion over millimeter-scale distances, can be achieved. There are also coarse motion mechanisms based on the Inchworm [56], a device in which an alumina shaft surrounded by a three-section PZT sleeve is moved by successive clamping or unclamping of the shaft by the end sections of the sleeve and deformation of the center section.

Finally, a key component in the tunneling measurement is the probe tip itself. The structure and cleanliness of STM tips exert a profound influence on the quality and reproducibility of tunneling measurements. Tungsten, platinum–iridium, and gold are among the materials commonly used for fabrication of tips. Ideally, an STM tip should have a sturdy 'shank' to minimize vibrations, and a high aspect ratio and small radius of curvature at the apex to facilitate high-resolution imaging. A wide variety of methods have been used to fabricate STM tips, with simple mechanical cutting or electrochemical etching being especially common [57–59]. In addition to the basic tip fabrication procedure, a variety of treatments may be used to clean, sharpen, and characterize the tip either prior to or during tunneling. Tip annealing to remove contaminants and oxides, sharpening and characterization by field emission, tunneling at high bias voltages, and controlled crashing of the tip into the sample are among procedures that have been used to improve tip quality, and consequently imaging or spectroscopic measurements, in STM.

2.1.4. Sample geometries

Atomic-scale spatial resolution and sensitivity to electronic properties make STM a natural technique to apply to the characterization of novel semiconductor materials and device structures. Atomic- and nanometer-scale properties of alloy layers and heterojunction interfaces can profoundly influence the properties of heterostructure devices, particularly so-called 'nanostructures' in which device dimensions approach tens of nanometers or less. An understanding of and, eventually, control over material properties and device structure at or near the atomic scale will be required for realization and optimization of a wide range of heterostructure and nanoscale devices. More immediately, there

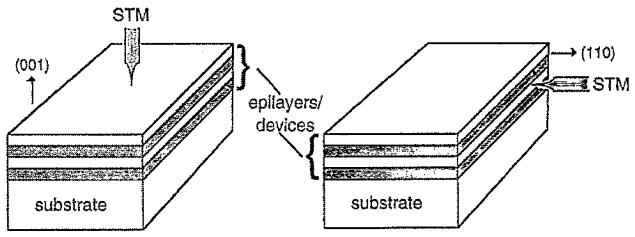

Fig. 7. (a) Planar and (b) cross-sectional sample geometries for scanning tunneling microscopy studies of semiconductor epitaxial layers and device structures.

is increasing recognition that nanometer-scale characterization of and control over fabrication processes and the resulting device structures have become essential for continued scaling of Si electronics to extreme ultrasubmicron dimensions. For example, nanometer-scale characterization of and control over source and drain junction profiles (both lateral and vertical), dopant fluctuations, and oxide thickness and uniformity are among the issues that are of critical importance for scaling of Si metal–oxide–semiconductor technology over the next decade [60]. Because many of the traditional experimental techniques applied to these problems are inadequate for effective characterization of extreme ultrasubmicron devices, new methods such as scanning probe microscopies must be exploited.

Two experimental geometries, shown schematically in Fig. 7, are of particular interest [61]: the 'planar' geometry, in which the surface — typically (001) or (111) — on which growth or processing occurs is studied directly, and the cross-sectional geometry, in which (001) wafers are cleaved to expose a cross-section, generally a (110) or $(1\bar{1}0)$ plane, of epitaxial layers or device structures fabricated on the wafer. The former geometry allows surface characteristics during various stages of crystal growth or processing to be studied, while the latter has developed into a powerful tool for detailed investigation of epitaxially grown layers and actual device structures.

For experiments conducted in the planar geometry, a major concern is the integrity of the surface during transfer from growth or processing chambers to the microscope system. In particular, oxidation during exposure of a semiconductor surface to atmosphere can be a severe impediment to performing high-resolution STM imaging and spectroscopy. A variety of techniques, including direct connection, under ultrahigh-vacuum conditions, of growth (e.g., molecular-beam epitaxy) chambers to an analytical chamber containing an STM, portable ultrahigh-vacuum transfer modules, and capping layers grown on a semiconductor surface and subsequently removed in the analytical chamber after transfer through air, have been employed to address this issue.

In the cross-sectional geometry, semiconductor wafers are cleaved to expose a cross-section of epitaxial layers grown or device structures fabricated on the wafer. Scanning tunneling microscopy experiments performed on the cross-sectional surface can then reveal information about the atomic-scale morphology and electronic structure of these epitaxial layers and devices. Two factors are of critical importance in such experiments: the production of a cross-sectional surface that is atomically flat and as free as possible of surface states or defects that can act to pin the Fermi level at the surface; and the ability to position the tunneling tip reliably and reproducibly over specific regions of interest.

A cross-sectional surface with the requisite structural quality can at present be obtained only by cleaving. III–V compound semiconductors cleave easily to yield a (110) surface that is atomically flat, with monolayer steps typically spaced tens to hundreds of nanometers apart. Furthermore, the cleaved (110) surface is, for most III–V materials, electronically unpinned; spectroscopic measurements therefore reflect the electronic properties of the bulk material, rather than being dominated by surface states. For Si and Si-based structures cleaving is more difficult, although flat (110) surfaces

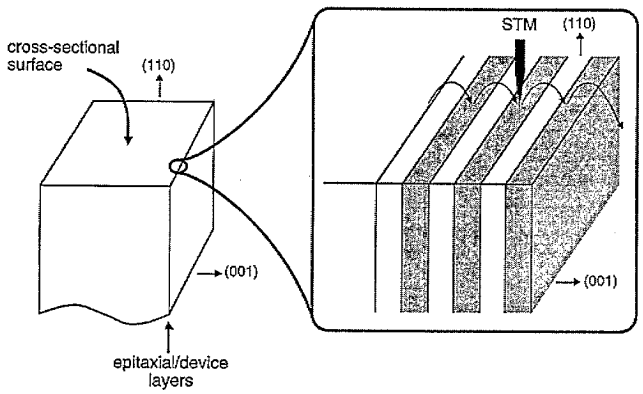

Fig. 8. Procedure for locating epitaxial or device layers in cross-sectional scanning tunneling microscopy. The initial tunneling approach is made over the substrate region, which is easily visible in an optical microscope. The tip is then gradually stepped towards the edge, the location of which is signaled by a failure to detect any tunneling current when the tip is advanced.

can be obtained. Hydrogen passivation can be accomplished by dipping the cleaved wafer in HF or by exposure of a clean, cleaved (110) surface to atomic hydrogen *in vacuo*, and is required to obtain a (110) surface that is not strongly pinned.

Positioning of the STM tip over the region of interest can be a non-trivial matter, as one is often interested in locating structures extending across ~ 1 μm or less on a cross-sectional surface that is a substantial fraction of a millimeter in width. One approach that has been used to locate epitaxial layers in such studies is to mount the STM in an ultrahigh-vacuum scanning electron microscope (SEM) [62,63]. By imaging the sample and tip using the SEM, it is possible to position the tip in the vicinity of epitaxially grown layers rapidly and reliably. An alternative method utilized by a number of researchers is shown in Fig. 8. The tip is positioned as close as possible to the sample edge, and gradually moved towards the edge using the coarse positioning mechanism. When the tip has crossed over the sample edge, tunneling current can no longer be detected. The sample edge can then be used as a reference to locate the region of interest on the cross-sectional surface.

2.1.5. *Ballistic electron emission microscopy*

In addition to performing characterization of either planar or cross-sectional surfaces, it is often desirable to probe nanoscale properties of buried layers or interfaces. Nanometer-scale characterization of buried interfaces, e.g. semiconductor heterojunctions or metal–semiconductor interfaces, can be performed using ballistic electron emission microscopy (BEEM) [64,65]. An extensive review of BEEM is given in Ref. [66]. In this technique, illustrated schematically in Fig. 9, a bias voltage V_{bias} is applied between the STM probe tip and the base layer at the top of the sample, and the STM probe tip is used to inject carriers toward the interface. As in conventional scanning tunneling microscopy, the tip–sample separation may be controlled by a feedback circuit that maintains a constant value for the tunneling current I_t. If the base layer is sufficiently thin, a substantial fraction of the injected carriers will be transported ballistically across the base layer. Fig. 10(a) and (b) show schematic energy-band diagrams for an n-type Schottky barrier system in which the metal acts as the base layer and the n-type semiconductor as the collector. Fig. 10(c) shows the collector current I_c schematically as a function of the bias voltage. For $V_{\text{bias}} = 0$, both the tunneling current and the collector current are zero. For $0 < V_{\text{bias}} < V_b$, the tunneling current is non-zero but, because the energies of the injected carriers are lower than the barrier height, the tunneling current flows primarily through the base contact and the collector current is negligibly small. For $V_{\text{bias}} > V_b$, some of the injected electrons are transported ballistically across the interface, producing a current I_c at the collector contact. With appropriate

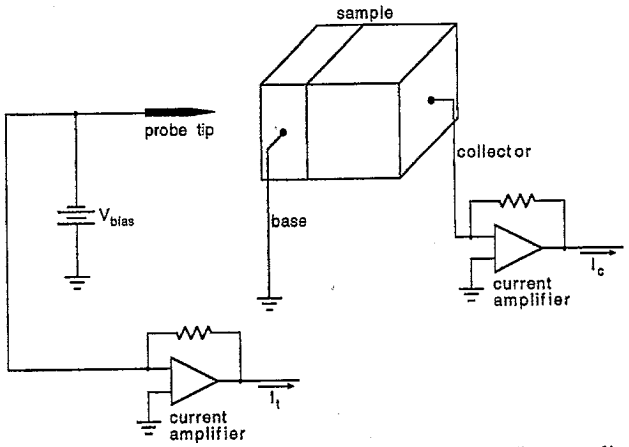

Fig. 9. Schematic diagram for ballistic electron emission microscopy (BEEM). The tunneling current I_t may be measured directly or used in a feedback loop to control the tip–sample separation, as in conventional STM. Measurement of the current I_c arising from carriers transported ballistically from the tip into the collector allows the electronic structure of a subsurface interface to be probed.

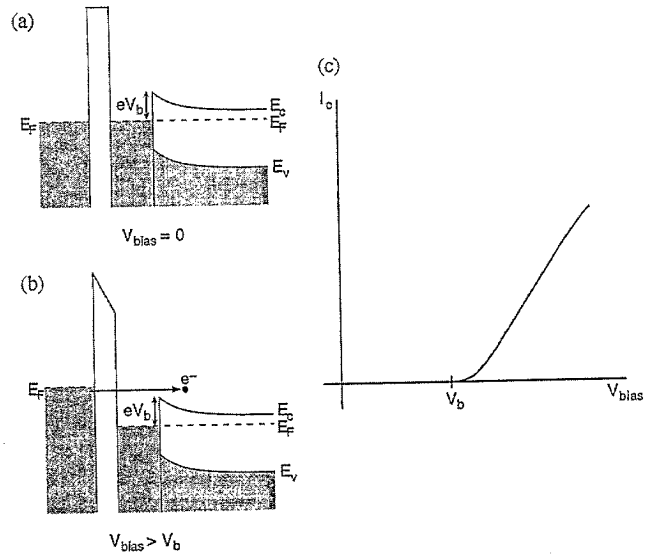

Fig. 10. Schematic energy-band diagram for (a) $V_{bias} = 0$ and (b) $V_{bias} > V_b$ in ballistic electron emission microscopy performed on a Schottky barrier system with Schottky barrier height eV_b. The metal layer in the Schottky barrier structure acts as the base, and the semiconductor as the collector. Ballistic transport of carriers across the metal–semiconductor interface for $V_{bias} > V_b$ yields the current–voltage characteristic shown in (c).

theoretical modeling [65–68], the threshold voltage for the onset of collector current can be used to determine the Schottky barrier height; furthermore, the detailed shape of the current–voltage characteristic can provide information about transport across the buried interface and also about various features in the electronic band structure of the semiconductor. Similar measurements can be made for p-type metal–semiconductor Schottky barrier systems, with holes rather than electrons undergoing ballistic transport across the interface [69].

The spatial resolution attainable in BEEM and the detailed behavior of the BEEM current as a function of voltage should depend on the degree to which the component of carrier momentum parallel to the interface, $\hbar\vec{k}_t$, is conserved during ballistic transport. Conservation of parallel (also referred to at times as transverse) momentum is often assumed in theoretical studies of tunneling, and comparisons

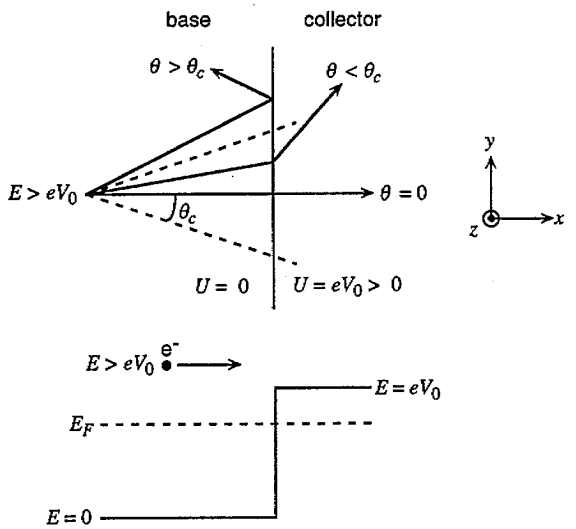

Fig. 11. Critical angle and electron focusing effect in BEEM. If transverse momentum is conserved, an electron with energy E will be transported across the base–collector interface only if its angle of incidence is less than a critical angle θ_c. For semiconductors such as Si or GaAs, θ_c is often 10° or less, corresponding to an expected spatial resolution on the order of ~ 10–20 Å.

of BEEM current–voltage spectra measured for the Au/n-Si (100) Schottky barrier system with spectra calculated with and without the condition of parallel momentum conservation have been used to suggest that parallel momentum is indeed conserved [65]. Specifically, it was shown that the assumption of parallel momentum conservation yielded a quadratic dependence of the collector current on bias voltage near threshold, $I_c \propto (V_{\text{bias}} - V_b)^2$, in agreement with experiment, while relaxation of the parallel momentum conservation law yielded a linear threshold. However, more detailed theoretical modeling of BEEM current–voltage spectra, in which the quantum-mechanical energy dependence of the carrier transmission coefficient at the metal–semiconductor interface was included, suggested that the collector current near threshold should vary according to $I_c \propto (V_{\text{bias}} - V_b)^{5/2}$, independent of whether or not transverse momentum is conserved [67,70].

Conservation of parallel momentum should lead to a substantial electron focusing effect and a corresponding increase in spatial resolution [65,66]. Specifically, for carriers transmitted across the base–collector interface, the energy corresponding to the wave vector component normal to the interface must be sufficient to overcome the metal–semiconductor Schottky barrier. If both the parallel momentum and the total energy of the carrier are conserved, the wave vector of the carrier normal to the interface, k_x, and therefore the direction of propagation, will change as the carrier crosses the potential step at the interface. If a potential barrier exists at the interface, k_x will decrease and the angle of propagation θ (measured from the direction normal to the interface) will increase. A particle incident at an angle greater than a critical angle θ_c will therefore be reflected at the interface, and only carriers whose momenta are contained within a cone $\theta < \theta_c$ will contribute to the current measured at the collector, as shown schematically in Fig. 11. Calculations have shown that for materials such as Si (100) or GaAs, θ_c is considerably less than 10°, corresponding to spatial resolution on the order of 10–20 Å for a metal base layer 100 Å in thickness [65].

2.2. *Other scanning probe microscopies*

The invention of the scanning tunneling microscope led to the development of numerous additional instruments and characterization techniques based to a considerable degree upon the instrumentation developed for STM — most notably, the methods used for the positioning of samples and probes with

extremely high precision. These additional scanning probe techniques have dramatically extended the basic capabilities of STM with regard to flexibility in samples that can be characterized and sensitivity to different properties of samples under investigation. In the following sections we describe briefly a few such techniques. In addition, a number of methods for performing highly localized electrical measurements using scanning probe instrumentation, e.g. scanning capacitance microscopy and Kelvin probe force microscopy, are described in Section 6, in connection with their application to dopant and carrier profiling in ultrasubmicron Si device structures.

2.2.1. Atomic force microscopy

Atomic force microscopy [5], the first of STM's numerous progeny, differs from STM in that atomic and molecular forces, rather than a tunneling current, are detected and used to control the tip–sample separation. AFM therefore allows non-conducting samples to be characterized; however, the sensitivity to electronic structure inherent to STM is largely absent. In AFM, forces are detected by a probe tip mounted on a flexible cantilever, as shown in Fig. 12. Forces acting between the sample and probe tip cause the cantilever to deflect, with the size of the deflection being, to a good approximation, directly proportional to the force. These deflections can be detected by several different techniques, and the deflection signal used to modulate the tip–sample separation in a role analogous to that of the tunneling current in STM. By maintaining a constant cantilever deflection while scanning, one can obtain a profile of constant atomic or molecular force over the sample surface. Much of the technology for AFM and other scanning probe microscopies, particularly the instrumentation for fine- and coarse-scale positioning, was adapted from techniques developed and refined for STM. These have been augmented by the development of techniques for fabricating suitable cantilevers and probe tips, and of a variety of mechanisms for detecting cantilever deflections.

The nature and size of the forces exerted between sample and probe tip vary with tip–sample separation. Intermolecular forces between the sample and tip can be modeled using the Lennard–Jones potential [71], plotted in Fig. 13:

$$V(z) = 4\epsilon\left[\left(\frac{\sigma}{z}\right)^{12} - \left(\frac{\sigma}{z}\right)^{6}\right] \tag{11}$$

The inverse sixth-power term in Eq. (11) describes the attractive Van der Waals force, and the inverse twelfth-power term is an empirical potential accounting for the core–core repulsive force that dominates at small distances. In the contact mode of operation, the separation between sample and tip is very small — comparable to or smaller than that in STM — and the dominant force is the core–core repulsive force between atoms on the sample surface and those at the apex of the probe tip. Typical forces in this regime are 10^{-6}–10^{-9} N. Because of the small tip–sample separation and the strong dependence of the core–core repulsive force on this separation, imaging of individual atoms can be achieved on suitable surfaces.

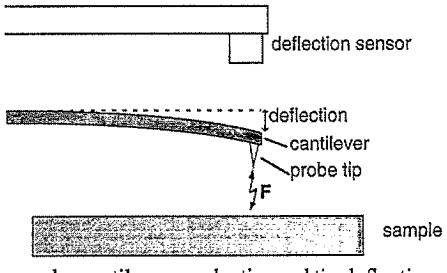

Fig. 12. Schematic diagram showing a sample, cantilever, probe tip, and tip deflection sensor used in atomic force microscopy. Forces acting between the sample and probe tip cause the cantilever to deflect, with the size of the deflection being, to a good approximation, proportional to the force.

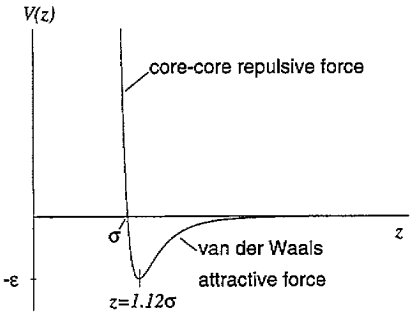

Fig. 13. The Lennard-Jones potential used to describe intermolecular forces between the sample and probe tip as a function of separation z. At small distances, the core–core replusive force dominates, while the attractive Van der Waals force dominates at larger distances.

In the non-contact mode of operation, the separation between sample and tip is larger, resulting in the detection of the longer-range attractive Van der Waals force. The large tip–sample separation generally results in reduced spatial resolution in the non-contact mode compared with that in the contact mode of operation. However, it is possible to sense smaller forces and force gradients in the non-contact mode — sensitivities of $\sim 3\times 10^{-13}$ N and $\sim 1.5\times 10^{-4}$ N/m for forces and force gradients, respectively, have been reported [72]. Furthermore, a wider range of forces is present and can be detected in the non-contact mode — indeed, the development of techniques such as electric force microscopy and magnetic force microscopy has entailed primarily the adaptation of AFM techniques to the detection of electrostatic and magnetostatic forces, respectively.

Cantilevers used to detect these forces can be characterized by a force constant, k, and a resonant frequency, f_0. A small force constant — typically 10^{-2}–10^{2} N/m — is desirable for detection of small forces, since the cantilever deflection is directly proportional to the force but inversely proportional to the force constant. A high resonant frequency for the cantilever — generally greater than 10 kHz — is required to avoid excitation of cantilever oscillation modes during scanning. To achieve both a small spring constant and a high resonant frequency, the cantilever and tip must have very low mass — less than 10^{-6} g to achieve $k<1$ N/m and $f_0>10$ kHz [24]. Typical cantilevers and tips may consist of thin metal wires with the end bent over to form the probe tip, or structures microfabricated from silicon, silicon dioxide or silicon nitride to form an integrated cantilever–tip structure.

Extremely small cantilever deflections can be detected by several techniques [28]. In a number of systems, including the original atomic force microscope, deflection of the cantilever was detected by a tunneling tip mounted behind the cantilever; in these designs, the tunneling current between the tip and cantilever is extremely sensitive to changes in the cantilever deflection [5,73–78], and therefore provides a very effective means of detecting extremely small deflections. However, problems such as contamination of the cantilever or tunneling tip and the possibility of accidental contact between the tunneling tip and the cantilever have led other deflection feedback mechanisms to be employed much more widely. Additional methods for detecting cantilever deflections include the following: measurement of the capacitance between a reference plate and the cantilever [79,80]; optical interferometry [72,81,82]; detection of laser diode feedback with the cantilever acting as a reflector in an external cavity [83]; phase modulation of a polarized laser beam reflected off the cantilever [84]; and deflection of a laser beam reflected off the cantilever [85,86].

In the non-contact mode of operation, resonant enhancement techniques may be employed to improve sensitivity to minute cantilever deflections. For example, a tip with resonant frequency $f_0=(c/2\pi)\sqrt{k}$, where c is a constant dependent on the cantilever and tip mass and k is the cantilever spring constant, may be driven to oscillate at a frequency f. The amplitude A of the oscillation will then be given by [72]

$$A = \frac{A_0(f_0/f)}{\sqrt{1+Q^2(f/f_0 - f_0/f)^2}} \tag{12}$$

In Eq. (12), A_0 is the oscillation amplitude on resonance and Q is the quality factor. In the presence of a force F between sample and tip, the resonant frequency will shift to $f'_0 = (c/2\pi)\sqrt{k - F'}$, where F' is the gradient of the force in the direction normal to the sample surface. If the tip is excited at a frequency $f \neq f_0$, the shift in resonant frequency will induce a change in the oscillation amplitude, from which the force gradient can be derived. Such techniques allow extremely small force gradients to be detected.

2.2.2. Electric force microscopy

In electric force microscopy, the electrostatic force between a conducting probe tip and the sample is detected. This force arises from the separation-dependent capacitance present between the tip and sample when a voltage is applied. Direct measurements of the force are in good agreement with models describing the tip–sample system as a simple capacitor [87,88]. Specifically, the force between the sample and tip is given by

$$F = \frac{d}{dS}\left(\frac{1}{2}CV^2\right) = \frac{1}{2}V^2\frac{dC}{ds} \tag{13}$$

where V is the voltage, s the tip–sample separation, and C the separation-dependent capacitance of the sample and tip. If the tip and sample are assumed to form a parallel-plate capacitor of area A and dielectric constant ϵ, the force F and the force gradient F' are given by

$$F = \frac{1}{2}V^2\frac{\epsilon A}{s^2} = -\frac{V^2}{2\epsilon A}C^2 \tag{14}$$

and

$$F' = \frac{1}{2}V^2\frac{2\epsilon A}{s^3} = \left(\frac{V}{\epsilon A}\right)^2 C^3 \tag{15}$$

Martin et al. [87] have measured electric forces and force gradients as small as $\sim 10^{-10}$ N and 3×10^{-6} N/m, respectively, corresponding to estimated capacitances of 10^{-18} F and 4×10^{-20} F. Fig. 14 shows force measured as a function of tip–sample separation for a tungsten tip and a grounded Si sample, along with theoretical values for the force calculated using the parallel-plate capacitor model. Even this simple model provides a reasonably accurate description of the capacitive force, particularly for lower bias voltages. A few representative applications of electric force microscopy include the detection of variations in dielectric constant on a sample surface [87], detection of localized charge deposited on insulating surfaces [88–90] with resolution sufficient to detect a single electronic charge [91], and delineation of lateral dopant distributions in Si *p-n* junctions [92,93].

In addition to electric force microscopy as described above, a number of additional scanning probe techniques exist based upon the detailed measurement, with extremely high spatial resolution, of forces due to electrical interactions between a sample and the probe tip in the presence of applied bias voltages. These techniques provide the capability to perform conventional electrical characterization measurements such as capacitance–voltage spectroscopy and Kelvin probe measurements with spatial resolution at or near the nanometer scale. Such techniques open up numerous possibilities for probing charge distributions and other electronic properties with extremely high lateral spatial resolution and, by combining scanning probe instrumentation with techniques such as capacitance–voltage spectroscopy, for probing electronic properties in the vertical direction as well. Several of these

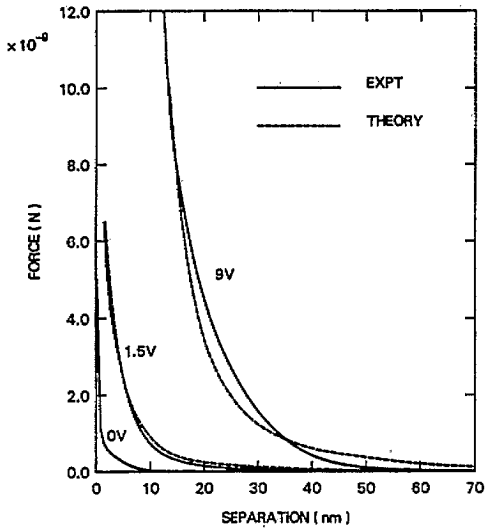

Fig. 14. Experimental and theoretical values for the electric force between a tungsten tip and a grounded Si sample as a function of tip–sample separation. The experimentally measured electric force, indicated by the solid line, is in reasonable agreement with the force calculated using a simple parallel-plate capacitor model, indicated by the dashed line from Ref. [87].

techniques and their application to nanometer-scale dopant profiling in Si microelectronic devices are described in detail in Section 6.

2.2.3. *Magnetic force microscopy*

In magnetic force microscopy, a ferromagnetic probe tip is mounted on the cantilever, allowing magnetic forces between the sample and tip to be detected with extremely high spatial resolution [94,95]. The force between a magnetic sample and tip can be understood by approximating the tip as a magnetic dipole $\mathbf{m}$ in the presence of a magnetic field $\mathbf{H}$ created by the sample. The force on a magnetic dipole $\mathbf{m}$ due to a magnetic field $\mathbf{H}$ is given (in cgs units) by

$$\mathbf{F} = \nabla(\mathbf{m} \cdot \mathbf{H}) \tag{16}$$

If we consider the interaction between two individual dipoles, one in the sample and the other in the tip, the field $\mathbf{H}$ and force $\mathbf{F}$ become particularly simple. For two point dipoles $\mathbf{m}_1$ and $\mathbf{m}_2$ corresponding to the tip and sample, respectively, the magnetic field due to $\mathbf{m}_2$ and the force between the two dipoles are given by [96]

$$\mathbf{H}(\mathbf{r}) = \frac{(3\hat{\mathbf{r}}(\mathbf{m}_2 \cdot \hat{\mathbf{r}}) - \mathbf{m}_2)}{r^3} \tag{17}$$

$$\mathbf{F} = \nabla\left(\frac{3(\mathbf{m}_1 \cdot \hat{\mathbf{r}})(\mathbf{m}_2 \cdot \hat{\mathbf{r}}) - \mathbf{m}_1 \cdot \mathbf{m}_2}{r^3}\right) \tag{18}$$

The total magnetic force between sample and tip can be obtained by calculating the field $\mathbf{H}$ produced by the entire sample and then calculating the force on the tip by integrating Eq. (16) over the magnetic dipoles contained in the volume of the tip. An alternative approach is to integrate Eq. (18) over the entire volumes of the tip and sample to obtain the total force between each dipole in the sample and each in the tip. Using such approaches, simulations of magnetic force microscope images have been obtained for constant force or constant force gradient contours, and such simulations using various models for the tip geometry have been found to agree reasonably well with experimental images [96].

Experimentally, magnetic imaging with a lateral spatial resolution of 50–100 nm can now be achieved quite regularly [97,98], with resolution on the order of 10–25 nm having been reported [99,100]. Magnetic force microscopy has been used to image a variety of magnetic materials and devices, including a magnetic recording head [94], longitudinal magnetic recording media [101–103], and materials for magneto-optical storage [104,105].

2.2.4. Near-field scanning optical microscopy

Another characterization technique based to a large degree upon instrumentation developed for STM and other scanning probe microscopies is near-field scanning optical microscopy (NSOM), in which the diffraction limit present in conventional optical microscopy is circumvented by either illuminating or collecting light from a sample at a distance from the sample that is small compared with the wavelength [106–113]. For near-field optical microscopy in the illumination mode (also referred to as the transmission mode), radiation is incident on an aperture of diameter d, as shown in Fig. 15(a), where d is smaller than the wavelength λ of the incident radiation. On the opposite side of the aperture, the radiation within a distance $\sim d/\pi$ is collimated by the aperture; at greater distances the collimation effect is reduced. A sample placed in this so-called 'near-field' or 'proximity' region will be illuminated over an area corresponding approximately to the aperture opening. By scanning the illuminated aperture over the sample surface and detecting radiation transmitted through or subsequently emitted by the sample, scanning optical microscopy with resolution limited by the aperture size, rather than by diffraction, can be performed. Conversely, detection through such an aperture of radiation from a conventionally illuminated or self-luminous sample — the so-called collection mode, shown in Fig. 15(b) — is also possible. The reflection mode, in which both illumination and detection occur through the aperture as shown in Fig. 15(c), has also been demonstrated [114]. In this mode of operation, however, the signal strength is, for obvious reasons, substantially reduced.

The combination of scanning probe technology with optical imaging and spectroscopy has allowed optical properties of samples to be studied with spatial resolution of ~ 20 nm or better [115,116]. More recently, spatial resolution of ~ 3 nm has been demonstrated in near-field scanning optical microscopy performed using the electric field scattered from the apex of a sharp Si tip as the illumination source [117]. The ultimate spatial resolution of this approach was estimated to be on the order of 1–2 Å, suggesting that near-field scanning optical microscopy with atomic resolution may be feasible.

3. III–V semiconductor characterization

The development of epitaxial crystal growth techniques such as molecular-beam epitaxy (MBE), combined with great flexibility in choice of materials, has allowed semiconductor heterostructure device concepts to be explored extensively in III–V compound semiconductor material systems. Advances in heterostructure materials and device technology have depended to a considerable degree upon studies of, and consequently improvements in, crystal growth techniques and the resulting structure of epitaxially grown layers. As material quality has improved and as device structures have grown in sophistication, it has become increasingly apparent that an understanding of, and ultimately control over, growth processes and epitaxial layer structure at the atomic scale will be needed for realization and optimization of advanced semiconductor heterostructure and nanoscale devices. To this end, III–V semiconductors have been studied extensively by STM in both the planar ((100) or (111) surfaces) and cross-sectional ((110) surface) geometries.

3.1. Characterization of epitaxial growth

Studies of (100) surfaces produced during epitaxial growth by techniques such as MBE are of particular relevance to semiconductor technology. The first STM studies of MBE-grown surfaces, performed by Pashley et al. [118], provided detailed information about the structure of the arsenic-rich (2×4) and $c(2\times8)$ reconstructions of the GaAs (100) surface. In these experiments, MBE-grown samples were capped with a layer of As and transferred through air into an ultrahigh-vacuum analytical chamber in which the As cap layer was removed by heating; surfaces protected in this manner from contamination during transfer were then studied by STM. Low-energy electron diffraction (LEED) studies of these GaAs (100) surfaces yielded a $c(2\times8)$ pattern on the arsenic-rich surface, confirming that the overall surface reconstruction was preserved during the As capping procedure. As shown in Fig. 16, constant-current STM images revealed the formation of As dimers on the surface, with the unit cell of the (2×4) reconstruction consisting of three As dimers combined with a single dimer vacancy, corresponding to an As surface coverage of 75%. The dimers were found to form along

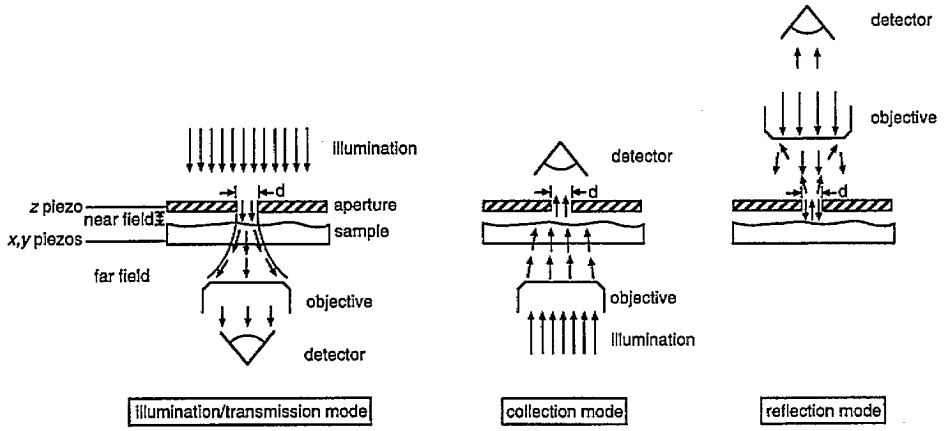

Fig. 15. Schematic diagram of three possible modes of operation in near-field scanning optical microscopy: the illumination (or transmission) mode, the collection mode, and the reflection mode.

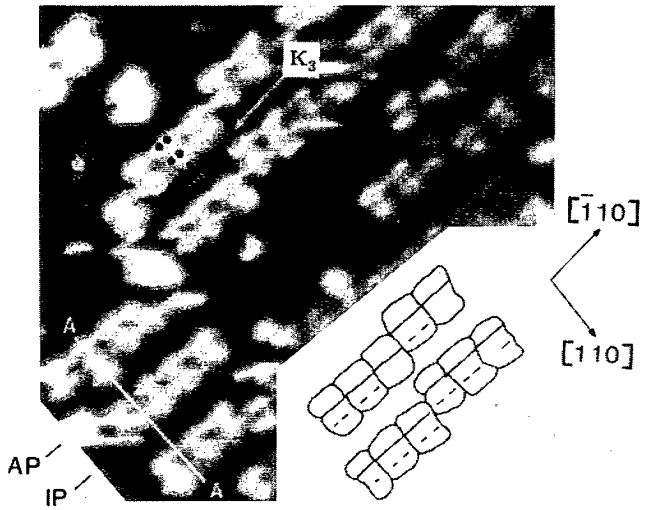

Fig. 16. STM image of the GaAs (100) (2×4) surface. The three As dimers (solid circles) and single dimer vacancy (open circles) indicated in the figure consitute the (2×4) unit cell. Antiphase (AP) and in-phase (IP) missing-dimer boundaries, leading to domains of $c(2\times8)$ and (2×4) respectively, are indicated on the image (from Ref. [118]).

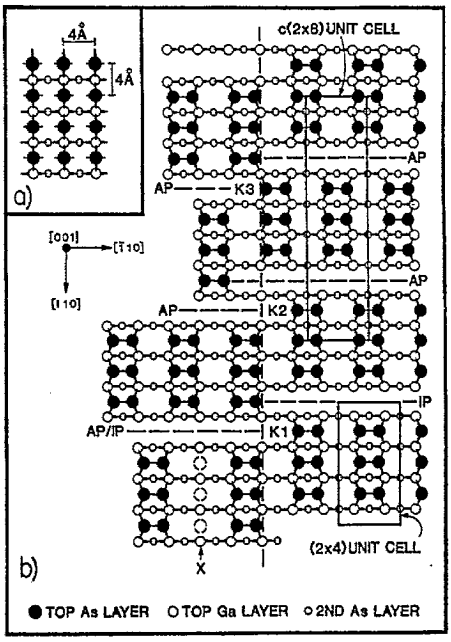

Fig. 17. Structure of the GaAs (100) arsenic-rich surface: (a) unreconstructed surface; (b) reconstructed surface showing the (2×4) unit cell corresponding to the in-phase (IP) missing dimer boundary, and the $c(2\times8)$ unit cell corresponding to the antiphase (AP) boundary (from Ref. [118]).

the [$\bar{1}$10] direction, with every fourth dimer in the [110] direction missing. This result confirmed calculations by Chadi indicating that a unit cell consisting of three dimers and a dimer vacancy was the most favorable energetically [119]. In addition, the $c(2\times8)$ reconstruction was found to arise from a particular configuration of the missing dimer boundary between the three dimer blocks within each (2×4) unit cell. As shown in Fig. 17, the so-called antiphase boundary leads to the $c(2\times8)$ reconstruction, while the in-phase boundary yields the (2×4) reconstruction. At the nanometer scale, both types of reconstruction were found to be present on a given surface, with domains as small as a few unit cells.

While the As capping technique allows oxidation of the sample surface during transfer through air to be prevented, it is necessary to consider the possibility that this procedure does not entirely preserve the atomic-scale structure of the as-grown surface [120]. Several subsequent studies of MBE-grown surfaces have been reported in which samples were tranferred from the MBE chamber into the STM and subsequently imaged without exposure to air. Biegelsen et al. [120] performed atomically resolved imaging of several reconstructions on the GaAs (100) surface, encompassing a wide range of [As]/[Ga] relative surface concentrations. For (2×4)–$c(2\times8)$ surfaces prepared by cooling as-grown samples to 500°C in an As flux followed by quenching, (2×4) cells consisting of three As dimers and one missing As dimer were observed, consistent with the results reported for As capped samples; surfaces annealed for longer periods or at higher temperatures contained (2×4) cells with two neighboring As dimers and two dimer vacancies per unit cell. The basic conclusions reached from imaging of surfaces protected by As capping regarding the structure of the GaAs (001) (2×4)–$c(2\times8)$ surface were confirmed in studies of surfaces transferred entirely under ultrahigh-vacuum conditions; as might be expected, however, samples transferred under ultrahigh vacuum exhibited considerably less roughened and disordered surfaces than those transferred using the As capping technique [120].

Pashley et al. have used a multichamber, combined MBE/STM system to study the effect of Si doping [121,122] and vicinality [123] on the structure and local electronic properties of MBE-grown GaAs (100) surfaces. For growth on vicinal surfaces, a substantial dependence of the monoatomic step structure on the orientation of the step edge was observed: step edges running in the [$\bar{1}$10] direction (parallel to the As dimer rows on the surface) were found to be quite smooth, while those running in the [110] direction (perpendicular to the dimer rows) were very ragged. Such phenomena have significant implications for efforts directed towards, for example, growth of serpentine superlattice structures on vicinal surfaces. In studies of Si doping during MBE growth of GaAs (001), Si concentrations of greater than $\sim 1 \times 10^{18}$ cm^{-3} were found to induce the formation of kinks in the As dimer rows on the surface, with the density of kinks increasing with doped layer thickness until a saturation density that increased with Si concentration was reached. The kinks were postulated to act as surface acceptors which were occupied by electrons from the doped epitaxial layer, thus providing an explanation for the increase in kink density with doped layer thickness, for pinning of the Fermi level near the acceptor state energy, and for the saturation in kink density once the doped layer thickness reached the depletion layer-width. These observations have significant implications for our understanding of electronic structure on epitaxially grown surfaces, and for the formation of Schottky barriers, particularly those involving unreactive metals, on such surfaces.

In addition to atomic-scale characterization of structure and electronic properties on epitaxially grown surfaces, correlations observed between results of other characterization techniques such as electron or X-ray diffraction, which typically probe much larger areas or volumes of the sample under investigation, and direct, atomic-scale imaging by STM, can be particularly valuable. For example, comparisons of STM images with reflection high-energy electron diffraction (RHEED) observations have suggested that during the initial stages of growth, RHEED intensity oscillations are correlated with periodic variations in step density; furthermore, the eventual decay of the RHEED oscillations was found to arise from the development of a surface with a constant step density and stable surface height variation, rather than from a continuous increase in surface roughness [124,125]. Such information provides essential insights into not only the evolution of surfaces during epitaxial growth, but also the interpretation of widely used diagnostic techniques such as RHEED.

Numerous studies of larger-scale structural phenomena such as roughening, island formation, and terrace structure in MBE growth of GaAs (100) have also been reported. For example, anisotropic island or terrace formation has been observed on both nominally flat [124,126,127] and vicinal [123,127,128] GaAs (100) surfaces, with terraces elongated preferentially along the [1$\bar{1}$0] direction. Such observations can help elucidate growth mechanisms in MBE and, in addition, have significant implications for interface formation in semiconductor heterostructures, as surface roughness during epitaxial growth should contribute substantially to interface roughness in heterostructures. For lattice-mismatched heteroepitaxial growth, such as that of InGaAs on GaAs (100) [129], or GaAs on InP (100) or InAs (100) [130], roughening of the epitaxially grown surface, e.g. the development of a 'rippled' surface morphology for InGaAs deposited on GaAs, and the transition from two-dimensional growth to three-dimensional island growth, have been observed by STM.

Atomic force microscopy, in addition to STM, is finding increasingly widespread application to the structural characterization of epitaxially grown semiconductor films and device structures. Because AFM can be used to characterize insulating samples, useful structural information can be obtained from AFM images of epitaxially grown semiconductor surfaces that have been exposed to air and consequently undergone oxidation. However, spatial resolution is usually reduced in AFM performed both in air and under ultrahigh-vacuum conditions compared with that attainable in ultrahigh vacuum STM, and AFM does not provide information about the electronic structure of a sample. Nevertheless, AFM performed in air has become, because of both its enormous utility and its relative ease of use

compared with ultrahigh-vacuum STM, a very widely used, and in fact almost routine, tool for high-resolution structural characterization of epitaxially grown semiconductor films.

For illustrative purposes we describe briefly some early, representative applications of AFM to the study of large-scale surface structure during homoepitaxial growth of GaAs (100). In growth of GaAs (100) at 600°C, Smith et al. [131] observed the formation of ridge stuctures along the $[1\bar{1}0]$ direction, and attributed the observed ridge formation to the higher lateral growth rate in the $[1\bar{1}0]$ direction. This interpretation was consistent with the observation of anisotropic island formation in STM studies of GaAs (100) growth. However, post-growth annealing was found to yield considerably flatter surfaces dominated by misorientation steps. Subsequent studies of GaAs (001) homoepitaxial growth by Orme et al. [132] revealed the formation of mounds elongated along the $[1\bar{1}0]$ direction, but only under growth conditions favoring island formation over step-flow growth. For growth at higher temperatures yielding uniform step flow, island formation was not observed. Large-scale features such as these were found to be consistent with results of STM studies of GaAs (100) homoepitaxial growth, but would not have been as evident in studies focusing upon high-resolution imaging of atomic-scale features on epitaxially grown surfaces.

3.2. *Cross-sectional studies*

Characterization of epitaxial layer structures by cross-sectional STM provides a powerful complement to studies of MBE-grown surfaces. III–V semiconductors are in many ways ideally suited for study by cross-sectional STM. Cleaving of (001) wafers can produce (110) cross-sectional surfaces with atomically flat planes extending over tens to hundreds of nanometers. To avoid contamination of the cleaved surface, cleaving under ultrahigh-vacuum conditions is necessary. Furthermore, for atomically flat (110) surfaces of most III–V materials [133,134] — GaP being a notable exception [135–137] — the Fermi level at the surface is unpinned, and tunneling spectroscopy performed on the surface can yield information about the electronic properties of the bulk material.

The first cross-sectional STM experiments in which actual epitaxial and device structures were investigated were performed by Muralt et al. [138–140]. In these studies, scanning tunneling microscopy and potentiometry were used to probe potential distributions in a GaAs *p-n* junction and a GaAs/$Al_{0.40}Ga_{0.60}As$ double-heterojunction laser structure. Salemink et al. performed the first studies in which a GaAs/$Al_xGa_{1-x}As$ heterojunction interface was resolved directly by scanning tunneling spectroscopy [141], and subsequently extended this work to obtain the first atomically resolved images of GaAs/$Al_xGa_{1-x}As$ heterostructures [142–145]. A number of groups have reported scanning tunneling microscopy studies, both in air and under ultrahigh-vacuum conditions, of GaAs *p-n* junctions [146–148] and GaAs/$Al_{1-x}Ga_xAs$ [148–151], $In_{1-x}Ga_xAs$/InP [152–157], $In_{1-x}Ga_xAs$/GaAs [158,159], and InAs/$Ga_{1-x}In_xSb$ [160,164] heterostructures.

3.2.1. *Electronically induced topographic contrast*

In constant-current cross-sectional images of heterostructures, apparent 'topographic' contrast between the different materials present in the heterostructure is typically observed, with corrugation amplitudes ranging from less than 1 Å to over 100 Å. This contrast is generally ascribed to differences in the electronic properties of the constituent materials, rather than to actual physical topography. Factors such as differing energy band gaps, dopant and carrier concentrations, and electron affinities can contribute to the apparent topographic contrast between materials in a heterostructure. In most cases, however, the observed contrast is consistent with that expected on the basis of variations in band-edge energy from one layer to the next.

To explain the electronically induced topographic contrast observed in such images, we note that the tunneling current integral in Eq. (4) includes factors for the densities of states in the tip and sample

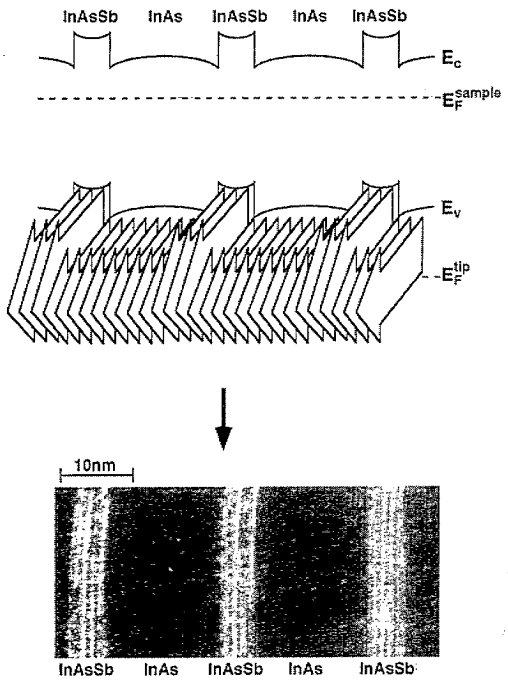

Fig. 18. Current flow in cross-sectional scanning tunneling microscopy performed on an InAs/InAsSb heterostructure. For negative bias voltage applied to the sample, the tip Fermi level, E_F^{tip}, will be below the sample Fermi level, E_F^{sample}, and tunneling of electrons will occur from filled (valence-band) states in the sample into empty states in the tip. The arrows provide a schematic indication of the tunneling current arising from carriers in the sample at energies between the Fermi levels in the sample and tip. Because the electronic structure changes from one layer of the heterostructure to the next, the tunneling current measured for a fixed tip–sample separation varies accordingly. In constant current imaging, the tip–sample separation is adjusted to yield a constant tunneling current, resulting in the observation of electronically induced topographic contrast.

and for the difference between the Fermi distribution function in the sample and that in the tip. At bias voltages typically applied for tunneling in semiconductors, the main contribution to the tunneling current will therefore involve an integral of the sample density of states over the energy range between the Fermi energies in the sample and tip. As shown in Fig. 18, this contribution to the tunneling current will vary from layer to layer in a heterostructure because of the changes in electronic structure from one material to the next. In constant-current imaging, these variations are manifested as changes in the apparent topographic height of the surface as the tip–sample separation is adjusted to yield a constant tunneling current at each point. In complex structures such as superlattices, in which the electronic structure changes considerably from that in bulk material, these effects can become more complex, but the basic principle remains valid.

Fig. 18 shows the band-edge energy structure and a cross-sectional STM image of an InAs/InAsSb superlattice. As shown in the band-edge energy diagram, tunneling occurs over a greater range of states in the InAsSb layers than in the InAs layers. Consequently, maintaining a constant tunneling current requires that the tip–sample separation be increased when the tip is located over the InAsSb layers, leading to an apparent difference in topographic height. Furthermore, an additional periodic structure is visible within each InAsSb layer. This contrast arises from the periodic compositional structure within each InAsSb layer induced by the modulated MBE technique [165,166] employed during the growth of the InAsSb layers in the superlattice. In this growth technique, the average Group V composition in the InAsSb alloy layer is controlled by growing alternating layers of InAs and InSb rather than a random alloy, resulting in the periodic structure evident in the cross-sectional STM image.

The wide range of height differences from layer to layer reported by different investigators is likely to be due, at least in part, to variations in tip and sample cleanliness. If excessive contamination is present on the tip or sample, the apparent barrier height will be anomalously low and the change in tip–sample separation required to maintain a constant tunneling current will be much larger than that for an ideal vacuum barrier. Furthermore, different rates of oxidation in air for different materials in a heterostructure can lead to actual physical topography that is correlated with composition. The latter phenomenon has been observed in AFM studies of $GaAs/Al_xGa_{1-x}As$ heterostructures [167]. In addition, STM studies of InGaAs/InP multiple quantum wells conducted in air revealed that large (tens of angstroms or more) corrugation amplitudes were correlated with low apparent barrier heights and with increases in ambient humidity [153].

3.2.2. Atomic-scale structure of alloy layers and heterojunction interfaces

It has been noted [145,168] that, because STM imaging is sensitive primarily to the one or two uppermost layers on the surface, atomic-scale features in structure and electronic properties can be resolved with considerably greater detail than in other techniques. High-resolution X-ray diffraction can in some circumstances yield information about atomic-scale interface structure in superlattices [169,170], but this information is inevitably averaged over many layers and also over a large area of the sample. Transmission electron microscopy (TEM), particularly the chemical lattice imaging technique [171–173], can provide information about atomic-scale interface structure, but averaging that occurs through the thickness of the sample — typically on the order of 100 Å — limits the technique's ability to resolve features such as atomic-scale interface roughness and fluctuations in composition.

Atomically resolved imaging of cross-sectional surfaces, which thus far has been achieved only for III–V semiconductors and under ultrahigh-vacuum conditions, is therefore a uniquely powerful tool for exploring alloy layer and interfacial structure at the atomic scale. In studies of $GaAs/Al_xGa_{1-x}As$ heterojunctions, Albrektsen et al. [145,174] were able to determine the locations of heterojunction interfaces with a precision of ± 1 unit cell, allowing monolayer steps at the interfaces to be resolved. These studies yielded direct images of step bunching and consequent terrace formation at interfaces for heterostructures grown on GaAs (001) substrates with a 2° miscut in the $[1\bar{1}0]$ direction.

Cross-sectional STM has also revealed the presence of atomic-scale fluctuations in the composition of ternary III–V alloys. In studies of $GaAs/Al_xGa_{1-x}As$ heterojunctions, Albrektsen et al. [174] observed nanometer-scale 'mottling' in constant-current images of the $Al_xGa_{1-x}As$ layers, indicative of nonuniformity in the electronic structure of the alloy that was tentatively attributed to fluctuations in composition. Detailed imaging of a $GaAs/Al_{0.35}Ga_{0.65}As/GaAs$ structure by Salemink and Albrektsen [175] revealed clustering of Al atoms in the ternary alloy with a typical length scale estimated to be two to three unit cells (10–15 Å). Further studies by Johnson et al. [176] confirmed these observations of interface roughness and alloy fluctuations, and revealed Al-rich regions running along the $[\bar{1}12]$ and $[1\bar{1}2]$ directions (as observed on the (110) cross-sectional surface) — possible evidence for preferential growth of Al-rich regions in the $Al_xGa_{1-x}As$ layers. Fig. 19 shows an atomically resolved cross-sectional image of a $GaAs/Al_xGa_{1-x}As/GaAs$ heterostructure. The $Al_xGa_{1-x}As$ layer is clearly lower topographically, on average, than the surrounding GaAs layers, consistent with the valence-band-edge discontinuity at the heterojunction interface. Mottling in the $Al_xGa_{1-x}As$ layer is also visible, reflecting local variations in the Al concentration within the ternary alloy layer. Salemink and Albrektsen [177] have also observed atomic-scale fluctuations in quaternary alloy composition in studies of $InP/In_{1-x}Ga_xAs_yP_{1-y}$ heterojunctions.

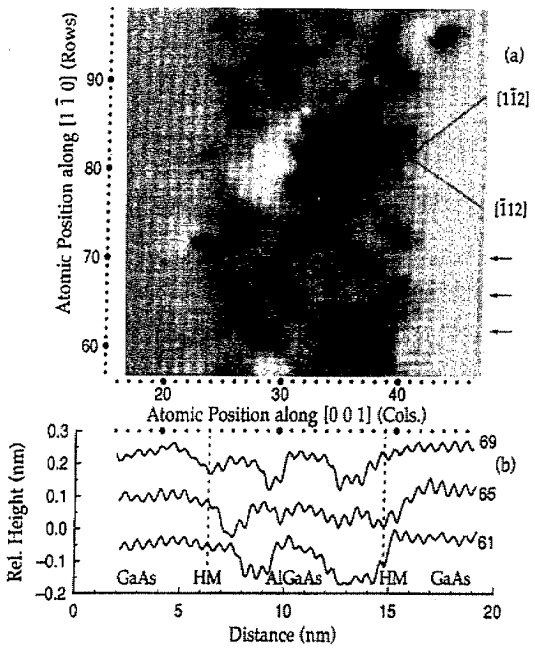

Fig. 19. Atomically resolved cross-sectional STM image of a GaAs/AlGaAs/GaAs heterostructure. Topographic line scans along the rows indicated are shown below the image. The average topographic height within the AlGaAs layer is clearly lower than in the surrounding GaAs, reflecting the change in electronic structure across the interface. Mottling in the AlGaAs layer reflects local variations in Al concentration (from Ref. [176]).

Clustering of In and asymmetric interface broadening have also been observed by STM in cross-sectional studies of $GaAs/In_xGa_{1-x}As$ heterostructures. Zheng et al. [158] found chainlike clusters containing 2–3 In atoms aligned in the [001] direction in coherently strained $In_{0.20}Ga_{0.80}As$ layers grown on GaAs (001) substrates. In addition, segregation of In on the growth surface was found to produce asymmetric broadening at the $GaAs/In_{0.20}Ga_{0.80}As$ interfaces. For $In_{0.20}Ga_{0.80}As$ grown on GaAs, the interfaces were found to be 2–4 atomic layers wide; for the opposite growth sequence, incorporation of excess In segregated on the growth surface was believed to be responsible for producing interfaces extending over 5–10 atomic layers. In cross-sectional STM studies of InGaAs quantum wells and InGaAs quantum wires embedded in $(AlAs)_4(GaAs)_4$ superlattice barriers grown on V-groove patterned GaAs (001) substrates performed by Pfister et al. [159], substantial segregation of In from the InGaAs quantum well and incorporation of In into the subsequently grown $(AlAs)_4(GaAs)_4$ barrier was observed. However, no In clustering beyond that expected statistically for a random alloy was detected, nor was evidence seen for preferential In incorporation at the center of the quantum wire.

Mixed-anion material systems, in which the Group V as well as the Group III constituent changes across a heterojunction interface, are particularly rich in possibilities for complex interfacial structure. In these material systems, two distinct bond configurations — both of which correspond to a structurally perfect heterojunction — can be present at each interface [178]. The InAs/AlSb heterojunction, for example, can contain either InSb-like or AlAs-like bonds at the interface. Furthermore, it has been demonstrated that interfacial composition can exert a considerable influence on electron transport and optical properties [179] in InAs/AlSb quantum wells and superlattices, and on the superlattice band gap and background doping characteristics of $InAs/Ga_{1-x}In_xSb$ superlattices [180].

Cross-sectional STM studies of InAs/GaSb [160–162] and $InAs/Ga_{1-x}In_xSb$ [163,164] superlattices have begun to provide insight into some of these issues. A cross-sectional constant-current

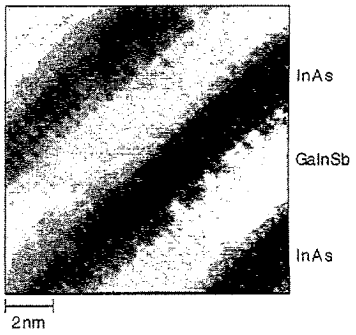

Fig. 20. Cross-sectional STM image of an InAs/$Ga_{0.75}In_{0.25}Sb$ strained-layer superlattice. The bright and dark regions correspond to the $Ga_{0.75}In_{0.25}Sb$ and InAs layers, respectively. Features corresponding to individual atomic orbitals on the Group V sublattice of the cleaved (110) surface are clearly visible, allowing phenomena such as atomic-scale interface roughness and atomic cross-incorporation to be investigated.

image of an InAs/$Ga_{0.75}In_{0.25}Sb$ superlattice is shown in Fig. 20. Atomic-scale interface roughness is clearly visible in the superlattice image. Feenstra et al. [160–162] have performed quantitative studies of interface roughness in InAs/GaSb superlattices as a function of MBE growth conditions. Fourier spectra computed for heterojunction interface profiles obtained from InAs/GaSb superlattices were consistent with a Lorentzian spectral distribution expected to be characteristic of interfaces with random step distributions. A significant dependence of interface structure on growth sequence was observed, with InAs-on-GaSb interfaces being significantly rougher than those in which GaSb was grown on InAs. This dependence of interface roughness on growth sequence was attributed to incorporation of excess Sb from the GaSb growth surface into the subsequently grown InAs layer. Consistent with this interpretation, growth by atomic layer epitaxy and growth at higher substrate temperatures (460°C vs 380°C) were found to yield significant reductions in interface roughness.

Lew et al. [181] have studied the dependence of interface roughness in InAs/$Ga_{1-x}In_xSb$ superlattices on orientation and growth sequence using cross-sectional STM. For growth on GaSb (001) substrates, interfaces imaged in the $(1\bar{1}0)$ cross-sectional plane were found to be significantly rougher, on average, than those imaged in the (110) plane. This observation is consistent with the formation on the epitaxially grown surface of islands elongated preferentially along the $[1\bar{1}0]$ direction during epitaxial growth, a phenomenon that has been widely observed in planar studies of III–V epitaxial growth, as described in Section 3.1. In addition, a strong dependence of interface roughness on growth sequence was observed. For imaging in both the (110) and the $(1\bar{1}0)$ cross-sectional planes, interfaces in which $Ga_{1-x}In_xSb$ was grown on InAs were found to be significantly rougher than those in which InAs was grown on $Ga_{1-x}In_xSb$. Possible sources of the observed dependence of interface roughness on growth sequence include preferential roughening — particularly at spatial wavelengths of ~ 20 Å or more — of the surface during growth of the InAs layer, or greater atomic cross-incorporation or variation in local interface stoichiometry during growth of the $Ga_{1-x}In_xSb$-on-InAs interface.

Studies of InAs/GaSb and InAs/$Ga_{1-x}In_xSb$ superlattices have also revealed clear evidence, in both spectroscopy [160,161] and imaging [163,164], of a dependence of interfacial electronic structure on interface growth sequence; such an asymmetry could arise from a number of sources. As mentioned above, Feenstra et al. [160–162] attributed the asymmetry to incorporation of Sb riding on the growth surface into InAs grown on GaSb. Lew et al. [163,164] have suggested that an additional factor may be the asymmetry in superlattice electronic structure that can arise if different interfacial bond configurations are formed for different growth sequences.

Atomic-scale cross-incorporation and variations in interface composition are also significant issues for heterojunctions containing combinations of arsenide and phosphide compounds, e.g. InP/

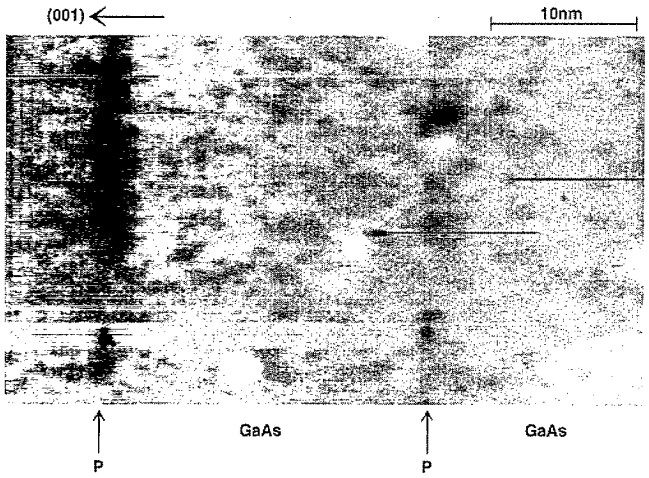

Fig. 21. Cross-sectional STM image of a sample in which growth of GaAs by gas source MBE was interrupted periodically and the sample surface exposed to a pure P_2 flux. Topographic contrast indicated in the image reveals substantial incorporation of phosphorus into the GaAs during the exposure to P_2.

$In_{1-x}Ga_xAs$, $InP/In_{1-x}Ga_xAs_yP_{1-y}$ and $GaAs/In_{1-x}Ga_xP$. Studies of an $InP/In_{0.25}Ga_{0.75}As_{0.5}P_{0.5}$ heterojunction by cross-sectional STM yielded direct images of atomic-scale fluctuations in Group V composition in the quaternary alloy [177]. Recent studies of various arsenide/phosphide heterostructures by cross-sectional STM have revealed considerable dependence of atomic-scale interface and alloy layer structure on growth conditions, with significant implications for the realization and optimization of arsenide/phosphide heterostructure devices. In cross-sectional STM studies of $In_{1-x}Ga_xAs$/InP double-barrier resonant tunneling diodes grown by metalorganic MBE [155,156], a dependence of both interface roughness and interface chemical composition on growth sequence was observed. As in the studies by Feenstra et al. of InAs/GaSb superlattices [160–162], interface profiles were extracted from constant-current images, and spatial frequency spectra were computed from these profiles. Fitting of the resulting spectra to a Lorentzian spectral distribution function revealed that the interfaces in which InP was grown on $In_{1-x}Ga_xAs$ exhibited significantly shorter correlation lengths and larger roughness amplitudes than the $In_{1-x}Ga_xAs$-on-InP interfaces. In addition, constant-current images of the double-barrier regions revealed a growth-sequence-dependent asymmetry in the interfacial electronic structure which was believed to be a consequence of a difference in bonding types at the $In_{1-x}Ga_xAs$-on-InP and InP-on-$In_{1-x}Ga_xAs$ interfaces resulting from the growth procedures used.

Lew et al. [157,182] have demonstrated that considerable atomic cross-incorporation and interfacial grading can occur at arsenide/phosphide heterojunction interfaces, with diffusion during growth interrupts being a significant contributing factor, particularly as the growth temperature is increased. Fig. 21 shows a cross-sectional STM image of a structure in which growth of GaAs by gas source MBE has been interrupted periodically and the surface exposed to a pure P_2 flux. The dark areas in the image are indicative of phosphorus incorporation into the GaAs layers during the growth interrupts; nanometer-scale lateral variations in phosphorus incorporation are clearly visible, and the shape of the phosphide interlayers (generally ragged at the lower interface and smoother at the upper interface) suggests that diffusion of phosphorus into the underlying GaAs is more significant than carryover of phosphorus into GaAs grown after the interrupt. Studies of nominally identical structures grown at different temperatures (450°C vs 550°C) have shown that phosphorus incorporation is dramatically reduced by growth at lower substrate temperatures.

Fig. 22 shows a cross-sectional image of an $In_{1-x}Ga_xAs/InP$ heterostructure grown by low-pressure metalorganic vapor phase epitaxy (MOVPE). The $In_{1-x}Ga_xAs$ and InP layers appear bright

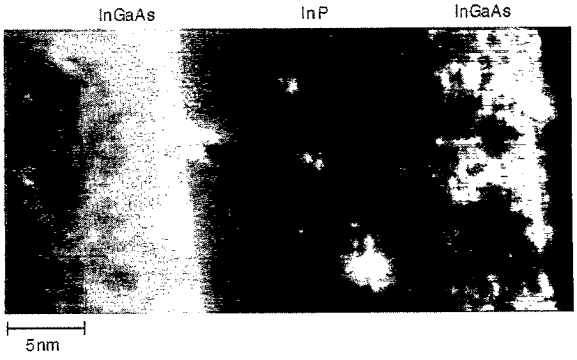

Fig. 22. Cross-sectional STM image of an (001) InGaAs/InP multiple quantum well structure. The direction of growth is from right to left in the image. Growth-sequence-dependent interfacial asymmetry and substantial atomic cross-incorporation are clearly visible.

and dark, respectively. The heterojunction interface structure is clearly dependent on growth sequence, with the $In_{1-x}Ga_xAs$-on-InP interfaces appearing to be fairly abrupt and the InP-on-$In_{1-x}Ga_xAs$ interfaces exhibiting substantial interfacial grading. Arsenic incorporation into InP layers grown on $In_{1-x}Ga_xAs$ is believed to be a significant factor contributing to the contrast in the InP layer near the InP-on-$In_{1-x}Ga_xAs$ interface. In addition, considerable inhomogeneity and a clear asymmetry in electronic structure in the direction of growth are visible in the $In_{1-x}Ga_xAs$ layer. These features could arise from intermixing of either Group III or Group V consituents; however, the reduced contrast near the InP-on-$In_{1-x}Ga_xAs$ interface, combined with the observation of phosphorus diffusion into GaAs during growth interrupts in gas source MBE [182], suggests that phosphorus diffusion into the $In_{1-x}Ga_xAs$ layers during InP growth might contribute substantially to the observed asymmetry in samples grown by MOVPE.

Nanometer-scale electronic properties of heterostructures can be probed by scanning tunneling spectroscopy. Using this technique, Salemink et al. [141] were able to detect the two-dimensional electron gas formed at a $GaAs/Al_{0.5}Ga_{0.5}As$ interface with spatial resolution approaching 1 nm. In subsequent detailed spectroscopic measurements on $GaAs/Al_xGa_{1-x}As$ heterojunctions [142,143], a clear transition in the valence-band-edge energy, occurring over approximately 35–50 Å in the growth direction, was evident. The distance over which the transition from the GaAs to the $Al_xGa_{1-x}As$ valence-band-edge energy occurred was taken to reflect the inherent width of the electronic transition across the heterojunction interface. The observed shift in band-edge energy was quantitatively consistent with the expected band offset for the heterojunction, provided that tip-induced electrostatic band bending in the sample was taken into account.

Detailed, quantitative interpretation of spectroscopic measurements on unpinned (110) surfaces of III–V semiconductors can be complicated considerably by tip-induced band-bending in the semiconductor, as described in Section 2.1.2. However, complications in quantitative data interpretation arising from tip-induced band-bending can, to a limited extent, be circumvented by performing spectroscopic measurements on surfaces for which the Fermi level is pinned. Such an approach is viable provided that the pinning does not completely obscure the electronic properties of the bulk material. Gwo et al. [183] have explored this approach, performing imaging and spectroscopy on sulfide-passivated cross-sectional surfaces of $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructures. Their experiments suggested that the pinning induced by sulfide passivation did not alter the shift in valence-band-edge energy between the GaAs and $Al_{0.3}Ga_{0.7}As$ layers as measured by scanning tunneling spectroscopy, and that spectroscopic measurements were in fact able to probe the bulklike electronic properties of the sample. Pinnington et al. [148] have also used sulfur passivation of the cross-sectional surface to

perform imaging and spectroscopy, in air, of GaAs/$Al_xGa_{1-x}As$ heterostructures and *p-n* junctions. While these experiments demonstrate that sulfur passivation layers can facilitate certain types of spectroscopic measurements on (110) surfaces of III–V semiconductors, the ability to probe atomic-scale compositional structure and electronic properties is considerably reduced. Contrast between alternating layers in a heterostructure can generally be observed, provided the layers are of sufficient thickness. However, atomic-scale details in alloy-layer and interface structure are generally obscured.

3.2.3. Dopant distributions and individual dopant atoms

Characterization of dopant distributions and, indeed, of individual dopant atoms in III–V semiconductors has also been accomplished using cross-sectional STM. Muralt [138] performed the first cross-sectional studies of GaAs *p-n* junctions, using potentiometry to probe the potential distribution across a junction. Feenstra et al. [146] carried out the first detailed imaging and spectroscopic studies of GaAs *p-n* junctions, observing electronically induced topographic contrast in which the *p*-type regions appeared to be ~ 2 Å lower than the *n*-type regions for a sample bias voltage of -2 V. Also observed were unexpectedly large widths for the *n*-type layers compared with those expected from the growth procedure, and correspondingly smaller widths for the *p*-type regions; this was interpreted as evidence for diffusion of Si from the *n*-type layers into the surrounding *p*-type regions. Current–voltage spectroscopy allowed the *n*-type, *p*-type, and depleted regions to be identified unambiguously, confirming the interpretation of contrast in the constant-current images. Images and spectroscopic measurements consistent with these results were obtained in studies of GaAs *p-n* junctions by Gwo et al. [147]. Measurements of tunneling conductivity have been used by Feenstra et al. [184,185] to facilitate the study of *p-n* junctions on cross-sectional surfaces containing relatively high densities of monoatomic steps. In constant-current imaging on these surfaces, the electronically induced topographic contrast between *p*-type and *n*-type regions is most likely diminished by partial pinning of the Fermi level [184], and further obscured by actual topographic features on the stepped surface. Tunneling conductivity, however, was observed to vary with carrier type, allowing *p*-type, *n*-type, and depleted regions to be distinguished. In measurements of tunneling conductivity, the distance over which the transition in conductivity from the *p*-type to the *n*-type value occurred was found to be close to the expected depletion layer-width for the junction, thereby providing a direct measure of the depletion length and, consequently, the dopant concentration.

Pinnington et al. [148] and Tseng et al. [186] have performed imaging and spectroscopy on GaAs *p-n* junctions in air, using sulfide passivation to prevent oxidation of the cross-sectional surface. In both cases, electronically induced topographic contrast was observed between the *n*-type and *p*-type regions, with the *p*-type regions appearing 4–8 Å lower than the *n*-type regions for approximately -4 V bias applied to the sample; this degree of topographic contrast is comparable to that observed for sulfur-passivated GaAs *p-n* junctions studied by cross-sectional STM under ultrahigh-vacuum conditions [183]. In addition, Tseng et al. [186] observed a discrepancy between the apparent widths of the *p*-type and *n*-type regions in cross-sectional images and the layer-widths expected from the growth procedure, with the *n*-type regions being substantially wider and the *p*-type regions narrower than intended. This was attributed to a shift in the apparent position of the *p-n* junction arising from tip-induced band bending effects, rather than diffusion of Si from the *n*-type material into the adjacent *p*-type regions as postulated by Feenstra et al. [146]. However, Gwo et al. [147] observed that the Fermi level on sulfur-passivated cross-sectional surfaces appeared to be pinned, which would tend to minimize tip-induced band-bending effects. While further work is required to understand fully the relative influence of actual sample structure and factors such as surface preparation, tip quality, and tip-induced band bending, it is clear that cross-sectional imaging and spectroscopic measurements with

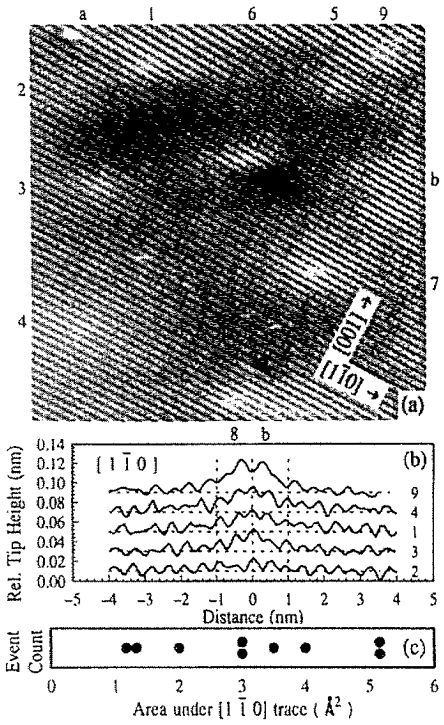

Fig. 23. (a) Cross-sectional STM image of a Be-doped GaAs sample, obtained at a sample voltage of −2.1 V and a tunneling current of 0.1 nA. Individual Be dopant atoms, labeled 1–9, appear as 'hillocks' in the image. (b) Topographic line scans through individual hillocks in (a). (c) Distribution of areas under topographic line scans for each hillock. Larger areas correspond to dopant atoms closer to the surface; it was estimated that dopants up to five monolayers (~10 Å) below the surface produced visible features in the image (from Ref. [187]).

the STM offer the possibility of performing dopant profiling with a spatial resolution approaching 1 nm, far better than the resolution achievable with more traditional characterization techniques.

In addition to nanometer-scale profiling of dopant distributions, cross-sectional STM has been used to study the properties of individual dopant atoms, defects, and other atomic-scale structures in GaAs. It has been demonstrated in high-resolution imaging of cleaved (110) surfaces of GaAs that Be and Zn dopant atoms in GaAs up to four layers below the cross-sectional surface can be detected, appearing as small hillocks in filled-state images of the cross-sectional surface; from the size and shape of the features, dopants at the surface and one layer below the surface could be distinguished from each other and from dopants farther below the surface [187,188]. The appearance of these hillocks was consistent with that expected on the basis of theoretical modeling of the effect of a Coulomb potential on the tunneling current. Fig. 23 shows a constant-current cross-sectional STM image of a Be-doped GaAs sample. Individual dopant atoms, labeled 1–9, appear as 'hillocks' in the image; the features labeled 'a' and 'b' were interpreted as As vacancies and adatoms, respectively. Detection of dopants in this manner was used to obtain dopant profiles in modulation-doped and delta-doped GaAs/AlGaAs epilayers [189]. Results consistent with these were reported by Zheng et al., who obtained images of both Si donors [190] and Zn acceptors [191] in GaAs using cross-sectional STM.

In addition to dopants, features such as As antisite defects in GaAs [192] and As precipitates in low-temperature-grown GaAs [193] have been studied by cross-sectional STM. Given the eminent suitability of III–V semiconductors for characterization by cross-sectional STM and the increasing realization of the importance of atomic-scale material and device properties in heterostructure and nanoscale device technology, it is likely that cross-sectional STM studies of epitaxial layers and device

structures will play a significant role in the development and application of advanced semiconductor heterostructures and nanostructures. Further development and effective utilization of this technique will require effort in a number of areas. A detailed understanding of the relationship between measured tunneling current (and, consequently, images and spectroscopic data) and the actual atomic-scale structure of the sample is essential; theoretical simulations of tunneling experiments are likely to be particularly useful. And systematic comparisons of cross-sectional STM studies with data from various other characterization techniques such as transmission electron microscopy, X-ray diffraction, diagnostics such as RHEED performed during epitaxial growth, and optical and electrical measurements on a wide range of actual device structures will aid in the interpretation of STM data and ensure that high-resolution measurements performed on relatively small areas of a device do indeed provide information representative of the entire device structure.

Finally, while the use of cross-sectional STM for characterization of III–V materials and devices is likely to play an important role in the exploration and development of novel device concepts and high performance devices based on heterostructures and nanostructures, the application of cross-sectional STM to Si-based materials and device structures could profoundly increase its impact on relatively near-term, state-of-the-art commercial semiconductor technology. Work directed toward this goal is described in Sections 4.2 and 6.3.

3.3. Nanometer-scale optical characterization

Optical measurements such as photoluminescence can serve as highly sensitive probes of atomic- to nanometer-scale properties of semiconductor heterostructures. For example, photoluminescence measurements performed on quantum-well structures by Sakaki et al. [194] were able to provide information about atomic-scale interface roughness and layer-width fluctuations in GaAs/$Al_xGa_{1-x}As$ heterostructures. However, such measurements inevitably average such atomic-scale properties over much larger length scales, and provide only indirect, and typically incomplete, information about local optical properties and their dependence on atomic-scale structural and electronic properties of materials and devices. Scanning probe techniques have made possible the direct characterization of optical properties at or near the nanometer scale.

Detection of luminescence induced by recombination of carriers injected during imaging in a scanning tunneling microscope has allowed energy-band profiles and carrier transport characteristics in GaAs/AlGaAs quantum wells to be probed at the nanometer scale [195–197]. In these experiments, *p*-type GaAs/$Al_xGa_{1-x}As$ quantum well structures were cleaved *in situ* in an ultrahigh-vacuum scanning tunneling microscope system. Light emission arising from recombination of electrons injected during constant-current imaging with holes present in the *p*-type material was measured, allowing luminescence properties to be probed with nanometer-scale spatial resolution. Higher luminescence intensity was observed while tunneling into the GaAs layers compared with that observed when injecting electrons into the $Al_xGa_{1-x}As$ layers, with the ratio of luminescence intensity in the different layers increasing with increasing magnitude of the bias voltage. Luminescence contrast from GaAs quantum wells as narrow as 20 Å was observed. For tunneling of electrons into both GaAs and $Al_xGa_{1-x}As$ layers, luminescence at photon energies corresponding to the GaAs band gap was observed, suggesting that most of the injected electrons diffused to the GaAs quantum well layers before recombining. Indeed, measurement of luminescence intensity as a function of lateral tip distance from a GaAs quantum well was used to estimate the diffusion length in $Al_xGa_{1-x}As$, and the value obtained was found to be in reasonable agreement with previously reported values. Detailed examination of the dependence of luminescence intensity on bias voltage revealed that the onset of luminescence occurred at bias voltages for which the tip Fermi level was just above the bulk conduction band edge in the sample; this contributed to a substantial difference at low to moderate bias voltages between

luminescence intensity for electron injection into GaAs and that for electron injection into $Al_xGa_{1-x}As$. This difference was, as expected, consistent with contrast observed in luminescence imaging of the $GaAs/Al_xGa_{1-x}As$ quantum well structures. A mapping of the threshold voltage for the onset of luminescence as the STM tip was scanned across a $GaAs/Al_xGa_{1-x}As$ multiple quantum well structure was found to correspond to the profile of the conduction band-edge energy in the barrier regions and of the lowest confined-state energy in the quantum wells, with energy variations observable at the nanometer scale.

Near-field scanning optical microscopy (NSOM), by providing the capability for highly localized ($\sim$20 nm to several μm) illumination or light collection, has also made possible the identification of specific luminescence characteristics associated with various atomic- to nanometer-scale features in a heterostructure device. Grober et al. [198] have used near-field scanning optical microscopy to perform low-temperature optical spectroscopy on a $GaAs/Al_xGa_{1-x}As$ quantum wire structure fabricated using cleaved-edge overgrowth. The probe tip used in these studies was $\sim$0.25 μm in diameter, and measurements were performed at 1.5 K. In NSOM measurements performed in the collection mode (sample excited from the far field and luminescence collected locally through the fiber probe), luminescence peaks corresponding to emission both from various quantum-well structures within the sample and from quantum wires formed at the intersections of quantum wells grown on the (001) surface of the wafer with quantum-well structures grown on the cleaved (110) surface were clearly identifiable. Furthermore, specific luminescence peaks corresponding to the quantum-well and quantum-wire structures were seen to arise from the locations of the respective structures within the sample.

Hess et al. [199] have used NSOM to perform low-temperature luminescence measurements on $GaAs/Al_xGa_{1-x}As$ quantum wells. Measurements were made in the illumination mode (localized photoexcitation of the sample through the fiber probe, with the resulting luminescence collected in the far field). Spatially resolved luminescence spectra were obtained which revealed spectrally sharp luminescence peaks arising from recombination of excitons localized by nanometer-scale fluctuations in quantum-well width. Luminescence spectra arising from excitation at different locations varied quite widely. However, averaging together a collection of spectra obtained over a large (6.4 μm $\times$ 6.4 μm) grid yielded a close approximation to the measured conventional (i.e., far-field) luminescence spectrum, thereby demonstrating that the far-field luminescence spectrum from a quantum well is inhomogeneously broadened, consisting of the superposition of luminescence from discrete, spectrally sharp luminescence sites within the well. Broadening in the spectral distribution of luminescence peaks as the quantum-well width was decreased, combined with measurements of the magnetic-field dependence of the luminescence spectra, provided evidence that well thickness variations (as opposed to individual impurities) were responsible for localizing excitons and thereby giving rise to spatially varying luminescence properties.

Optical properties associated with individual defects in a semiconductor material or device structure can also be detected using NSOM. For example, Hsu et al. [200] have used NSOM to detect variations in photoresponse associated with individual threading dislocations in strain-relaxed $Si_{1-x}Ge_x$ films grown on Si (001). Because threading dislocations act as recombination centers, the photoresponse is reduced in the vicinity of a dislocation, with the spatial extent of the region of reduced photoresponse related to both the size of the optical excitation beam and the carrier diffusion length. The combination of NSOM with a conventional photoresponse measurement allowed optical properties associated with individual defects to be characterized with a spatial resolution of better than 100 nm, an order-of-magnitude improvement over the spatial resolution attainable in conventional photoconductivity measurements.

4. Group IV semiconductor characterization

The overwhelming importance of Si in microelectronics technology provides a powerful motivation for applying scanning tunneling microscopy — in both the planar and cross-sectional geometries — to the characterization of Si and Si-based materials. Extensive studies have been performed of fundamental properties of various Si surfaces and of processes such as epitaxial growth, adsorption of atoms and molecules, and etching on Si surfaces. Cross-sectional studies of epitaxial and device structures have been more limited, largely because preparation of a cross-sectional surface suitable for study by STM is much more difficult for Si than for III–V semiconductors. This difficulty stems from the following: first, Si (001) wafers are more difficult to cleave than III–V wafers, although with some care flat (110) cleaved surfaces can be obtained; and second, the as-cleaved (110) cross-sectional surface has been found to be atomically disordered with its electronic structure dominated by dangling-bond states [201]. Despite these complications, nanometer-scale cross-sectional characterization of Si-based materials and devices has been achieved. Detailed atomic-scale studies of such structures will, however, require the ability to prepare cross-sectional surfaces comparable in quality to cleaved (110) surfaces of III–V compounds.

4.1. Characterization of epitaxial growth

STM has been used to perform detailed investigations of epitaxial growth on Si (111) and Si (001) surfaces by both solid-source evaporation [202–212] and chemical vapor deposition [213,214]. In this section we review some studies of the initial stages of Si and Ge growth on Si (001), the surface of greater technological importance. As shown in Fig. 24, atoms on the Si (001) surface form dimers arranged in rows in a (2×1) reconstruction; these rows run alternately in the [110] and [1$\bar{1}$0] directions on terraces separated by monoatomic steps. Long a subject of debate, the structure of the Si (001) 2×1 reconstructed surface was in fact not determined definitively until the advent of atomically resolved STM imaging [12,215,216]. On clean Si (001) surfaces, step edges running parallel to dimer rows on the upper terrace of the step are found to be quite smooth, while those running

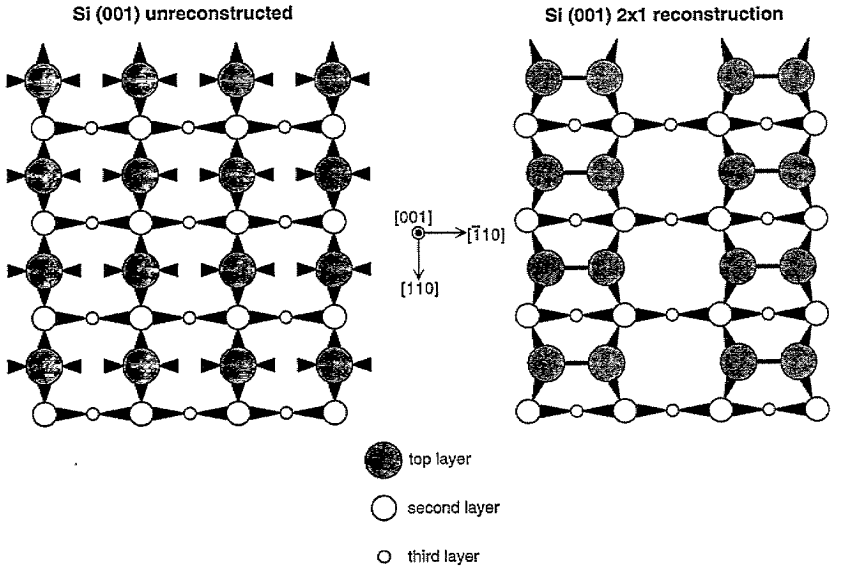

Fig. 24. Schematic diagrams of the unreconstructed Si (001) surface, and of the Si (001) 2×1 surface reconstruction. In the 2×1 reconstruction, Si atoms on the (001) surface form dimer rows running alternately in the [110] and [1$\bar{1}$0] directions on successive terraces separated by monoatomic steps.

perpendicular to the dimer rows are much rougher; these steps and the associated upper terraces have been labeled Type A and Type B respectively [217]. Differences in accommodation coefficients for arriving atoms and in step formation energies for Type A and Type B steps are believed to exert a significant influence on epitaxial growth processes on Si (001) surfaces. At a growth temperature of 750 K, Hoeven et al. [206,207] observed that after deposition of 0.5 monolayers (ML) of Si the Type B terraces expanded to cover the Type A terraces and terminated at the smooth Type A steps. STM images of surfaces after deposition of 0.2 ML of Si suggested that differences in step formation energy, rather than in diffusion coefficients for motion parallel or perpendicular to the dimer rows as proposed by Stoyanov [218], were responsible for preferential growth at the ends of dimer rows forming the Type B terraces.

Detailed studies of homoepitaxial growth on Si (001) surfaces at various substrate temperatures have provided clear evidence of anisotropic growth and further information about its origins. Hamers et al. [204,205] observed the formation of islands highly elongated along the dimer row direction, as seen in Fig. 25; aspect ratios of up to 30:1 were observed for 0.1 ML Si deposited at 580 K, decreasing to ~5:1 for deposition at 750 K. Deposition at higher temperatures also resulted in the formation of larger islands, as expected because of the increased diffusion length. Similarly, Mo et al. [202,209] observed anisotropic island formation, with aspect ratios up to 10–15:1, for submonolayer deposition of Si on Si (001) at growth temperatures ranging from 300 K to 575 K. However, the island shape anisotropy was observed to decrease upon annealing to approximately 2–3:1. These experiments were interpreted as indicating that the large anisotropies observed during growth were a consequence of a difference in the accommodation coefficient for atoms approaching the side of a dimer row compared with that for atoms approaching the end of the row. Estimates of diffusion coefficients, based on island density observed by STM combined with Monte Carlo calculations, suggested that diffusional anisotropy plays a minor role in determining island shape. More detailed studies revealed that the diffusion coefficient along a dimer row was in fact on the order of 1000 times larger than that in the orthogonal direction [219]; however, this anisotropy in the diffusion coefficient was not thought to contribute significantly to the island shape anisotropy. Finally, the reduction in island shape anisotropy upon

Fig. 25. STM image of a Si (001) surface following deposition of 0.1 monolayer Si at 580 K. Monolayer islands elongated along the dimer row direction for each terrace on the surface are clearly visible (from Ref. [205]).

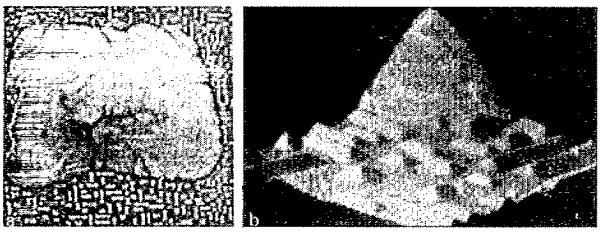

Fig. 26. STM images of Ge clusters formed during heteroepitaxial growth on Si (001): (a) 8000 Å×8000 Å image of a large three-dimensional cluster approximately 250 Å high surrounded by 20–50 Å high hut clusters; (b) 1500 Å×1500 Å magnified view of hut clusters and one corner of a large cluster (from Ref. [203]).

annealing suggested that island shape during growth was significantly different from the equilibrium shape.

In addition to investigations of homoepitaxial growth on Si (001), studies have been performed of heteroepitaxial growth of Ge on Si (001) [203,210,219,220]. Diffusional anisotropy and anisotropic island shape very similar to those observed for growth of Si were observed for deposition of Ge on Si (001). In addition, the transition between two-dimensional, strained-layer growth and three-dimensional cluster growth was observed directly by STM. For deposition of 3 ML or less at temperatures of ~775 K, Ge growth was observed to be two-dimensional, albeit with a rough growth front that became smoother upon annealing at ~875 K. Beyond 3 ML, large three-dimensional islands were observed to form, in agreement with previous observations. In addition to these large islands, a large number of much smaller 'hut'-shaped clusters were observed. Fig. 26 shows a large three-dimensional Ge cluster, approximately 250 Å high, surrounded by many smaller hut clusters of height ranging from 20 Å to 50 Å. All four facets of the hut clusters were found to be {105} planes, with the principal axes of the clusters forming in the ⟨100⟩ directions, i.e. at 45° to the dimer rows. Studies of growth on miscut Si (001) substrates suggested that the hut clusters nucleate along ⟨100⟩ steps on the Si surface [210]. Furthermore, these hut clusters were observed to form only at growth temperatures below 800 K, and were not observed on surfaces grown or annealed at 850 K. On the basis of these observations, Mo et al. [203,210,220] postulated that the barrier for formation of hut clusters is much smaller than that for formation of the much larger three-dimensional islands, and that nucleation of the former provides a relatively low-energy path for the initial formation of three-dimensional Ge structures that eventually evolve into the much larger islands that are stable at equilibrium and are therefore observed at higher growth temperatures.

AFM studies have revealed similar phenomena in the epitaxial growth of $Si_{1-x}Ge_x$ films on Si (001). In studies of $Si_{1-x}Ge_x$ ($x \approx 0.22$–0.26) growth on Si (001) by ultrahigh-vacuum vapor phase epitaxy at 610°C, Pidduck et al. [221] observed the initial formation of islands and ridges in an isotropic distribution, gradually evolving into islands and ridges oriented along the ⟨100⟩ directions with sides sloped by ~9°–12°. Further growth resulted in the formation of a partially relaxed layer with deep ⟨110⟩ trenches and pyramidal pits with sidewalls sloped at angles of ~9°–16°. Lutz et al. [222] performed detailed quantitative analyses of AFM images of strained $Si_{1-x}Ge_x$ films grown by ultrahigh-vacuum chemical vapor deposition; these studies confirmed the observations of Pidduck et al. [221] and provided much more detailed information concerning the facet structure of $Si_{1-x}Ge_x$ strained film surfaces. For relatively thin films (film thickness ~20 nm for $x \approx 0.30$), islands with {105} facet sidewalls were observed; these structures were noted to correspond to the 'hut' structures observed during growth of Ge on Si (001). For thicker films, deep pits with walls consisting of {518} and {311} facets were observed.

Characterization by AFM of partially to fully strain-relaxed $Si_{1-x}Ge_x$ films grown on Si (001) has confirmed the presence of the well-known 'cross-hatched' pattern in surface morphology arising

from the network of dislocations present in the strain-relaxed film [223–225]. For strain-relaxed $Si_{1-x}Ge_x$ films, the cross-hatch pattern is characterized by ridges and trenches running along the ⟨110⟩ directions on the (001) surface of the film. For films grown at temperatures of ~550°C, the cross-hatched surface topography appeared to be due to steps on the surface caused by individual dislocations in the case of thin films [224], and by dislocation pile-ups in the case of thicker films or films annealed at high temperature [224,225]. These conclusions were supported by studies showing a close correlation between the detailed structure of the cross-hatched surface morphology as observed by AFM, and TEM micrographs showing dislocations in the strain-relaxed films [224,225]. For strain-relaxed, compositionally graded $Si_{1-x}Ge_x$ films grown at higher temperatures (~900°C), evidence was found suggesting that film surface morphology can also be influenced by local strain fields such as those surrounding threading dislocations on the surface [223].

Growth of Si and $Si_{1-x}Ge_x$ alloys by chemical vapor deposition (CVD) has become of increased technological importance in microelectronics with the demonstration of high-performance $Si/Si_{1-x}Ge_x$ heterostructure devices grown by ultrahigh-vacuum CVD [226–228]. Several detailed investigations by STM of atomic-scale processes relevant to CVD growth on Si (001) surfaces have been reported. Studies by Lin et al. [214] revealed that, during CVD growth using disilane, features such as island and step structure evolved in a manner very similar to that observed in solid-source Si MBE growth. STM images of surfaces exposed to disilane at 350°C revealed anisotropic island formation, although with a lower degree of anisotropy than that observed for Si MBE growth under similar conditions. This quantitative difference was attributed to the possibility of having a lower surface mobility under CVD growth conditions due to the presence of hydrogen on the surface coming from SiH_3 dissociation. As in Si MBE growth, increased island size but decreased anisotropy were observed as the growth temperature was increased to ~420–450°C. Furthermore, terraces on the surface exhibited denuded zones in the vicinity of Type B downsteps, consistent with a higher accommodation coefficient at the end of a Si dimer row than along the side. Finally, at ~550°C, i.e. above the hydrogen desorption temperature, multilayer growth was observed with a smooth growth surface, but also with an uneven step distribution compared with that observed on the original surface. As described above, phenomena similar to these were observed in STM studies of Si growth by solid-source evaporation.

STM has also provided insight into the atomic-scale mechanisms of growth by CVD. Boland has used STM to study the chemistry of hydrogen, and its role in CVD growth using disilane precursors, on the Si (001) (2×1) surface [213,229–231]. Fig. 27 shows STM images of a clean Si (001)

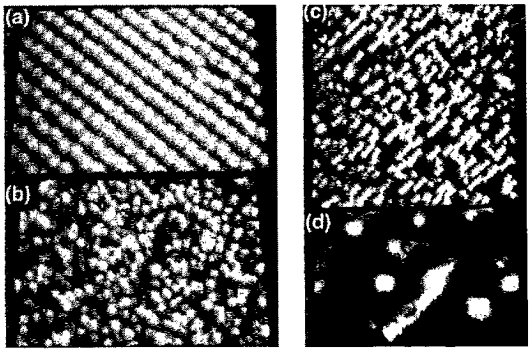

Fig. 27. STM images of (a) a clean Si (001) 2×1 surface and (b) a Si (001) surface following exposure to disilane. Disilane exposure produces SiH_3 fragments on the Si (001) surface, which react with surface dangling bonds or decompose to yield SiH_2 species. Also shown are STM images of the surface in (b) annealed for (c) 10 s at 670 K and (d) 5 s at 650 K. In (c), dimer rows aligned along the [110] direction are visible, while in (d) some dimer rows along with unreacted disilane fragments can be seen (from Ref. [213]).

(2×1) surface and of a Si (001) surface following exposure to disilane. Exposure of a clean Si (001) (2×1) surface, such as that shown in Fig. 27(a), to disilane at room temperature produces SiH_3 on the surface which can react with dangling bonds to form SiH_2 fragments; the STM image in Fig. 27(b) shows these species randomly distributed over the Si (001) surface following a saturation exposure to disilane. Upon annealing, these fragments react to form a new epitaxial layer containing dimer rows with monohydride termination running, as expected, orthogonal to rows on the layer below. Fig. 27(c) shows the surface in Fig. 27(b) following a 10 s anneal at 670 K; 2×1 islands aligned along the [110] direction are clearly visible. Annealing the surface in (b) for 5 s at 650 K yielded the surface shown in (d), in which disilane fragments bonded to the Si surface, appearing as bright features on the surface, are visible along with some dimer row islands. This shows directly the process of decomposition of disilane to form dimers on the Si (001) surface. Further epitaxial growth was observed upon exposure to disilane of a (2×1) monohydride-terminated Si (001) surface at 690 K, at which temperature the monohydride termination is expected to be preserved. This observation suggested that disilane is able to react directly with the passivated, monohydride-terminated surface, resulting in epitaxial growth of Si.

Detailed studies of Si (001) surfaces exposed to disilane at room temperature have made possible the observation, at the atomic scale, of the adsorption of SiH_3, followed by spontaneous dissociation of these groups into SiH_2 and H on the Si (001) surface [232,233]. Thorough analysis of images obtained at different bias voltages, combined with considerations of bond length, bond angle and electron density, allowed specific chemical species such as H or SiH_2 bonded to the Si (001) surface, pure silicon dimers, and monohydride dimers to be distinguished [232–234]. Annealing of these surfaces at 500 K for 5 min resulted in the production of anisotropic islands similar to those observed by Lin et al. [214] in studies of Si growth by CVD. These islands were found to consist of pure silicon dimers, rather than monohydride-terminated dimers as observed by Lin et al.; differences in parameters such as annealing temperature, however, make direct comparisons difficult. Wang et al. [235,236] also studied the interaction of the Si (001) surface with phosphine (PH_3), which is widely used for *n*-type doping of Si during CVD growth. PH_3 was found to adsorb molecularly on the Si (001) surface with fivefold coordination for the P atom; also observed was ejection of Si atoms from the substrate (mostly from existing defect sites) to yield vacancies and Si adatoms. Upon annealing at 950 K, large Si islands were found to form at the surface, originating most likely from ejection of Si atoms displaced by P incorporated in the bulk.

Studies such as these of atomic-scale surface morphology and growth processes provide information essential for atomic-scale control of structure, dopant distribution, and composition in semiconductor devices, particularly at heterojunction interfaces. Control over structure and composition at or near the atomic scale is becoming increasingly important for the realization of advanced heterostructures and nanostructures, and is essential for optimizing performance in a wide range of heterostructure devices.

4.2. *Cross-sectional studies*

Cross-sectional studies are a natural complement to investigations of epitaxial growth. As is the case for III–V semiconductors, detailed cross-sectional imaging and spectroscopy of Si-based materials and device structures ideally requires the production of an atomically flat, electronically unpinned surface. As mentioned earlier, however, cleaving of Si (001) wafers to obtain atomically flat (110) cross-sectional surfaces is highly problematic. Furthermore, the as-cleaved Si (110) surface tends to be disordered, and the Si (110) surface can exhibit a highly complex surface reconstruction. Nevertheless, Johnson and Halbout [237] have shown that an *ex situ* cleave of a Si (001) wafer followed by immersion in dilute HF is able to yield a (110) cross-sectional surface that is nearly atomically flat

and is electronically unpinned. Using this sample preparation procedure, Yu et al. have performed electronic profiling of epitaxially grown Si *p-n* junctions [238], imaging and spectroscopy of Si/$Si_{1-x}Ge_x$ superlattices [239], and two-dimensional electronic profiling of Si MOSFET structures [240]. Spatially resolved spectroscopic measurements obtained on cross-sections of *p-n* junctions grown by MBE revealed systematic variations in current–voltage spectra as the junction region was traversed; an analysis of these variations allowed the potential distribution in the junctions to be mapped out with spatial resolution on the order of 10 nm. In addition, changes in the potential distribution across the *p-n* junction occurring as a reverse-bias voltage was applied across the junction could be detected using potentiometric techniques. Similar spectroscopic techniques have been applied by Yu et al. [240] to obtain two-dimensional profiles of carrier type in Si MOSFET structures with spatial resolution on the order of 10 nm. These studies are described in Section 6.

Cross-sectional STM imaging of Si-based heterostructures has yielded results qualitatively similar to those obtained in studies of III–V heterostructures, but with reduced spatial resolution and sensitivity to local electronic structure because of the lower quality of the Si (110) cross-sectional surface. Electronically induced contrast between Si and $Si_{1-x}Ge_x$ layers similar to that seen in studies of III–V heterostructures has been observed in constant-current cross-sectional images obtained under ultra-high-vacuum conditions of Si/$Si_{1-x}Ge_x$ superlattices [239] cleaved and passivated *ex situ*, and in images of passivated Si/Ge multilayers obtained in air [241]. Fig. 28 shows a cross-sectional STM image of a Si/$Si_{0.76}Ge_{0.24}$ (001) strained-layer superlattice. The cross-sectional surface was obtained using an *ex situ* cleave followed by immersion in a dilute HF solution as described above. The $Si_{0.76}Ge_{0.24}$ layers appear as bright vertical stripes in the image; three $Si_{0.76}Ge_{0.24}$ layers can be seen, with the underlying Si buffer layer visible in the left part of the image. Several monoatomic steps on the cleaved surface, running from the lower left to the upper right in the image, can also be seen. The presence of actual surface roughness reduces the visibility in the grey-scale image of the electronically induced contrast between different materials in the superlattice, although the Si and $Si_{0.76}Ge_{0.24}$ layers can still be distinguished.

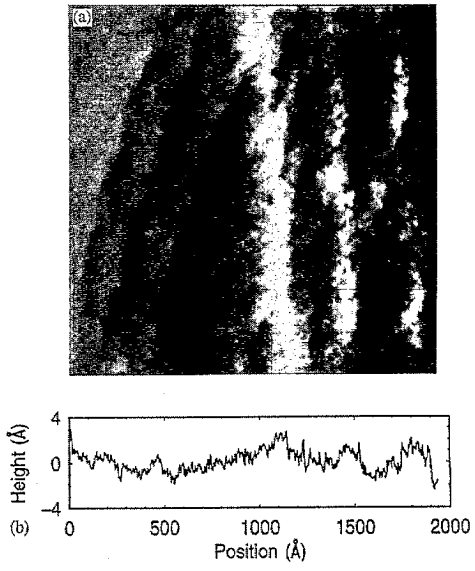

Fig. 28. (a) Cross-sectional STM image of a 260 Å Si/75 Å $Si_{0.76}Ge_{0.24}$ strained-layer superlattice, near the interface between the superlattice and the underlying Si buffer layer. The bright regions correspond to the $Si_{0.76}Ge_{0.24}$ layers, and the dark to Si. Monolayer roughness of the surface is also visible in the image. (b) Line scan across the superlattice; the $Si_{0.76}Ge_{0.24}$ layers appear as peaks in the topography (from Ref. [239]).

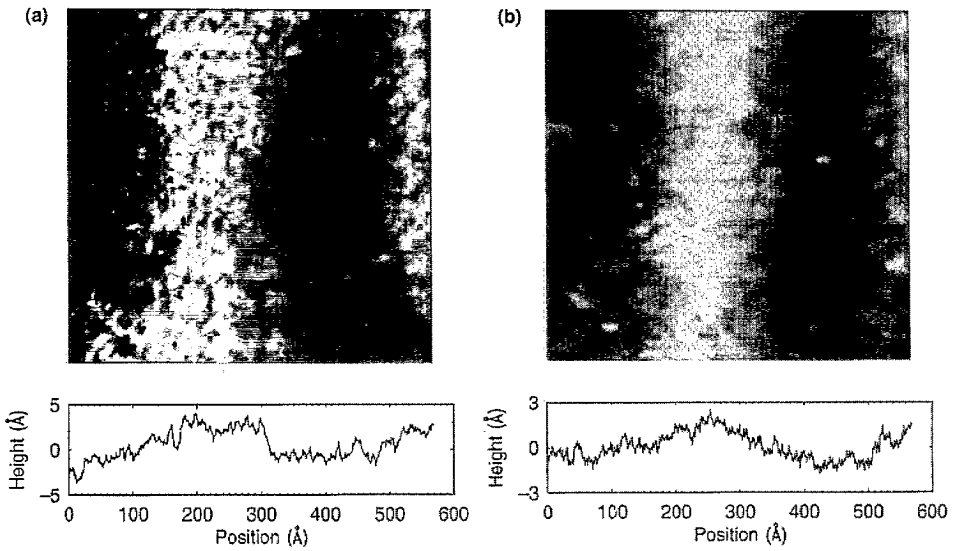

Fig. 29. Cross-sectional STM image of a $Si/Si_{0.76}Ge_{0.24}$ strained-layer superlattice at (a) negative sample bias voltage and (b) positive sample bias voltage. Below each image are single topographic line scans traversing the superlattice layers shown in each image.

Fig. 29 shows more detailed images of the $Si/Si_{0.76}Ge_{0.24}$ superlattice at both positive and negative sample bias. The characteristic shape of the superlattice corrugation is clearly different for images obtained at positive and negative sample bias, as shown in the figure, confirming that the contrast is indeed electronically induced [242]. Also visible in the figure is monolayer-level roughness of the cross-sectional surface induced by the cleaving and HF etching procedure. Such roughness is likely to induce partial pinning of the surface. However, the degree of pinning present apparently is not sufficient to completely obscure the electronic properties of the bulk material, as evidenced by the spectroscopic studies of *p-n* junctions described in Refs. [238] and [240]. Indeed, current–voltage spectra obtained for sequences of points traversing multiple periods of the $Si/Si_{1-x}Ge_x$ superlattice appeared to reflect nanometer-scale spatial variations in the electronic structure of the superlattice [239].

Alternative methods for obtaining high-quality Si (110) cross-sectional surfaces have also been explored. Lutz et al. [201] have performed detailed studies of (110) surfaces cleaved and hydrogen-passivated under ultrahigh-vacuum conditions, and compared measurements from these surfaces to those obtained from samples cleaved *ex situ* and hydrogen-passivated by dipping in HF. Imaging and spectroscopy of (110) surfaces obtained by *in situ* cleaving revealed that the as-cleaved surface is disordered, with dangling-bond states in the band gap; substantial variations in local electronic structure were evident from spectroscopic measurements performed on as-cleaved surfaces. Upon exposure to atomic hydrogen, mostly passivated (110) surfaces were obtained, although completely homogeneous passivation of the entire surface was not observed. Spectroscopic measurements on epitaxial *p*-type and *n*-type Si layers indicated that surfaces prepared in this manner were partially pinned; however, *p*-type and *n*-type material could clearly be distinguished. Compared with the *ex situ* cleave and HF passivation, the *in situ* approach yielded somewhat less homogeneous passivation but offered the possibility of reduced contamination and consequently more stable tunneling characteristics.

A comparison of images and spectroscopy obtained from (110) cross-sectional surfaces of Group IV and III–V semiconductor heterostructures makes evident the importance of surface quality in cross-sectional scanning tunneling microscopy. The atomically flat, electronically unpinned (110) surfaces obtainable by *in situ* cleaving for III–V semiconductors allow structure and electronic properties to be probed with atomic resolution, as described in Section 3. For Group IV semiconductors, resolution

and sensitivity to bulk electronic properties are limited to the nanometer scale by roughness, contamination, or inhomogeneous passivation on the (110) cross-sectional surface.

5. BEEM characterization of buried interfaces

As semiconductor devices shrink in size, nanometer-scale variations in the properties of metal–semiconductor contacts will exert an increasing influence on the properties of individual devices and on uniformity across large numbers of devices. The detailed, atomic-scale structure of both semiconductor–semiconductor and metal–semiconductor interfaces can exert a profound influence on electronic properties such as band offsets and Schottky barrier heights at these interfaces via the formation of localized states and dipole layers at the interface. Nanometer-scale variations in composition and structure at interfaces could therefore produce corresponding variations in the electronic properties of the interface. In addition, the discreteness of dopants and other impurities can lead to significant fluctuations in electronic properties at the nanometer scale. A detailed understanding of the origin and nature of such variations will be crucial for reliable fabrication of nanoscale device structures.

5.1. Metal–semiconductor contacts

Ballistic electron emission microscopy (BEEM) allows the electronic properties of metal–semiconductor contacts to be probed with nanometer-scale resolution. As discussed in detail in Section 2.1.5, BEEM requires a three-terminal configuration, shown schematically in Fig. 30, with contacts to the tip, base and collector layers. A bias voltage is applied between the tip and the base, and the total tunneling current I_t measured in the tip may be used to control the tip–sample separation and also to perform constant-current imaging, as is done in conventional STM. Measurement of the collector current I_c, which arises from electrons transported ballistically through the metal layer and across the metal–semiconductor interface, allows the electronic properties of the buried interface to be probed. Specifically, a large increase is observed in I_c when the applied bias voltage exceeds the barrier voltage.

In the earliest BEEM experiments, Kaiser and Bell used BEEM to investigate the properties of Au/Si and Au/GaAs Schottky barrier contacts [64,65]. Thin films ($\sim$100 Å in thickness) of Au were evaporated on chemically etched Si (001) and GaAs (001) wafers. Because the electron attenuation length in the metal layer is expected to be greater than 100 Å, electrons with injection energies greater than the Schottky barrier height should be transported ballistically across the metal–semiconductor interface. The detailed dependence of the collector current I_c on bias voltage V can be used to determine the local Schottky barrier height V_b, and variations in I_c can, under appropriate conditions, be used to probe local fluctuations in the electronic structure of the metal–semiconductor interface. However, it is necessary to remain cognizant at all times of the potential influence of the metal surface morphology, in addition to the Schottky barrier height, on I_c.

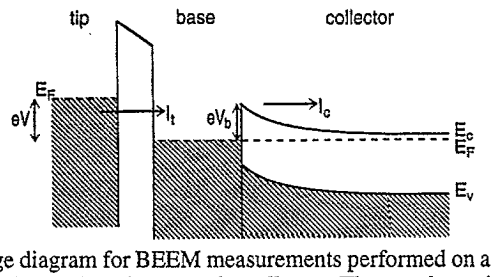

Fig. 30. Schematic energy-band-edge diagram for BEEM measurements performed on a metal–semiconductor junction. The metal film acts as the base layer and the semiconductor as the collector. The metal–semiconductor Schottky barrier height is V_b, and a bias voltage V is applied between the tip and base.

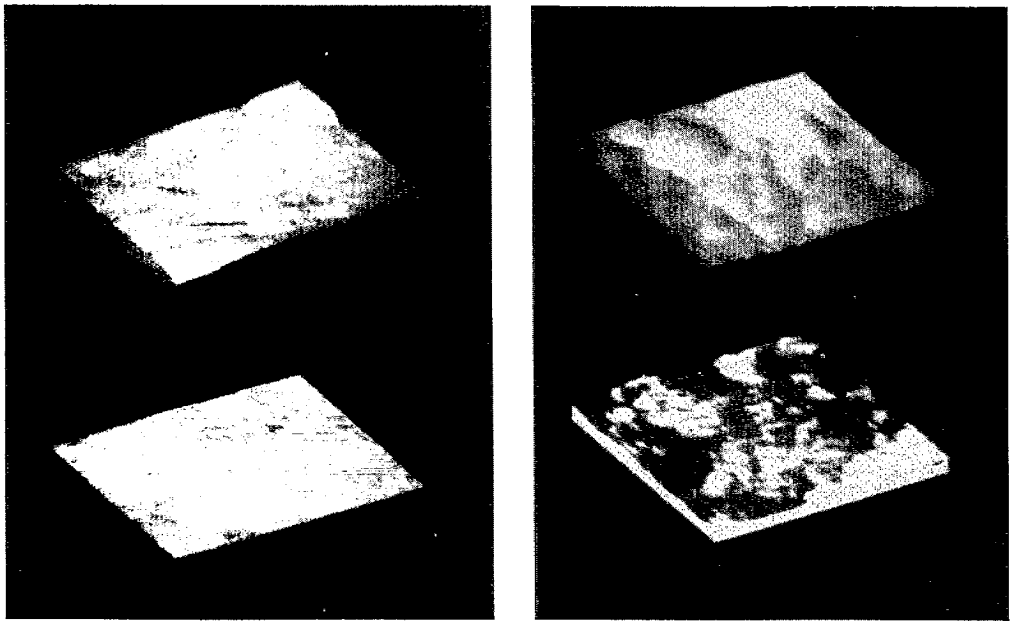

Fig. 31. Constant current STM images of Au deposited on n-Si (100) (upper left) and of Au deposited on n-GaAs (100) (upper right), and BEEM current images of the same structures (lower left and lower right respectively). For the Au/n-Si structure, the image area is 510 Å×310 Å, the surface height range for the STM image is 80 Å, and the RMS variation in the BEEM current is 0.7 pA. For the Au/n-GaAs structure, the image area is 510 Å×390 Å, the surface height range is 63 Å, and the BEEM current I_c ranges from 0.1 pA (black) to 14 pA (white) (from Ref. [66]).

BEEM measurements performed by Kaiser and Bell on Au/Si (001) and Au/GaAs (001) junctions revealed significant differences in the spatial variation of the collector current measured at fixed bias voltage and fixed tunneling current for the two material systems. Fig. 31 shows topographic and BEEM current images of Au/n-Si (100) and Au/n-GaAs (100) structures. For the Au/n-Si interface, little spatial variation in the BEEM current I_c was observed, suggesting that the electronic properties of the interface were quite homogeneous even at the nanometer scale. In contrast, BEEM images of the Au/n-GaAs interface revealed large spatial variations in I_c at length scales as small as $\sim$20 Å, with no direct correlation observed between these variations and features in the surface topography measured simultaneously. It was suggested that these variations may arise because of dissociation of GaAs at the Au/GaAs interface, which can lead to diffusion of Ga to the Au surface and formation of As islands at the interface [243].

Substantial variations in the local, nanometer-scale electronic properties of metal–semiconductor interfaces have also been observed in other material systems. BEEM studies of the Au/n-CdTe interface by Fowell et al. [244,245] revealed considerable nanometer-scale spatial variation in Schottky barrier height, which ranged from $\sim$0.7 eV to 1.1 eV over a 200 Å×400 Å area. Areas of low barrier height were thought to arise from small regions of excess Te at the Au/CdTe interface; such regions could explain large variations in Au/n-CdTe Schottky barrier heights obtained from I–V measurements performed on large-area diodes, in which the current could be dominated by small patches with low barrier heights. In contrast, studies by Fowell et al. [245] of Schottky barriers formed by evaporation under ultrahigh-vacuum conditions of Au on clean, MBE-grown GaAs indicated that the Au/n-GaAs barrier height was highly uniform on the nanometer scale, with a barrier height measured by BEEM of 0.82 $\pm$ 0.05 eV. However, it was also observed that BEEM measurements on the Au/n-GaAs samples degraded over a period of several days, suggesting that the detailed structure and composition of, and

the possible presence of contaminating species at, the metal–semiconductor interface can exert a substantial influence on the electronic behavior of the Schottky barrier structure.

It is essential to note that variations in BEEM current measured across a metal–semiconductor interface are not necessarily correlated directly with variations in the electronic structure of the interface. BEEM studies performed under ultrahigh-vacuum conditions of interfaces formed by evaporation of various metals on *n*-GaP (110) have shown that variations in BEEM current can be observed even across interfaces for which the barrier heights measured by BEEM are highly uniform; these variations were observed to be related to gradients in the surface topography, rather than variations in Schottky barrier height [67,68]. Such a dependence of BEEM current on surface topography was explained by noting that the wave vector of an electron tunneling into a sloped surface will have a smaller component normal to the metal–semiconductor interface than that of an electron injected with the same total energy over a flat area. Since the probability of ballistic transmission across the Schottky barrier depends most strongly on the normal, or 'forward', component of the wave vector, the BEEM currents from areas with sloped surfaces would be lower than those measured over areas with flat surfaces, even in the absence of local variations in the Schottky barrier height or other electronic properties of the metal–semiconductor interface.

Spatially resolved measurement of the local Schottky barrier height using BEEM should provide a more direct probe of variations in the electronic structure of metal–semiconductor interfaces. Nanometer-scale, statistically significant lateral variations in Schottky barrier height have been measured by Talin et al. [246,247] for Au/*n*-GaAs and Au/PtSi/*n*-Si (100) diode structures. The total range of these variations was found to be ~ 0.1 eV in both cases, and no correlation was detected between variations in Schottky barrier height measured by BEEM and roughness of the sample surface as determined by cross-sectional transmission electron microscopy and by constant-current STM imaging of the surfaces on which BEEM measurements were performed. Detailed measurements of local electronic properties such as Schottky barrier heights using BEEM, and comparison of these results with variations that would be expected to arise from factors such as the presence of dopant atoms near the metal–semiconductor interface, variations in semiconductor alloy composition, or impurities at the interface, should provide valuable insights into the nature and origins of local variations in electronic properties at metal–semiconductor interfaces.

5.2. *Semiconductor heterojunction interfaces*

BEEM has also been used to probe the electronic structure of semiconductor heterojunction interfaces. In BEEM studies of *n*-type, strain-relaxed InAs/GaAs heterojunctions, a conduction-band offset of ~ 0.72 eV was measured, corresponding to a valence-band offset of ~ 0.35 eV [248,249]. The conduction-band offset in these experiments was determined from a measurement of the overall barrier height ϕ_b for ballistic transport across an Au/InAs/GaAs structure. As shown in Fig. 32(a), the conduction-band offset may be obtained by adding to this barrier height the Fermi energy relative to the InAs conduction-band edge at the Au/InAs interface (Δ) and the energy shift due to electrostatic band bending at the InAs/GaAs interface (Σ). The quantities Δ and Σ were obtained theoretically by a numerical simulation of Poisson's equation in which the conduction-band offset was varied until the overall barrier height ϕ_b in the simulation matched the experimentally measured value. Considerable lateral variation was observed in BEEM current measured at different locations across the device structures, with some correlation between the BEEM current and surface topography being observed; barrier heights, however, varied by only ~ 0.05–0.06 eV or less, which is within the experimental error of the measurement.

Determination of band offsets for the InAs/GaAs material system, and comparisons among experiments and between theory and experiment, are complicated by the large lattice mismatch ($\sim 7\%$)

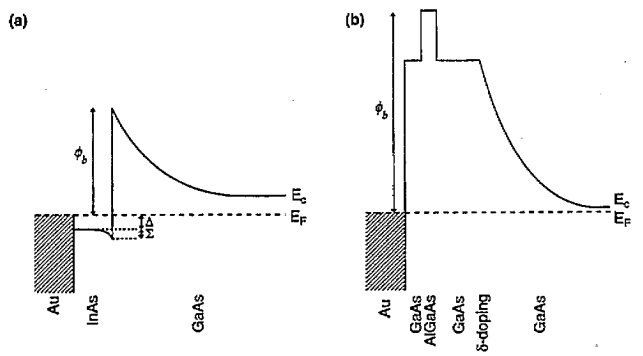

Fig. 32. Energy-band diagrams for structures used in BEEM measurements of conduction-band offsets for (a) InAs/GaAs and (b) GaAs/$Al_xGa_{1-x}As$ heterojunctions. For the InAs/GaAs heterojunction, the barrier height ϕ_b was measured, with calculated values for Δ and Σ added to ϕ_b to obtain the conduction-band offset. For the GaAs/$Al_xGa_{1-x}As$ heterojunction, the conduction-band offset is obtained by measuring ϕ_b for the specific composition $x>0$ and subtracting the barrier height measured for $x=0$; the δ-doped layer is inserted to eliminate electrostatic band bending near the GaAs/$Al_xGa_{1-x}As$ single-barrier structure.

between InAs and GaAs. X-ray photoelectron spectroscopy has been used to measure the valence-band offset for a coherently strained InAs/GaAs heterojunction, yielding a value $\Delta E_v = 0.17 \pm 0.07$ eV [250]. Theoretical models for band offsets have generally yielded small values for the InAs/GaAs valence-band offset: the interface dipole theory of Tersoff [251] yields $\Delta E_v = 0$ eV, the model solid theory of Van de Walle and Martin [252,253] yields $\Delta E_{v,av} \approx 0.17$ eV, and the dielectric midgap energy model of Cardona and Christensen [254] yields $\Delta E_{v,av} = 0.18$ eV, where $\Delta E_{v,av}$ is the discontinuity in the average energy of the heavy-hole, light-hole and split-off valence bands. These values are all somewhat lower than that measured by BEEM. In the structures characterized using BEEM, however, the InAs layers were 100 Å thick, and therefore were expected to have undergone strain relaxation. The likely presence of misfit dislocations in the structure and the uncertainty in the strain configuration at the InAs/GaAs interface make comparisons of this measurement with theory or other experimental results somewhat difficult.

A slightly different approach has been employed by O'Shea et al. [255] to measure conduction-band offsets in single-barrier $Al_xGa_{1-x}As$/GaAs heterostructures using BEEM. In these experiments, heterostructure samples were designed and grown in which band bending at the heterojunction interface was minimized by the incorporation of a delta-doped layer below an undoped GaAs/$Al_xGa_{1-x}As$ single-barrier structure, as shown in Fig. 32(b). For BEEM performed on such a single-barrier structure, the total barrier height measured by BEEM was found to correspond to the combined heights of the GaAs Schottky barrier and the GaAs/$Al_xGa_{1-x}As$ heterostructure barrier. The total barrier height for ballistic transport over the single-barrier structure was measured by BEEM for a range of $Al_xGa_{1-x}As$ compositions, and the conduction-band offset was then determined by comparison of barrier heights for structures having $Al_xGa_{1-x}As$ compositions $x>0$ with the barrier height for a structure with $x=0$. Using this technique, band offsets in good agreement with accepted values [256] were obtained.

The work discussed in these sections has demonstrated that BEEM offers the ability to investigate electronic properties of buried metal–semiconductor and semiconductor–semiconductor interfaces with spatial resolution at or near the nanometer scale. An understanding of, and control over, structure and electronic properties at these length scales is becoming of increasing importance for successful fabrication of advanced heterostructure and nanoscale devices. By providing information about lateral spatial variations in the electronic structure of buried interfaces, BEEM should be a valuable complement to techniques such as cross-sectional scanning tunneling microscopy, which provides direct

information about structure and electronic properties of interfaces and alloy layers with spatial resolution on the atomic scale, but only within the (110) or ($1\bar{1}0$) cross-sectional planes. Among the areas in which further progress should particularly enhance the effectiveness of BEEM for nanometer-scale characterization of buried interfaces are the following: development of a more detailed understanding of the effect of surface morphology on the BEEM current — as shown in the studies of Prietsch and Ludeke [67,68], BEEM currents can be highly influenced by structural features on the sample surface; investigation of correlations of the structure and composition at an interface, determined by scanning probe or other techniques, with the electronic characteristics of the interface as determined by BEEM; and more detailed theoretical modeling of ballistic transport processes in BEEM, particularly if complex interfacial structure exists or for samples in which transport occurs through several layers of a heterostructure device.

6. Nanometer-scale characterization of advanced silicon devices

As feature sizes in advanced Si microelectronic devices such as metal-oxide-silicon field-effect transistors (MOSFETs) enter the ultrasubmicron, and eventually the nanometer-scale, size regime, the ability to characterize and ultimately to control fabrication processes and the resulting structure of a device with nanometer-scale spatial resolution has become essential. Indeed, successful fabrication of ultrasubmicron Si MOSFETs with gate lengths approaching 0.1 μm and below will require the ability to characterize dopant and carrier profiles in the source and drain junction regions of a MOSFET with vertical and lateral resolution approaching 10 nm or better. Nanometer-scale characterization of and control over the source and drain junction profiles in ultrasubmicron MOSFET structures are especially critical for low-voltage, low-power applications that are becoming of central importance in microelectronics. However, such information can be extremely difficult to obtain using traditional characterization techniques such as spreading resistance profiling and secondary ion mass spectrometry (SIMS); the vertical resolution required for effective junction profiling is approaching the limits of these techniques, and the lateral resolution that can be achieved is far from adequate for this application.

A number of particularly promising approaches to this problem based on various scanning probe microscopies have begun to be explored. Recent work, described in Sections 6.1–6.3, has demonstrated the power of scanning tunneling microscopy, and spectroscopy in both the planar and the cross-sectional geometries to delineate the electronic structure of epitaxially grown Si *p-n* junctions and of Si MOSFETs with extremely high spatial resolution. Related techniques such as scanning capacitance microscopy, scanning resistance microscopy, and Kelvin probe force microscopy have also been used for extensive high-resolution characterization of Si *p-n* junctions; these studies are discussed in Section 6.4. As feature sizes in state-of-the-art commercial microelectronic devices such as Si MOSFETs continue to shrink, scanning probe techniques will assume increased importance for performing the nanometer-scale electronic and structural characterization of device structures and fabrication processes that will be essential for reliable, reproducible, and uniform fabrication of large-scale circuits based on ultrasubmicron devices.

6.1. Planar characterization of Si p-n junctions

In an early study of Si *p-n* junctions using STM, Hosaka et al. [257] performed scanning tunneling microscopy and spectroscopy on the (001) surface of Si *p-n* junctions fabricated by implantation of As^+ ions into a *p*-type Si (001) wafer, as illustrated schematically in Fig. 33(a). Implantation was performed using photoresist pattern masking through an 18 nm SiO_2 layer which was etched away in HF and H_2O prior to tunneling. The resulting (001) surface was found to be optically flat, facilitating subsequent tunneling measurements, which were performed under high vacuum conditions

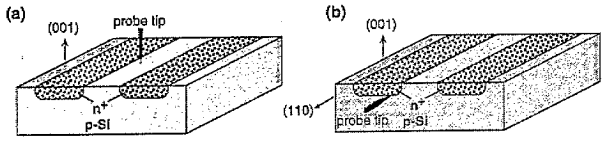

Fig. 33. (a) Planar sample and tip geometry for delineation of Si p–n junctions fabricated by ion implantation. Tunneling measurements are performed on the Si (001) surface, allowing information to be obtained about lateral junction profiles, but not about junction depth. (b) Cross-sectional sample and tip geometry for Si p–n junction delineation. Tunneling measurements are performed on the cleaved Si (110) surface, allowing information about both lateral and vertical junction profiles to be obtained.

(2×10^{-8} torr) to prevent oxidation of the Si surface. Samples were inserted into the vacuum system immediately following removal of the oxide, allowing the hydrogen-passivated, unpinned surface to be preserved during the entire course of the experiment. Constant-current STM images of the implanted samples revealed corrugations between 5 nm and 20 nm in height, with elevated regions appearing near the junctions for images obtained with negative bias voltage applied to the sample. The p-type and n-type regions in the sample were identified using current imaging tunneling spectroscopy (CITS), an imaging technique described in Section 2.1.2. Differences in the current voltage spectra from p-type and n-type regions were very apparent, and current images constructed from tunneling currents measured at +2 V sample bias (with the tip–sample separation fixed by requiring a tunneling current of 2 nA at −2.4 V bias) allowed the structure of the junctions on the (001) surface to be delineated with spatial resolution on the order of ~0.1 μm.

STM characterization of Si junctions formed by ion implantation has also been used to investigate the effect of annealing conditions on the lateral distribution of implanted dopants. Hessel et al. [258] fabricated arrays of Si junctions by implantation of As into a Si (100) substrate doped with boron ($p=2$–3×10^{15} cm^{-3}). The array pattern was formed using polysilicon stripes deposited on a thin gate oxide layer and covered by a ~300 nm oxide layer, and ions were implanted in the regions between these stripes through a 20 nm oxide layer. Implantation was followed by either furnace annealing at 900°C for 60 min or rapid thermal annealing at 1100°C for 30 s. TEM measurements on these samples yielded evidence of substantial lateral scattering of implanted As beneath the polysilicon stripes, and formation of a ~20 nm high ridge of Si below the polysilicon layers.

The samples used in the STM experiments were etched in 50% HF prior to insertion into the ultrahigh-vacuum chamber, yielding a hydrogen-passivated surface suitable for tunneling measurements. Topographic measurements allowed the ridges corresponding to the locations of the polysilicon and oxide mask layers to be identified, and current imaging tunneling spectroscopy was used to determine the carrier type at the sample surface. Spectroscopic measurements revealed that lateral scattering of As during implantation and lateral diffusion during subsequent annealing was sufficient to render the areas masked by the polysilicon regions during implantation moderately n-type. For elevated ridge widths of ~600 nm, the n-type regions were found to be centered underneath the ridges with widths of ~390 nm for furnace-annealed samples and ~285 nm for samples that had undergone rapid thermal annealing. n^+ regions were observed, as expected, near the edges of and between the elevated ridges. These measurements demonstrated the high spatial resolution achievable with the STM, and were quantitatively consistent with SIMS measurements of the extent of vertical scattering and diffusion of implanted As during similar process steps. Studies such as these have yielded considerable information about nanometer-scale lateral dopant distributions in Si devices fabricated under realistic processing conditions, and have provided ample demonstration of the ability of STM to probe, with extremely high spatial resolution, various properties of realistic Si device structures that cannot be effectively characterized by more traditional techniques.

Si *p-n* junctions formed by ion implantation have also been studied using scanning tunneling microscopy and spectroscopy performed in air. LaBrasca et al. [259] performed scanning tunneling microscopy and spectroscopy on the (001) surface of boron-doped Si wafers ($p \approx 10^{15}$ cm^{-3}) on which *p-n* junctions had been formed by implantation of phosphorus through a photoresist mask and 200 Å protective oxide. Prior to tunneling, the samples were cleaned and etched in 1:10 HF:NH_4F; while this is expected to result in a hydrogen-passivated and relatively inert surface, exposure to air during the tunneling measurements is likely to lead to eventual formation of an oxide layer on the surface. It was suggested, in fact, that oxidation of the surface could lead to unpinning of the Fermi level at the Si (001) surface, allowing *p*-type and *n*-type material to be distinguished via spectroscopic measurements; this idea was supported by results of current–voltage spectroscopy performed on *p*-type and *n*-type Si wafers. For the implanted samples, the *p-n* junctions on the Si (001) surface were imaged in both the constant-current and constant height mode, with contrast between the *n*-type and *p*-type regions observable in both modes. While the ability to perform such measurements in air provides numerous practical benefits, considerable caution must be exercised in the interpretation of images, and especially of spectroscopic measurements, because of the possibility of contamination of the tip or sample surfaces during exposure to atmospheric conditions.

6.2. *Scanning probe microscopy and impurity-sensitive etching*

While these experiments demonstrated the efficacy of scanning tunneling spectroscopy in delineating the electronic structure of *p-n* junctions, the geometry employed did not allow information to be obtained about the vertical distribution of dopants in the device structures. In an alternative approach designed to yield information about both lateral and vertical dopant distributions, Takigami and Tanimoto [260] applied an impurity-sensitive etch to a cleaved cross-section of a Si *p-n* junction formed by ion implantation, and performed tunneling measurements, in air, on the resulting surface. Because the etch rate was dependent on the dopant concentration, a topographic image obtained by STM could be translated directly into a profile of the dopant concentration. Quantitative measures of local dopant concentration were obtained by calibrating etch rates using Si samples with known implanted dopant concentrations and subsequently using the measured etch rates to convert topographic measurements obtained by STM to dopant concentration profiles. Vertical dopant distributions obtained using this technique were found to agree well with dopant concentrations determined by SIMS and spreading resistance measurements, and the spatial resolution attainable using the STM technique in combination with impurity-sensitive etching was estimated to be in the range of 10 nm or better in both the lateral and the vertical directions.

More recently, atomic force microscopy measurements in combination with dopant-sensitive etch processes have been used by Raineri et al. [261] and by Barrett et al. [262] to perform dopant profiling in Si MOSFET structures. Samples were cleaved to expose a cross-section of the Si (001) wafer, then polished, and finally etched in an impurity-sensitive etching solution typically consisting of a mixture of HF, HNO_3, and either H_2O or CH_3COOH. The etched cross-sectional surfaces were then characterized using AFM, with the etch depth interpreted as a measure of the local dopant concentration. As in the work of Takigami and Tanimoto [260], calibration of etch rates using Si standards with known dopant concentrations allowed dopant concentrations to be determined quantitatively with dopant concentration sensitivity and spatial resolution comparable to those achieved in the STM experiments, and with results found to be consistent with determinations of vertical dopant distributions using SIMS and spreading-resistance profiling [262]. Among the advantages of using AFM compared with STM in performing topographic measurements on selectively etched device cross-sections are that AFM is less sensitive to the detailed electronic structure of the etched surface and to potential contamination of the sample or tip surfaces, and that imaging by AFM allows surrounding oxide, dielectric, and other

layers present in real device structures to be imaged along with the semiconductor regions of interest. AFM has in fact been used to image polished cross-sections of fully processed VLSI device structures with nanometer-scale spatial resolution [263].

6.3. *Cross-sectional scanning tunneling spectroscopy*

Scanning tunneling microscopy and spectroscopy performed on cleaved cross-sectional surfaces of Si device structures without the intermediate step of impurity-sensitive etching, as shown schematically in Fig. 33(b), offer the possibility of probing more directly the electronic properties of advanced microelectronic devices with nanometer-scale spatial resolution. Kordic et al. [264,265] performed the first cross-sectional STM studies of Si *p-n* junctions, using the scanning tunneling microscope to study cross-sections of implanted junctions exposed by cleaving. Experiments were conducted in which sample cleaving and subsequent tunneling measurements were performed both in air [264] and under ultrahigh-vacuum conditions [265]. In both cases tunneling measurements were peformed directly on cleaved (110) surfaces rather than on surfaces that had undergone hydrogen passivation by immersion in an HF solution. Although the as-cleaved (110) surfaces were most likely to have been electronically pinned, the *p-n* junctions could be detected using potentiometric techniques. Samples were fabricated with separate electrical contacts to the *p*-type and *n*-type regions of the *p-n* junctions, and tunneling currents were measured while forward or reverse-bias voltages were applied across the *p-n* junction (in addition to an overall bias voltage applied to the sample relative to the tip). Differences in tunneling current measured in *p*-type, depleted and *n*-type regions for various bias voltages applied to the *p-n* junctions then revealed the electronic structure of the biased junctions. For experiments performed under ultrahigh-vacuum conditions, the locations of the junctions could be resolved to within ~30 nm using these techniques.

Current imaging tunneling spectroscopy performed by Yu et al. [240] under ultrahigh-vacuum conditions on cleaved, hydrogen-passivated cross-sections of Si MOS structures provided a demonstration of the ability, using STM, to characterize realistic device structures with spatial resolution in both the vertical and lateral directions on the order of 10 nm or better. In this work, MOS structures were fabricated so as to simulate the gate and source/drain junction structure and topology characteristic of 0.1 μm Si MOSFET technology. The sample and tip geometry were similar to that shown in Fig. 33(b). Current imaging tunneling spectroscopy measurements were performed on the exposed cross-sections of the MOS junctions over the region indicated in Fig. 34(a). Spatially resolved tunneling spectroscopy confirmed that clear differences were observable among current–voltage spectra

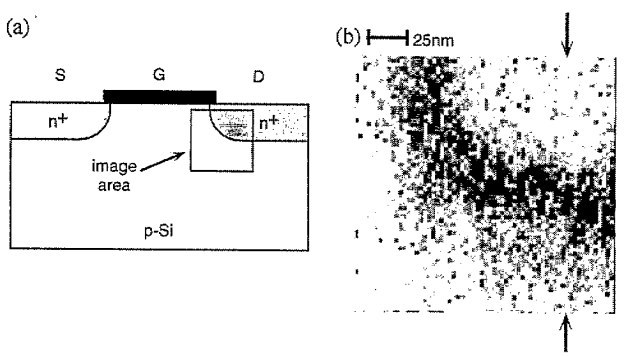

Fig. 34. (a) Cross-sectional schematic of a Si MOSFET structure. Nanometer-scale characterization of the source and drain junction profiles, particularly in the boxed area, is critical in controlling threshold voltages and subthreshold currents in MOSFET devices. (b) Cross-sectional current image, generated at −2 V sample bias voltage, corresponding to the boxed area in (a). The dark band in the image corresponds to the depletion region of the junction, clearly delineating the junction profile with extremely high spatial resolution in both the lateral and the vertical directions.

obtained from p-type, n-type and depleted regions of the junctions. Because the current–voltage spectra differed significantly for the p-type, n-type and depleted regions, current images generated from the spatially resolved tunneling current spectra were able to reveal the profiles of the p-n junctions with spatial resolution in both the lateral and vertical directions on the order of 10 nm.

Fig. 34(b) shows a current image obtained for a sample bias voltage of -2 V, with the tip–sample separation at each point fixed at 1 nA for $+1.5$ V sample bias voltage. As seen in the figure, a small negative tunneling current is present in the n^+ source/drain region, and a somewhat larger negative current in the p-type region. The dark band in the current image, representing large negative tunneling currents present in the depletion layer, clearly delineates the shape of the junction. Fig. 35 shows a profile of the tunneling current along the line indicated by the arrows in Fig. 34. A sharp increase in the magnitude of the tunneling current is seen at the edge of the n^+ region, providing a precise indication of the location of the p-n junction. The depletion layer-width determined from tunneling spectroscopy measurements was found to agree well with that calculated using dopant concentrations obtained from SIMS measurements on the same samples, and the junction shapes seen in the current images were consistent with junction profiles obtained from transmission electron microscopy images of chemically delineated junctions. The ability to perform two-dimensional carrier profiling of source and drain junctions in Si MOSFETs with spatial resolution on the order of 10 nm, as demonstrated in these experiments, will be a critical capability for successful realization and optimization of MOSFET circuits as gate lengths approach 0.1 μm and below.

To fully exploit the power of STM for microelectronic device characterization, detailed modeling of the tunneling process, particularly aspects such as the electrostatic interaction between the tip and the sample, will be essential. Chapman et al. [266] have modeled electrostatic effects and computed tunneling currents for tunneling into Si p-n junctions ($p = 1 \times 10^{15}$ cm^{-3}, $n \approx 1 \times 10^{18}$ cm^{-3}) on the (001) surface, i.e. in the planar geometry. Computed tunneling currents and tip displacements were in qualitative agreement with constant-current images of p-n junctions, although the measured height differences between p-type and n-type regions were several times larger than those expected theoretically. In addition, the simulations suggested that the apparent junction location in topographic and current images can shift by as much as hundreds of nanometers from the actual junction location because of tip-induced band bending near and within the depletion layer. For tunneling with a negative bias voltage applied to the tip, their simulations suggested that the apparent junction location in STM could be shifted by as much as 200 nm into the n-type region. Further study, both experimental

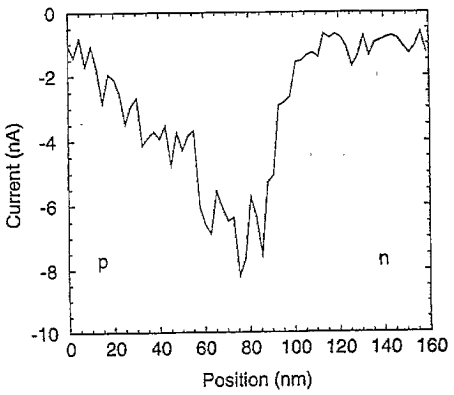

Fig. 35. Tunneling current measured along the line traversing the p–n junction indicated by the arrows in Fig. 34. A sharp increase in the magnitude of the tunneling current is seen at the edge of the heavily doped n-type layer, indicating the location of the junction.

and theoretical, of such effects will be required for STM to become a routine tool for quantitative characterization of microelectronic devices.

6.4. Other scanning probe techniques

A variety of other scanning probe techniques also offer the possibility of characterizing dopant or carrier profiles at or near the nanometer scale, and in some cases may offer significant advantages compared with STM, most notably by permitting greater flexibility in sample preparation and experimental conditions. Scanning capacitance microscopy, in which the capacitance between a sample and a conducting probe tip is measured using an extremely sensitive capacitance sensor [267], has been used to measure dopant profiles in Si *p-n* junction gratings with lateral resolution on the order of 100–200 nm [268,269]. The spatial resolution in these studies was believed to be limited in the most favorable cases by the probe tip radius of curvature, suggesting that capacitance measurements with spatial resolution on the order of ~ 10 nm should be possible. Scanning capacitance microscopy performed on patterned polymethylmethacrylate (PMMA) structures coated with gold has shown, in fact, that spatial resolution of ~ 25 nm can be achieved [270]. More recent work, combining scanning capacitance–voltage measurements with theoretical modeling of the tip–sample capacitance, has demonstrated the utility of this technique for quantitative dopant profiling over dopant concentrations ranging from 10^{17}–10^{20} cm^{-3}, with lateral spatial resolution comparable to the probe tip diameter [271].

Measurements of dopant profiles by scanning capacitance microscopy are performed by bringing a conducting probe tip into close proximity with the surface of the Si wafer. An oxide layer is often deposited either on the probe tip or on the sample surface to prevent the flow of tunneling current between the sample and tip; for this purpose a deposited oxide is often preferable to the native oxide that forms on the Si surface, as the deposited oxide should allow interface and trap state concentrations, and consequently leakage current and spurious charge, to be minimized more effectively. The capacitance between the probe tip and sample is then measured as a function of bias voltage applied between the sample and tip, using an extremely sensitive capacitance sensor as described above. Thus, one is effectively performing capacitance–voltage spectroscopy with lateral spatial resolution comparable to the diameter of the probe tip. Provided that the dopant concentrations vary over distances large compared with the Debye lengths for the dopant concentration range of interest, the carrier density profile obtained in a capacitance–voltage measurement can be taken as a reasonably good measure of the actual dopant concentration profile. Measurements performed on uniformly doped wafers have demonstrated that experimental capacitance–voltage spectra can be obtained with excellent reproducibility, and that the variations in the spectra with dopant concentration agree well with results of simple model calculations of the tip–sample capacitance. For very abrupt dopant profiles or low dopant concentrations, however, the carrier density does not necessarily follow the actual dopant distribution.

The spatial resolution attainable for moderate dopant concentrations can be improved, and the analysis of capacitance–voltage spectra to obtain actual dopant profiles simplified, by performing scanning capacitance microscopy and incorporating a feedback loop in which a tip–sample ac bias voltage is adjusted to maintain a constant capacitance change [271,272]. This feedback control method ensures that the depletion depth beneath the probe tip remains roughly constant even as the dopant concentration changes. If the depletion depth is small compared with the tip radius, the capacitance can be approximated by a quasi-one-dimensional model, allowing dopant concentration profiles to be extracted at reasonable computational expense. This technique has been shown to yield vertical dopant profiles in good agreement with SIMS and spreading resistance profiling measurements [272], and has been extended to yield two-dimensional, cross-sectional profiles of dopant concentration in

implanted junctions, with spatial resolution on the order of 20–150 nm in both the lateral and vertical directions [273].

A related technique for dopant profiling involves the application of capacitive (or electric) force microscopy. In this approach, the capacitive force present between a sample and a conductive probe tip when a bias voltage is applied is used in the feedback loop in an atomic force microscope, as described in Section 2.2.2. The capacitive force varies with dopant concentration, allowing dopant profiling to be performed with spatial resolution limited ultimately by the size of the probe tip. This mode of capacitive imaging of implanted Si *p-n* junction gratings has yielded clear images of the junction structures, with spatial resolution on the order of 100 nm [274].

Another technique sensitive to local tip–sample capacitance, and therefore suitable for nanometer-scale dopant and carrier profiling in advanced Si device structures, is surface scanning harmonic microscopy [275,276]. In this technique, an STM is placed in a microwave cavity with a microwave signal applied across the tip–sample gap. Nonlinearities in the resistance or capacitance of the system lead to the generation of higher harmonic signals; the applied signal can be set at the cavity resonant frequency or some fraction thereof, leading to detection of the fundamental or an appropriate harmonic signal at the cavity resonant frequency. For semiconductors, the higher harmonic signals are found to correspond to successive derivatives of the tip–sample capacitance, which can be modeled as that of a metal–insulator–semiconductor junction. Localized probing of the tip–sample capacitance using this technique has demonstrated the ability to detect changes in dopant concentration for lightly vs heavily doped *p*-type and *n*-type Si samples, and to delineate the profile of implanted p^+-*n* junctions laterally on the surface of a Si (001) wafer with spatial resolution estimated to be potentially as high as ~ 5 nm [276].

Localized measurements of resistance using scanning probe microscopy have also been used to delineate Si *p-n* junction profiles [277–279]. Shafai et al. [277,278] have applied scanning resistance microscopy, in which a conducting probe is used to perform localized resistance measurements on a surface, to characterize Si *p-n* junctions in both the cross-sectional and planar geometries. Differences could be measured in contact resistance among heavily *p*-type, lightly *p*-type, and *n*-type regions, allowing the *p-n* junction profiles to be determined with spatial resolution on the order of ~ 35 nm. In a similar technique dubbed nano-spreading resistance profiling, DeWolf et al. [279] have used localized resistance measurements in an AFM with a conducting probe tip to perform one- and two-dimensional carrier profiling on cleaved and polished cross-sections of Si *p-n* junctions. Measurements were calibrated using sample structures for which the dopant concentrations were known precisely, and results were compared with SIMS and conventional spreading resistance measurements. These measurements demonstrated that nano-spreading resistance profiling is capable of measuring *n*-type and *p*-type carrier concentrations ranging from 10^{14} to 10^{19} cm^{-3} with spatial resolution of ~ 50 nm.

A number of junction profiling methods based upon detection of surface potential variations by scanning probe techniques have also been reported. Weaver and Wickramasinghe [280] have used scanning force surface photovoltage microscopy to profile implanted Si *p-n* junctions. In this technique, the local surface photovoltage generated by illuminating the sample is measured using a scanning probe. If the surface Fermi level is pinned in the band gap, as is the case for bare Si, the sign of the surface photovoltage indicates the local carrier type, and the magnitude is related to the carrier concentration. Surface photovoltage microscopy performed on Si *p-n* junctions fabricated by ion implantation yielded images with clear contrast between *p*-type and *n*-type material and apparent evidence of dopant diffusion that occurred during annealing of the *p-n* junction [280]. Finally, profiling of Si *p-n* junctions has been performed using Kelvin probe force microscopy [281] to measure directly the local surface potential on the hydrogen-passivated (001) surface of the Si wafer [282–284]. In this technique, a conducting probe is scanned over the sample and the probe bias voltage adjusted so

that the electric field between the probe and the sample is eliminated. The probe bias voltage then provides a measure of the contact potential difference between the sample and probe, or equivalently of the local surface potential of the sample relative to the probe tip work function. For a passivated, and consequently electronically unpinned, Si surface, the surface potential is related to the carrier type and concentration, allowing profiling of *p-n* junctions to be performed. Scanning Kelvin probe microscopy measurements performed on junctions fabricated by implantation of boron into *n*-type Si wafers have shown that contact potential differences as small as ~ 5 mV can be measured in semiconductors, suggesting a sensitivity to variations in dopant concentration of $\sim 10\%$ from $\sim 10^{15}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$, and that spatial resolution on the order of 50–100 nm can be achieved [283]. Kelvin probe force microscopy performed by Kikukawa et al. [284] on the (001) surface of Si *p-n* junction gratings was able to yield clear images of junctions produced by both thermal diffusion and ion implantation, and to reveal the sharper junction profile in the implanted junctions, reflecting the steeper dopant concentration profile produced by ion implantation compared with diffusion. Hochwitz et al. [285] have used scanning Kelvin probe microscopy to perform detailed studies of dopant distributions in Si integrated circuit structures, including Si bipolar devices and MOSFET structures.

Continued development of scanning probe-based experimental techniques, in conjunction with extensive computer simulation and modeling, will be required to realize the full potential of these approaches to nanometer-scale Si microelectronic device characterization. The ability to characterize semiconductor fabrication processes and the resulting device structures with nanometer-scale spatial resolution in both the vertical and lateral directions will be essential for continued scaling of Si microelectronic devices and circuits to smaller and smaller dimensions over the coming decade and beyond. Si *n*-MOSFETs with gate lengths of 0.04 μm have been reported [286,287], with gate lengths of 0.03 μm appearing to be feasible [288]. Scanning probe techniques are among the most promising approaches for providing the characterization capability that will be necessary for successful large-scale fabrication of devices at these dimensions.

7. Summary and future trends

Despite a relatively short history, scanning tunneling microscopy and other scanning probe techniques have had a profound impact on semiconductor surface science. In addition, scanning probe techniques are finding increasing application in the characterization of semiconductor materials and device structures of both immediate and long-term technological importance. As the characteristic dimensions of semiconductor devices continue to decrease, the need for detailed nanometer-scale to atomic-scale characterization, which in many situations can be met best — or exclusively — by scanning probe techniques, will grow.

In the fields of epitaxial crystal growth and semiconductor heterostructure materials and devices, STM has provided enormous insight into atomic-scale mechanisms of epitaxial growth, and AFM has rapidly developed into a nearly routine tool for nanometer-scale structural characterization of thin-film surfaces. STM and other scanning probe microscopies performed in the cross-sectional geometry are, and will continue to be, powerful techniques for atomic-scale structural and electronic characterization of semiconductor alloy layers, interfaces, and actual device structures. And ballistic electron emission microscopy provides a unique probe of the local electronic properties of both metal–semiconductor interfaces and semiconductor heterojunction interfaces.

More generally, the technology for extremely precise positioning of a probe tip with respect to a sample, developed originally for scanning tunneling microscopy, has made possible the extension of many conventional optical and electrical characterization techniques to the nanometer scale. Near-field scanning optical microscopy allows optical properties and luminescence characteristics to be

probed at length scales small compared with typical optical wavelengths, providing detailed information about local optical properties of materials and about various highly localized luminescence sources in, for example, semiconductor quantum-well structures that contribute to the overall luminescence spectrum observed in conventional optical measurements. The combination of various electrical measurements with scanning probe technology in techniques such as scanning capacitance microscopy, electric force microscopy, scanning resistance microscopy, and Kelvin probe force microscopy has allowed electrical properties such as capacitance, charge distribution, electric field, resistance, and contact potential to be probed with far higher spatial resolution than could previously be achieved. These measurement techniques are likely to play a central role in the development of processing technology and device structures for ultrasubmicron Si electronics over the next several years, and offer tremendous potential for improving our understanding of and control over the properties and behavior of a wide range of electronic materials and device structures.

As scanning probe technology continues to improve and as new capabilities are developed, the various scanning probe microscopy techniques — particularly those that can be performed in air, as opposed to those that require ultrahigh vacuum — are likely to develop into increasingly routine characterization tools for a wide range of applications. For the most critical applications demanding the highest spatial resolution, however, systems operating in ultrahigh vacuum are still likely to offer the highest level of performance. Realization of the full potential of these techniques is likely to require continued progress in a number of areas. For applications involving metrology for VLSI and ULSI devices and circuits, improved techniques for performing highly accurate dimensional measurements of structures with large aspect ratios and for accurate positioning and measurement over extended areas will be required. For obtaining highly accurate dimensional measurements, accurate characterization of probe tip shapes and extremely accurate measurement of probe position — accounting for hysteresis, creep, and nonlinearity in piezoelectric response, Abbé offsets, and other factors — will be required [289,290]. In addition, novel probe structures incorporating flared tips have been and continue to be developed to enable accurate topographic measurements of lines, via holes, deep trenches, and other structures with steep walls and high aspect ratios commonly encountered in VLSI device and circuit structures [291,292]. A variety of techniques for achieving extremely accurate measurement of and control over probe displacement over large distances are also being explored [293–295]. An additional requirement, the ability to handle large samples, e.g. 8 inch Si wafers, is in fact already available in commercial instruments.

In addition to improvements such as these in experimental capabilities, another key ingredient will be continued improvement in our theoretical understanding, particularly through extensive modeling and simulation, of tunneling and other interactions between the sample and probe tip in a scanning probe microscope. This will be particularly important when the sample structure is highly inhomogeneous, as is the case for many materials and device structures of technological interest, and in situations where it is necessary or desirable to obtain accurate quantitative information about energies of electronic states, dopant or carrier concentrations, or other electronic or optical properties of the sample under investigation. An outstanding example is in the application of scanning probe microscopy to characterization of ultrasubmicron Si MOSFET structures, in which detailed quantitative information, with nanometer-scale spatial resolution, about dopant distributions in a complex device structure is required. Detailed modeling of tunneling, capacitance, and other scanning probe measurements, combined with continued improvements in experimental capabilities, will be essential in meeting the characterization requirements of the microelectronics industry for successful fabrication of such structures over the coming decade and beyond. Such characterization studies, in conjunction with detailed modeling and simulation of fabrication processes and device behavior at the atomic to nanometer scale, are likely to be central to the success of efforts to continue scaling of microelectronic devices to smaller and smaller

dimensions. For more general structural and electronic characterization of VLSI and ULSI structures, approaches incorporating statistical process control may help to improve the accuracy and reliability of quantitative information obtained from scanning probe techniques, allowing such techniques to be used more routinely for process diagnosis in the microelectronics industry [296].

Finally, it will be extremely important to continue to investigate and establish correlations between results of atomic- to nanometer-scale characterization by scanning probe microscopy and information about material and device properties obtained using other measurements that probe properties at larger length scales or are otherwise complementary to scanning probe techniques. This is in fact of great importance for any characterization technique that provides information with extremely high spatial resolution but over a very small area or volume of the sample. For example, comparisons between STM studies of epitaxial growth and results of various *in situ* diagnostic measurements such as RHEED and ellipsometry confirm the consistency of structural information obtained by STM with the long-range periodicity and large-scale structure of the surfaces, and in addition provide information essential for making the most effective use of such *in situ* diagnostic measurements. Correlations established between atomic- to nanometer-scale characterization using scanning probe techniques and results of electrical transport measurements or optical measurements will provide information about the detailed relationship between atomic-scale properties and device behavior, and help confirm that information obtained from measurements over an extremely small area or volume are indeed representative of the whole. In addition to experimental measurements, extensive theoretical work, modeling, and simulation should prove to be extremely valuable in understanding the relationship between atomic-scale structure and various aspects of device behavior.

Fabrication and characterization of nanometer-scale materials and devices have become, and promise to remain, pervasive themes in research in a wide range of fields. As scanning probe techniques continue to progress beyond being ends in themselves, and are applied in an increasingly routine manner to a broad range of problems, they are likely to play a central role in much of the progress that will be made in nanometer-scale science and technology. Work in this area promises to provide fertile ground for exploration and innovation in the coming years.

Acknowledgements

The author would like to acknowledge Professor S.S. Lau for his patience and encouragement during the completion of this article. Part of this work was supported by the National Science Foundation under Award Nos. ECS 93-07986 and ECS 95-01469, and by an Alfred P. Sloan Research Fellowship.

References

[1] G. Binnig and H. Rohrer, *Helv. Phys. Acta, 55* (1982) 726.
[2] G. Binnig, H. Rohrer, Ch. Gerber and E. Weibel, *Appl. Phys. Lett., 40* (1982) 178.
[3] G. Binnig, H. Rohrer, Ch. Gerber and E. Weibel, *Phys. Rev. Lett., 49* (1982) 57.
[4] G. Binnig and H. Rohrer, *Surf. Sci., 126* (1983) 236.
[5] G. Binnig, C.F. Quate and Ch. Gerber, *Phys. Rev. Lett., 56* (1986) 930.
[6] G. Binnig, H. Rohrer, Ch. Gerber and E. Weibel, *Phys. Rev. Lett., 50* (1983) 120.
[7] R.S. Becker, J.A. Golovchenko, D.R. Hamann and B.S. Swartzentruber, *Phys. Rev. Lett., 55* (1985) 2032.
[8] R.M. Feenstra, W.A. Thompson and A.P. Fein, *Phys. Rev. Lett., 56* (1986) 608.
[9] R.J. Hamers, R.M. Tromp and J.E. Demuth, *Phys. Rev. Lett., 56* (1986) 1972.
[10] J.A. Stroscio, R.M. Feenstra and A.P. Fein, *Phys. Rev. Lett., 57* (1986) 2579.
[11] R.M. Tromp, R.J. Hamers and J.E. Demuth, *Phys. Rev. B, 34* (1986) 1388.
[12] R.J. Hamers, R.M. Tromp and J.E. Demuth, *Surf. Sci., 181* (1987) 346.
[13] C.R.K. Marrian (ed.), *Technology of Proximal Probe Lithography*, SPIE Optical Engineering Press, Bellingham, WA, 1993.

[14] P.K. Hansma and J. Tersoff, *J. Appl. Phys., 61* (1987) R1.
[15] P.K. Hansma, V.B. Elings, O. Marti and C.E. Bracker, *Science, 242* (1988) 209.
[16] Y. Kuk and P.J. Silverman, *Rev. Sci. Instrum., 60* (1989) 165.
[17] J.E. Griffith and G.P. Kochanski, *Annu. Rev. Mater. Sci., 20* (1990) 219.
[18] R.J. Behm, N. Garcia and H. Rohrer (eds.), *Scanning Tunneling Microscopy and Related Methods*, Kluwer Academic Publishers, Dordrecht, 1990.
[19] J.A. Stroscio and W.J. Kaiser (eds.), *Scanning Tunneling Microscopy*, Academic Press, Boston, 1993.
[20] D.A. Bonnell (ed.), *Scanning Tunneling Microscopy and Spectroscopy: Theory, Techniques, and Applications*, VCH Publishers, New York, 1993.
[21] R. Wiesendanger and H.-J. Güntherodt (eds.), *Scanning Tunneling Microscopy I*, Springer-Verlag, Berlin, 1992.
[22] R. Wiesendanger and H.-J. Güntherodt (eds.), *Scanning Tunneling Microscopy II*, Springer-Verlag, Berlin, 1992.
[23] R. Wiesendanger and H.-J. Güntherodt (eds.), *Scanning Tunneling Microscopy III*, Springer-Verlag, Berlin, 1993.
[24] C.J. Chen, *Introduction to Scanning Tunneling Microscopy*, Oxford University Press, New York, 1993.
[25] R. Wiesendanger, *Scanning Probe Microscopy and Spectroscopy: Methods and Applications*, Cambridge University Press, Cambridge, 1994.
[26] H.K. Wickramasinghe, *J. Vac. Sci. Technol. A, 8* (1990) 363.
[27] D. Sarid and V. Elings, *J. Vac. Sci. Technol. B, 9* (1991) 431.
[28] D. Sarid, *Scanning Force Microscopy with Applications to Electric, Magnetic, and Atomic Forces*, Oxford University Press, New York, 1991.
[29] J. Tersoff and D.R. Hamann, *Phys. Rev. Lett., 50* (1983) 1998.
[30] J. Tersoff and D.R. Hamann, *Phys. Rev. B, 31* (1985) 805.
[31] J. Bardeen, *Phys. Rev. Lett., 6* (1961) 57.
[32] J. Bono and R.H. Good, Jr, *Surf. Sci., 151* (1985) 543.
[33] J. Bono and R.H. Good, Jr, *Surf. Sci., 175* (1986) 415.
[34] R.M. Feenstra and J.A. Stroscio, *J. Vac. Sci. Technol. B, 5* (1987) 923.
[35] R.J. Hamers, *Annu. Rev. Phys. Chem., 40* (1989) 531.
[36] R.M. Feenstra, *Surf. Sci., 299/300* (1994) 965.
[37] J.A. Stroscio and R.M. Feenstra, in J.A. Stroscio and W.J. Kaiser (eds.), *Scanning Tunneling Microscopy*, Academic Press, San Diego, 1993, p. 95.
[38] R.M. Feenstra, J.A. Stroscio and A.P. Fein, *Surf. Sci., 181* (1987) 295.
[39] R.M. Feenstra, J.A. Stroscio, J. Tersoff and A.P. Fein, *Phys. Rev. Lett., 58* (1987) 1192.
[40] R.J. Hamers, Ph. Avouris and F. Bozso, *Phys. Rev. Lett., 59* (1987) 2071.
[41] A. Selloni, P. Carnevali, E. Tosatti and C.D. Chen, *Phys. Rev. B, 31* (1985) 2602.
[42] N.D. Lang, *Phys. Rev. B, 34* (1986) 5947.
[43] P. Mårtensson and R.M. Feenstra, *Phys. Rev. B, 39* (1989) 7744.
[44] R.M. Feenstra, *Phys. Rev. B, 50* (1995) 4561.
[45] J.A. Stroscio, R.M. Feenstra and A.P. Fein, *J. Vac. Sci. Technol. A, 5* (1987) 838.
[46] J.A. Stroscio, R.M. Feenstra, D.M. Newns and A.P. Fein, *J. Vac. Sci. Technol. A, 6* (1988) 499.
[47] D.W. Pohl, *IBM J. Res. Dev., 30* (1986) 417.
[48] M. Okano, K. Kajimura, S. Wakiyama, F. Sakai, W. Mizutani and M. Ono, *J. Vac. Sci. Technol. A, 5* (1987) 3313.
[49] S.I. Park and C.F. Quate, *Rev. Sci. Instrum., 58* (1987) 2004.
[50] T. Tiedje and A. Brown, *J. Appl. Phys., 68* (1990) 649.
[51] G. Binnig and D.P.E. Smith, *Rev. Sci. Instrum., 57* (1986) 1688.
[52] J.E. Demuth, R.J. Hamers, R.M. Tromp and M.E. Welland, *IBM J. Res. Dev., 30* (1986) 396.
[53] D.P.E. Smith and G. Binnig, *Rev. Sci. Instrum., 57* (1986) 2630.
[54] D.W. Pohl, *Rev. Sci. Instrum., 58* (1986) 54.
[55] D.W. Pohl, *Surf. Sci., 181* (1987) 174.
[56] Burleigh Instruments Inc., Burleigh Park, Fishers, NY 14453.
[57] I.H. Musselman and P.E. Russell, *J. Vac. Sci. Technol. A, 8* (1990) 3558.
[58] J.P. Ibe, P.P. Bey, Jr, S.L. Brandow, R.A. Brizzolara, N.A. Burnham, D.P. DiLella, K.P. Lee, C.R.K. Marrian and R.J. Colton, *J. Vac. Sci. Technol. A, 8* (1990) 3570.
[59] A.J. Melmed, *J. Vac. Sci. Technol. B, 9* (1991) 601.
[60] B. El-Kareh, *J. Vac. Sci. Technol. B, 12* (1994) 172.
[61] H. Salemink and O. Albrektsen, *Microelectron. Eng., 15* (1991) 101.
[62] H. Salemink and O. Albrektsen, *J. Vac. Sci. Technol. B, 9* (1991) 779.
[63] J.M. Gomez-Rodriguez, A.M. Baro, J.P. Silveira, M. Vazquez, Y. Gonzalez and F. Briones, *Appl. Phys. Lett., 56* (1990) 36.
[64] W.J. Kaiser and L.D. Bell, *Phys. Rev. Lett., 60* (1988) 1406.
[65] L.D. Bell and W.J. Kaiser, *Phys. Rev. Lett., 61* (1988) 236.
[66] L.D. Bell, W.J. Kaiser, M.H. Hecht and L.C. Davis, in J.A. Stroscio and W.J. Kaiser (eds.), *Scanning Tunneling Microscopy*, Academic Press, San Diego, 1993, p. 307.
[67] M. Prietsch and R. Ludeke, *Phys. Rev. Lett., 66* (1991) 2511.

[68] R. Ludeke and M. Prietsch, *J. Vac. Sci. Technol. A, 9* (1991) 885.
[69] M.H. Hecht, L.D. Bell, W.J. Kaiser and L.C. Davis, *Phys. Rev. B, 42* (1990) 7663.
[70] R. Ludeke, M. Prietsch and A. Samsavar, *J. Vac. Sci. Technol. B, 9* (1991) 2342.
[71] J. Israelachvili, *Intermolecular and Surface Forces*, Second Edition, Academic Press, San Diego, 1992, p. 113.
[72] Y. Martin, C.C. Williams and H.K. Wickramasinghe, *J. Appl. Phys., 61* (1987) 4723.
[73] O. Marti, B. Drake and P.K. Hansma, *Appl. Phys. Lett., 51* (1987) 484.
[74] T.R. Albrecht and C.F. Quate, *J. Appl. Phys., 62* (1987) 2599.
[75] H. Heinzelmann, P. Grütter, E. Meyer, H. Hidber, L. Rosenthaler, M. Ringger and H.-J. Güntherodt, *Surf. Sci., 189–190* (1987) 29.
[76] Y. Sugawara, T. Ishizaka, S. Morita, S. Imai and N. Mikoshiba, *Jpn. J. Appl. Phys., 29* (1990) L296.
[77] P.J. Bryant, R.G. Miller and R. Yang, *Appl. Phys. Lett., 52* (1988) 2233.
[78] N.A. Burnham and R.J. Colton, *J. Vac. Sci. Technol. A, 7* (1989) 2906.
[79] T. Goddenreich, H. Lemke, U. Hartmann and C. Heiden, *J. Vac. Sci. Technol. A, 8* (1990) 383.
[80] G. Newbauer, S.R. Cohen, G.M. McClelland, D.E. Horn and C.M. Mate, *Rev. Sci. Instrum., 61* (1990) 2296.
[81] C.M. Mate, G.M. McClelland, R. Erlandsson and S. Chiang, *Phys. Rev. Lett., 59* (1987) 1942.
[82] R. Erlandsson, G.M. McClelland, C.M. Mate and S. Chiang, *J. Vac. Sci. Technol. A, 6* (1988) 266.
[83] D. Sarid, D. Iams, V. Weissenberger and L.S. Bell, *Opt. Lett., 13* (1988) 1057.
[84] C. Schönenberger and S.F. Alvarado, *Rev. Sci. Instrum., 60* (1989) 3131.
[85] G. Meyer and N.M. Amer, *Appl. Phys. Lett., 53* (1988) 1045.
[86] S. Alexander, L. Hellemans, O. Marti, J. Schneir, V. Elings, P.K. Hansma, M. Longmire and J. Gurley, *J. Appl. Phys., 65* (1989) 164.
[87] Y. Martin, D.W. Abraham and H.K. Wickramasinghe, *Appl. Phys. Lett., 52* (1988) 1103.
[88] B.D. Terris, J.E. Stern, D. Rugar and H.J. Mamin, *Phys. Rev. Lett., 63* (1989) 2669.
[89] J.E. Stern, B.D. Terris, H.J. Mamin and D. Rugar, *Appl. Phys. Lett., 53* (1988) 2717.
[90] B.D. Terris, J.E. Stern, D. Rugar and H.J. Mamin, *J. Vac. Sci. Technol. A, 8* (1990) 374.
[91] C. Schönenberger and S.F. Alvarado, *Phys. Rev. Lett., 65* (1990) 3162.
[92] Y. Martin, D.W. Abraham and H.K. Wickramasinghe, *Appl. Phys. Lett., 52* (1988) 1103.
[93] D.W. Abraham, C. Williams, J. Slinkman and H.K. Wickramasinghe, *J. Vac. Sci. Technol. B, 9* (1991) 703.
[94] Y. Martin and H.K. Wickramasinghe, *Appl. Phys. Lett., 50* (1987) 1455.
[95] J.J. Saenz, N. Garcia, P. Grütter, E. Meyer, H. Heinzelmann, R. Wiesendanger, L. Rosenthaler, H.R. Hidber and H.-J. Güntherodt, *J. Appl. Phys., 62* (1987) 4293.
[96] P. Grütter, H.J. Mamin and D. Rugar, in R. Wiesendanger and H.-J. Güntherodt (eds.), *Scanning Tunneling Microscopy II*, Springer-Verlag, Berlin, 1992, p. 151, and references therein.
[97] Ch. Schönenberger and S.F. Alvarado, *Z. Phys. B, 80* (1990) 373.
[98] P. Grütter, D. Rugar and H.J. Mamin, *Ultramicroscopy, 47* (1992) 393.
[99] P. Grütter, E. Meyer, H. Heinzelmann, L. Rosenthaler, H.-R. Hidber and H.-J. Güntherodt, *J. Vac. Sci. Technol. A, 6* (1988) 279.
[100] P.C.D. Hobbs, D.W. Abraham and H.K. Wickramasinghe, *Appl. Phys. Lett., 55* (1989) 2357.
[101] H.J. Mamin, D. Rugar, J.E. Stern, B.D. Terris and S.E. Lambert, *Appl. Phys. Lett., 53* (1988) 1563.
[102] D.W. Abraham, C.C. Williams and H.K. Wickramasinghe, *Appl. Phys. Lett., 53* (1988) 1446.
[103] D. Rugar, H.J. Mamin, P. Guenther, S.E. Lambert, J.E. Stern, I. McFadyen and T. Yogi, *J. Appl. Phys., 68* (1990) 1169.
[104] Y. Martin, D. Rugar and H.K. Wickramasinghe, *Appl. Phys. Lett., 52* (1988) 44.
[105] H.W. van Kesteren, A.J. den Boef, W.B. Zeper, J.H.M. Spruit, B.A.J. Jacobs and P.F. Carcia, *J. Appl. Phys., 70* (1991) 2413.
[106] D.W. Pohl, W. Denk and M. Lanz, *Appl. Phys. Lett., 44* (1984) 651.
[107] A. Lewis, M. Isaacson, A. Harootunian and A. Muray, *Ultramicroscopy, 13* (1984) 227.
[108] G.A. Massey, *Appl. Opt., 23* (1984) 658.
[109] U.Ch. Fischer, *J. Vac. Sci. Technol. B, 3* (1985) 386.
[110] U. Dürig, D.W. Pohl and F. Rohner, *J. Appl. Phys., 59* (1986) 3318.
[111] D.W. Pohl, U.Ch. Fischer and U.T. Dürig, *Proc. SPIE, 897* (1988) 84.
[112] E. Betzig, M. Isaacson, H. Barshatzky, A. Lewis and K. Lin, *Proc. SPIE, 897* (1988) 91.
[113] M. Isaacson, J.A. Cline and H. Barshatzky, *J. Vac. Sci. Technol. B, 9* (1991) 3103.
[114] U. Ch. Fischer, U.T. Dürig and D.W. Pohl, *Appl. Phys. Lett., 52* (1988) 249.
[115] D.W. Pohl, in R. Wiesendanger and H.-J. Güntherodt (eds.), *Scanning Tunneling Microscopy II,* Springer-Verlag, Berlin, 1992, p. 233.
[116] E. Betzig, J.K. Trautman, T.D. Harris, J.S. Wiener and R.L. Kostelak, *Science, 251* (1991) 1468.
[117] F. Zenhausern, M.P. O'Boyle and H.K. Wickramasinghe, *Appl. Phys. Lett., 65* (1994) 1623.
[118] M.D. Pashley, K.W. Haberern, W. Friday, J.M. Woodall and P.D. Kirchner, *Phys. Rev. Lett., 60* (1988) 2176.
[119] D.J. Chadi, *J. Vac. Sci. Technol. A, 5* (1987) 834.
[120] D.K. Biegelsen, R.D. Bringnans, J.E. Northrup and L.E. Swartz, *Phys. Rev. B, 41* (1992) 5701.
[121] M.D. Pashley, K.W. Haberern and R.M. Feenstra, *J. Vac. Sci. Technol. B, 10* (1992) 1874.
[122] M.D. Pashley and K.W. Haberern, *Ultramicroscopy, 42–44* (1992) 1281.
[123] M.D. Pashley, K.W. Haberern and J.M. Gaines, *Appl. Phys. Lett., 58* (1991) 406.
[124] J. Sudijono, M.D. Johnson, C.W. Snyder, M.B. Elowitz and B.G. Orr, *Phys. Rev. Lett., 69* (1992) 2811.

[125] J. Sudijono, M.D. Johnson, M.B. Elowitz, C.W. Snyder and B.G. Orr, *Surf. Sci., 280* (1993) 247.
[126] E.J. Heller and M.G. Lagally, *Appl. Phys. Lett., 60* (1992) 2675.
[127] K. Pond, R. Maboudian, V. Bressler-Hill, D. Leonard, X.-S. Wang, K. Self, W.H. Weinberg and P.M. Petroff, *J. Vac. Sci. Technol. B, 11* (1993) 1374.
[128] M. Tanimoto, J. Osaka, T. Takigami, S. Hirono and K. Kanisawa, *Ultramicroscopy, 42* (1992) 1275.
[129] C.W. Snyder, D. Barlett, B.G. Orr, P.K. Bhattacharya and J. Singh, *J. Vac. Sci. Technol. B, 9* (1991) 2189.
[130] S. Ohkouchi, I. Tanaka and N. Ikoma, *Jpn. J. Appl. Phys., 33* (1994) 1489.
[131] G.W. Smith, A.J. Pidduck, C.R. Whitehouse, J.L. Glasper and J. Spowart, *J. Cryst. Growth, 127* (1993) 966.
[132] C. Orme, M.D. Johnson, J.L. Sudijono, K.T. Leung and B.G. Orr, *Appl. Phys. Lett., 64* (1994) 860.
[133] J. van Laar, A. Huijser and T.L. van Rooy, *J. Vac. Sci. Technol., 14* (1977) 894.
[134] F. Bechstedt and R. Enderlein, *Semiconductor Surfaces and Interfaces*, Academie-Verlag, Berlin, 1988, Chapter 3.
[135] W. Gudat and D.E. Eastman, *J. Vac. Sci. Technol., 13* (1976) 831.
[136] D. Norman, I.T. McGovern and C. Norris, *Phys. Lett. A, 63* (1977) 384.
[137] D. Straub, M. Skibowski and F.J. Himpsel, *J. Vac. Sci. Technol. A, 3* (1985) 1484.
[138] P. Muralt, *Appl. Phys. Lett., 49* (1986) 1441.
[139] P. Muralt, H. Meier, D.W. Pohl and H.W.M. Salemink, *Appl. Phys. Lett., 50* (1987) 1352.
[140] P. Muralt and D.W. Pohl, *Appl. Phys. Lett., 48* (1986) 514.
[141] H.W.M. Salemink, H.P. Meier, R. Ellialtioglu, J.W. Gerritsen and P.R.M. Muralt, *Appl. Phys. Lett., 54* (1989) 1112.
[142] O. Albrektsen, D.J. Arent, H.P. Meier and H.W.M. Salemink, *Appl. Phys. Lett., 57* (1990) 31.
[143] H.W.M. Salemink, O. Albrektsen and P. Koenraad, *Phys. Rev. B, 45* (1992) 6946.
[144] H.W.M. Salemink and O. Albrektsen, *J. Vac. Sci. Technol. B, 10* (1992) 1799.
[145] O. Albrektsen, H.P. Meier, D.J. Arent and H.W.M. Salemink, *Appl. Phys. Lett., 62* (1993) 2105.
[146] R.M. Feenstra, E.T. Yu, J.M. Woodall, P.D. Kirchner, C.L. Lin and G.D. Pettit, *Appl. Phys. Lett., 61* (1992) 795.
[147] S. Gwo, A.R. Smith, C.K. Shih, K. Sadra and B.G. Streetman, *Appl. Phys. Lett., 61* (1992) 1104.
[148] T. Pinnington, S.N. Patitsas, C. Lavoie, A. Sanderson and T. Tiedje, *J. Vac. Sci. Technol. B, 11* (1993) 908.
[149] J.M. Gomez-Rodriguez, A.M. Baro, J.P. Silveira, M. Vazquez, Y. Gonzalez and F. Briones, *Appl. Phys. Lett., 56* (1990) 36.
[150] I. Tanaka, T. Kato, S. Ohkouchi and F. Osaka, *J. Vac. Sci. Technol. A, 8* (1990) 567.
[151] S. Gwo, K.J. Chao, C.K. Shih, K. Sadra and B.G. Streetman, *Phys. Rev. Lett., 71* (1993) 1883.
[152] F. Osaka, I. Tanaka, T. Kato and Y. Katayama, *Jpn. J. Appl. Phys., 27* (1988) L1193.
[153] T. Kato, F. Osaka and I. Tanaka, *Jpn. J. Appl. Phys., 28* (1989) 1050.
[154] F. Osaka and T. Kato, *J. Vac. Sci. Technol. B, 11* (1993) 1697.
[155] S.L. Skala, W. Wu, J.R. Tucker, J.W. Lyding, A. Seabaugh, E.A. Beam III and D. Jovanovic, *J. Vac. Sci. Technol. B, 13* (1995) 660.
[156] W. Wu, S.L. Skala, J.R. Tucker, J.W. Lyding, A. Seabaugh, E.A. Beam III and D. Jovanovic, *J. Vac. Sci. Technol. A, 13* (1995) 602.
[157] A.Y. Lew, C.H. Yan, R.B. Welstand, J.T. Zhu, C.W. Tu, E.T. Yu and P.K.L. Yu, *J. Elec. Mater.*, (1996) (in press).
[158] J.F. Zheng, J.D. Walker, M.B. Salmeron and E.R. Weber, *Phys. Rev. Lett., 72* (1994) 2414; J.F. Zheng, J.D. Walker, M.B. Salmeron and E.R. Weber, *Phys. Rev. Lett., 73* (1994) 368.
[159] M. Pfister, M.B. Johnson, S.F. Alvarado, H.W.M. Salemink, U. Marti, D. Martin, F. Morier-Genoud and F.K. Reinhart, *Appl. Phys. Lett., 67* (1995) 1459.
[160] R.M. Feenstra, D.A. Collins, D.Z.-Y. Ting, M.W. Wang and T.C. McGill, *Phys. Rev. Lett., 72* (1994) 2749.
[161] R.M. Feenstra, D.A. Collins, D.Z.-Y. Ting, M.W. Wang and T.C. McGill, *J. Vac. Sci. Technol. B, 12* (1994) 2592.
[162] R.M. Feenstra, D.A. Collins and T.C. McGill, *Superlattices and Microstructures, 15* (1994) 215.
[163] A.Y. Lew, E.T. Yu, D.H. Chow and R.H. Miles, *Appl. Phys. Lett., 65* (1994) 201.
[164] A.Y. Lew, E.T. Yu, D.H. Chow and R.H. Miles, *Mat. Res. Soc. Symp. Proc., 340* (1994) 237.
[165] Y.-H. Zhang and D.H. Chow, *Appl. Phys. Lett., 65* (1994) 3239.
[166] Y.-H. Zhang, *Appl. Phys. Lett., 66* (1995) 118.
[167] F. Reinhardt, B. Dwir and E. Kapon, *Appl. Phys. Lett., 68* (1996) 3168.
[168] H. Salemink and O. Albrektsen, *Microelectronic Engineering, 15* (1991) 101.
[169] J.M. Vandenberg, M.B. Panish, H. Temkin and R.A. Hamm, *Appl. Phys. Lett., 53* (1988) 1920.
[170] J.C.P. Chang, T.P. Chin, K.L. Kavanagh and C.W. Tu, *Appl. Phys. Lett., 58* (1991) 1530.
[171] A. Ourmazd, W.T. Tsang, J.A. Rentschler and D.W. Taylor, *Appl. Phys. Lett., 50* (1987) 1417.
[172] A. Ourmazd, D.W. Taylor, J. Cunningham and C.W. Tu, *Phys. Rev. Lett., 62* (1989) 933.
[173] A. Ourmazd, F.H. Baumann, M. Bode and Y. Kim, *Ultramicroscopy, 34* (1990) 237.
[174] O. Albrektsen, D.J. Arent, H.P. Meier and H.W. Salemink, *Appl. Phys. Lett., 57* (1990) 31.
[175] H.W.M. Salemink and O. Albrektsen, *J. Vac. Sci. Technol. B, 10* (1992) 1799.
[176] M.B. Johnson, U. Maier, H.-P. Meier and H.W.M. Salemink, *Appl. Phys. Lett., 63* (1993) 1273.
[177] H.W.M. Salemink and O. Albrektsen, *Phys. Rev. B, 47* (1993) 16044.
[178] G. Tuttle, H. Kroemer and J.H. English, *J. Appl. Phys., 67* (1990) 3032.
[179] B. Brar, J. Ibbetson, H. Kroemer and J.H. English, *Appl. Phys. Lett., 64* (1994) 3392.
[180] D.H. Chow, R.H. Miles and A.T. Hunter, *J. Vac. Sci. Technol. B, 10* (1992) 888.
[181] A.Y. Lew, S.L. Zuo, E.T. Yu and R.H. Miles, *Electronic Materials Conference*, Santa Barbara, CA (1996).
[182] A.Y. Lew, C.H. Yan, C.W. Tu and E.T. Yu, *Appl. Phys. Lett., 67* (1995) 932.

[183] S. Gwo, K.J. Chao, C.K. Shih, K. Sadra and B.G. Streetman, *Phys. Rev. Lett., 71* (1993) 1883.
[184] R.M. Feenstra, A. Vaterlaus, E.T.Yu, P.D. Kirchner, C.L. Lin, J.M. Woodall, and G.D. Pettit, in H.W.M. Salemink and M.D. Pashley (eds.), *Semiconductor Interfaces at the Sub-nanometer Scale*, Kluwer Academic Publishers, Dordrecht, 1993, p. 127.
[185] A. Vaterlaus, R.M. Feenstra, P.D. Kirchner, J.M. Woodall and G.D. Pettit, *J. Vac. Sci. Technol. B, 11* (1993) 1502.
[186] W.F. Tseng, J.A. Dagata, R.M. Silver, J. Fu and J.R. Lowney, *J. Vac. Sci. Technol. B, 12* (1994) 373.
[187] M.B. Johnson, O. Albrektsen, R.M. Feenstra and H.W.M. Salemink, *Appl. Phys. Lett., 63* (1993) 2923.
[188] M.B. Johnson, O. Albrektsen, R.M. Feenstra and H.W. Salemink, *Appl. Phys. Lett., 64* (1994) 1454.
[189] M.B. Johnson, H.P. Meier and H.W.M. Salemink, *Appl. Phys. Lett., 63* (1993) 3636.
[190] J.F. Zheng, X. Liu, E.R. Weber, D.F. Ogletree and M. Salmeron, *J. Vac. Sci. Technol. B, 12* (1994) 2104.
[191] Z.F. Zheng, M.B. Salmeron and E.R. Weber, *Appl. Phys. Lett., 64* (1994) 1836.
[192] R.M. Feenstra, J.M. Woodall and G.D. Pettit, *Phys. Rev. Lett., 71* (1993) 1176.
[193] R.M. Feenstra, A. Vaterlaus, J.M. Woodall and G.D. Pettit, *Appl. Phys. Lett., 63* (1993) 2528.
[194] H. Sakaki, M. Tanaka and J. Yoshino, *Jpn. J. Appl. Phys., 24* (1985) L417.
[195] D.L. Abraham, A. Veider, Ch. Schönenberger, H.P. Meier, D.J. Arent and S.F. Alvarado, *Appl. Phys. Lett., 56* (1990) 1564.
[196] S.F. Alvarado, Ph. Renaud, D.L. Abraham, Ch. Schönenberger, D.J. Arent and H.P. Meier, *J. Vac. Sci. Technol. B, 9* (1991) 409.
[197] Ph. Renaud and S.F. Alvarado, *Phys. Rev. B, 44* (1991) 6340.
[198] R.D. Grober, T.D. Harris, J.K. Trautman, E. Betzig, W. Wegscheider, L. Pfeiffer and K. West, *Appl. Phys. Lett., 64* (1994) 1421.
[199] H.F. Hess, E. Betzig, T.D. Harris, L.N. Pfeiffer and K.W. West, *Science, 264* (1994) 1740.
[200] J.W.P. Hsu, E.A. Fitzgerald, Y.H. Xie and P.J. Silverman, *Appl. Phys. Lett., 65* (1994) 344.
[201] M.A. Lutz, R.M. Feenstra and J.O. Chu, *Surf. Sci., 328* (1995) 215.
[202] Y.W. Mo, B.S. Swartzentruber, R. Kariotis, M.B. Webb and M.G. Lagally, *Phys. Rev. Lett., 63* (1989) 2393.
[203] Y.W. Mo and M.G. Lagally, *J. Cryst. Growth, 111* (1991) 876.
[204] R.J. Hamers, U.K. Köhler and J.E. Demuth, *Ultramicroscopy, 31* (1989) 10.
[205] R.J. Hamers, U.K. Köhler and J.E. Demuth, *J. Vac. Sci. Technol. A, 8* (1990) 195.
[206] A.J. Hoeven, J.M. Lenssinck, D. Dijkkamp, E.J. van Loenen and J. Dieleman, *Phys. Rev. Lett., 63* (1989) 1830.
[207] A.J. Hoeven, D. Dijkkamp, E.J. van Loenen, J.M. Lenssinck and J. Dieleman, *J. Vac. Sci. Technol. A, 8* (1990) 207.
[208] M.G. Lagally, R. Kariotis, B.S. Swartzentruber and Y.-W. Mo, *Ultramicroscopy, 31* (1989) 87.
[209] Y.-W. Mo, R. Kariotis, B.S. Swartzentruber, M.B. Webb and M.G. Lagally, *J. Vac. Sci. Technol. A, 8* (1990) 201.
[210] Y.W. Mo and M.G. Lagally, *Mater. Sci. Eng. B, 14* (1992) 311.
[211] M.G. Lagally, *Jpn. J. Appl. Phys., 32* (1993) 1493.
[212] F. Wu, S.G. Jaloviar, D.E. Savage and M.G. Lagally, *Phys. Rev. Lett., 71* (1993) 4190.
[213] J.J. Boland, *Phys. Rev. B, 44* (1991) 1383.
[214] D.-S. Lin, E.S. Hirschorn, T.-C. Chiang, R. Tsu, D. Lubben and J.E. Greene, *Phys. Rev. B, 45* (1992) 3494.
[215] R.M. Tromp, R.J. Hamers and J.E. Demuth, *Phys. Rev. Lett., 55* (1985) 1303.
[216] R.J. Hamers, R.M. Tromp and J.E. Demuth, *Phys. Rev. B, 34* (1986) 5343.
[217] D.J. Chadi, *Phys. Rev. Lett., 59* (1987) 1691.
[218] S. Stoyanov, *J. Cryst. Growth, 94* (1989) 751.
[219] Y.W. Mo and M.G. Lagally, *Surf. Sci., 248* (1991) 313.
[220] Y.-W. Mo, D.E. Savage, B.S. Swartzentruber and M.G. Lagally, *Phys. Rev. Lett., 65* (1990) 1020.
[221] A.J. Pidduck, D.J. Robbins, A.G. Cullis, W.Y. Leong and A.M. Pitt, *Thin Solid Films, 222* (1992) 78.
[222] M.A. Lutz, R.M. Feenstra, P.M. Mooney, J. Tersoff and J.O. Chu, *Surf. Sci., 316* (1994) L1075.
[223] J.W.P. Hsu, E.A. Fitzgerald, Y.H. Xie, P.J. Silverman and M.J. Cardillo, *Appl. Phys. Lett., 61* (1992) 1293.
[224] M.A. Lutz, R.M. Feenstra, F.K. LeGoues, P.M. Mooney and J.O. Chu, *Appl. Phys. Lett, 66* (1995) 724; M.A. Lutz, R.M. Feenstra, F.K. LeGoues, P.M. Mooney and J.O. Chu, *Appl. Phys. Lett., 67* (1995) 724.
[225] S.Y. Shiryaev, F. Jensen and J.W. Petersen, *Appl. Phys. Lett., 64* (1994) 3305.
[226] B.S. Meyerson, *Appl. Phys. Lett., 48* (1986) 797.
[227] D.L. Harame, J.M.C. Stork, B.S. Meyerson, T.N. Nguyen and G.J. Scilla, *IEEE Electron Device Lett., 10* (1989) 156.
[228] D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabbe, J.Y.-C. Sun, B.S. Meyerson and T. Tice, *IEEE Trans. Electron Devices, 42* (1995) 455.
[229] J.J. Boland, *Phys. Rev. Lett., 65* (1990) 3325.
[230] J.J. Boland, *Surf. Sci., 261* (1992) 17.
[231] J.J. Boland, *J. Vac. Sci. Technol. A, 10* (1992) 2458.
[232] M.J. Bronikowski, Y.J. Wang, M.T. McEllistrem, D. Chen and R.J. Hamers, *Surf. Sci., 298* (1993) 50.
[233] Y.J. Wang, M.J. Bronikowski and R.J. Hamers, *Surf. Sci., 311* (1994) 64.
[234] Y.J. Wang, M.J. Bronikowski and R.J. Hamers, *J. Vac. Sci. Technol. A, 12* (1994) 2051.
[235] Y.J. Wang, X.X. Chen and R.J. Hamers, *Phys. Rev. B, 50* (1994) 4534.
[236] Y.J. Wang, M.J. Bronikowski and R.J. Hamers, *J. Phys. Chem., 98* (1994) 5966.
[237] M.B. Johnson and J.-M. Halbout, *J. Vac. Sci. Technol. B, 10* (1992) 508.
[238] E.T. Yu, M.B. Johnson and J.-M. Halbout, *Appl. Phys. Lett., 61* (1992) 201.
[239] E.T. Yu, J.-M. Halbout, A.R. Powell and S.S. Iyer, *Appl. Phys. Lett., 61* (1992) 3166.
[240] E.T. Yu, K. Barmak, P. Ronsheim, M.B. Johnson, P. McFarland and J.-M. Halbout, *J. Appl. Phys., 79* (1996) 2115.

[241] T. Pinnington, A. Sanderson, T. Tiedje, T.P. Pearsall, E. Kasper and H. Presting, *Thin Solid Films*, *222* (1992) 259.
[242] E.T. Yu, M.B. Johnson, A.R. Powell, J.-M. Halbout and S.S. Iyer, *J. Vac. Sci. Technol. B*, *11* (1993) 1149.
[243] J.L. Freeouf and J.M. Woodall, *Appl. Phys. Lett.*, *39* (1981) 727.
[244] A.E. Fowell, R.H. Williams, B.E. Richardson and T.-H. Shen, *Semicond. Sci. Technol.*, *5* (1990) 348.
[245] A.E. Fowell, R.H. Williams, B.E. Richardson, A.A. Cafolla, D.I. Westwood and D.A. Woolf, *J. Vac. Sci. Technol. B*, *9* (1991) 581.
[246] A.A. Talin, R.S. Williams, B.A. Morgan, K.M. Ring and K.L. Kavanagh, *Phys. Rev. B*, *49* (1994) 16474.
[247] A.A. Talin, R.S. Williams, B.A. Morgan, K.M. Ring and K.L. Kavanagh, *J. Vac. Sci. Technol. B*, *12* (1994) 2634.
[248] T.-H. Shen, M. Elliot, A.E. Fowell, A. Cafolla, B.E. Richardson, D. Westwood and R.H. Williams, *J. Vac. Sci. Technol. B*, *9* (1991) 2219.
[249] A.E. Fowell, A.A. Cafolla, B.E. Richardson, T.-H. Shen, M. Elliot, D.I. Westwood and R.H. Williams, *Appl. Surf. Sci.*, *56–58* (1992) 622.
[250] S.P. Kowalczyk, W.J. Schaffer, E.A. Kraut and R.W. Grant, *J. Vac. Sci. Technol.*, *20* (1982) 705.
[251] J. Tersoff, *Phys. Rev. Lett.*, *56* (1986) 2755.
[252] C.G. Van de Walle and R.M. Martin, *Phys. Rev. B*, *35* (1987) 8154.
[253] C.G. Van de Walle, *Phys. Rev. B*, *39* (1989) 1871.
[254] M. Cardona and N.E. Christensen, *Phys. Rev. B*, *35* (1987) 6182.
[255] J.J. O'Shea, T. Sajoto, S. Bhargava, D. Leonard, M.A. Chin and V. Narayanamurti, *J. Vac. Sci. Technol. B*, *12* (1994) 2625.
[256] E.T. Yu, J.O. McCaldin and T.C. McGill, *Solid State Phys.*, *46* (1992) 1.
[257] S. Hosaka, S. Hosoki, K. Takata, K. Horiuchi and N. Natsuaki, *Appl. Phys. Lett.*, *53* (1988) 487.
[258] H.E. Hessel, U. Memmert, H. Cerva and R.J. Behm, *J. Vac. Sci. Technol. B*, *9* (1991) 690.
[259] J.V. LaBrasca, R.C. Chapman, G.E. McGuire and R.J. Nemanich, *J. Vac. Sci. Technol. B*, *9* (1991) 752.
[260] T. Takigami and M. Tanimoto, *Appl. Phys. Lett.*, *58* (1991) 2288.
[261] V. Raineri, V. Privitera, W. Vandervorst, L. Hellemans and J. Snauwaert, *Appl. Phys. Lett.*, *64* (1994) 354.
[262] M. Barrett, M. Dennis, D. Tiffin, Y. Li and C.K. Shih, *IEEE Electron Device Lett.*, *16* (1995) 118.
[263] G. Neubauer, M. Lawrence, A. Dass and T.J. Johnson, *Mater. Res. Soc. Symp. Proc.*, *265* (1992) 283.
[264] S. Kordic, E.J. van Loenen, D. Dijkkamp, A.J. Hoeven and H.K. Moraal, *J. Vac. Sci. Technol. A*, *8* (1990) 549.
[265] S. Kordic, E.J. van Loenen and A.J. Walker, *Appl. Phys. Lett.*, *59* (1991) 3154.
[266] R. Chapman, M. Kellam, S. Goodwin-Johansson, J. Russ, G.E. McGuire and K. Kjoller, *J. Vac. Sci. Technol. B*, *10* (1991) 502.
[267] J.R. Matey and J. Blanc, *J. Appl. Phys.*, *47* (1985) 1437.
[268] C.C. Williams, J. Slinkman, W.P. Hough and H.K. Wickramasinghe, *Appl. Phys. Lett.*, *55* (1989) 1662.
[269] C.C. Williams, J. Slinkman, W.P. Hough and H.K. Wickramasinghe, *J. Vac. Sci. Technol. A*, *8* (1990) 895.
[270] C.C. Williams, W.P. Hough and S.A. Rishton, *Appl. Phys. Lett.*, *55* (1989) 203.
[271] Y. Huang, C.C. Williams and J. Slinkman, *Appl. Phys. Lett.*, *66* (1995) 344.
[272] Y. Huang, C.C. Williams and H. Smith, *J. Vac. Sci. Technol. B*, *14* (1996) 433.
[273] G. Neubauer, A. Erickson, C C. Williams, J.J. Kopanski, M. Rodgers and D. Adderton, *J. Vac. Sci. Technol. B*, *14* (1996) 426.
[274] D.W. Abraham, C. Williams, J. Slinkman and H.K. Wickramasinghe, *J. Vac. Sci. Technol. B*, *9* (1991) 703.
[275] B. Michel, W. Mizutani, R. Schierle, A. Jarosch, W. Knop, H. Benedikter, W. Bachtold and H. Rohrer, *Rev. Sci. Instrum.*, *63* (1992) 4080.
[276] J.-P. Bourgoin, M.B. Johnson and B. Michel, *Appl. Phys. Lett.*, *65* (1994) 2045.
[277] C. Shafai, D.J. Thomson, M. Simard-Normandin, G. Mattiussi and P.J. Scanlon, *Appl. Phys. Lett.*, *64* (1994) 342.
[278] C. Shafai, D.J. Thomson and M. Simard-Normandin, *J. Vac. Sci. Technol. B*, *12* (1994) 378.
[279] P. DeWolf, T. Clarysse, W. Vandervorst, J. Snauwaert and L. Hellemans, *J. Vac. Sci. Technol. B*, *14* (1996) 380.
[280] J.M.R. Weaver and H.K. Wickramasinghe, *J. Vac. Sci. Technol. B*, *9* (1991) 1562.
[281] M. Nonnenmacher, M.P. O'Boyle and H.K. Wickramasinghe, *Appl. Phys. Lett.*, *58* (1991) 2921.
[282] M. Nonnenmacher, M. O'Boyle and H.K. Wickramasinghe, *Ultramicroscopy*, *42–44* (1992) 268.
[283] A.K. Henning, T. Hochwitz, J. Slinkman, J. Never, S. Hoffman, P. Kaszuba and C. Daghlian, *J. Appl. Phys.*, *77* (1995) 1888.
[284] A. Kikukawa, S. Hosaka and R. Imura, *Appl. Phys. Lett.*, *66* (1995) 3510.
[285] T. Hochwitz, A.K. Henning, C. Levey, C. Daghlian, J. Slinkman, J. Never, P. Kaszuba, R. Gluck, R. Wells, J. Pekarik and R. Finch, *J. Vac. Sci. Technol. B*, *14* (1996) 440.
[286] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, H.S. Momose and H. Iwai, *J. Vac. Sci. Technol. B*, *13* (1995) 1740.
[287] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro and H. Iwai, *IEEE Trans. Electron Devices*, *42* (1995) 1822.
[288] C.A. Mead, *Analog Integrated Circuits and Signal Processing*, *6* (1994) 9.
[289] J.E. Griffith and D.A. Grigg, *J. Appl. Phys.*, *74* (1993) R83.
[290] J.E. Griffith, H.M. Marchman, G.L. Miller, L.C. Hopkins, M.J. Vasile and S.A. Schwalm, *J. Vac. Sci. Technol. B*, *11* (1993) 2473.
[291] Y. Martin and H.K. Wickramasinghe, *Appl. Phys. Lett.*, *64* (1994) 2498.
[292] Y. Martin and H.K. Wickramasinghe, *J. Vac. Sci. Technol. B*, *13* (1995) 2335.
[293] E.C. Teague, *J. Vac. Sci. Technol. B*, *7* (1989) 1898.
[294] R.C. Barrett and C.F. Quate, *Rev. Sci. Instrum.*, *62* (1991) 1393.
[295] J. Schneir, T.H. McWaid, J. Alexander and B.P. Wilfley, *J. Vac. Sci. Technol. B*, *12* (1994) 3561.
[296] P.K. Chu, R.G. Brigham and S.M. Baumann, *Mater. Chem. Phys.*, *41* (1995) 61.