Transport Coefficients of InAs Nanowires as a Function of Diameter**

Shadi A. Dayeh, Edward T. Yu, and Deli Wang**

InAs nanowires (NWs) have been the subject of intensive research recently in both synthesis[1–3] and transport[4–6] studies due to their potential for future high-speed nanoelectronic devices. Back-,[7] top-,[6,8] and wrap-gate[9] NW field-effect transistors (NWFETs) have been employed to study the low-field transport properties of InAs NWs at room temperature. Among these properties, the capacitive effects of interface states on FET characteristics and parameter extraction,[10] and the field-dependent transport properties in InAs NWs[11] have been explored by us recently in the top-gate geometry. Using conductive atomic force microscopy, the effects of channel-length scaling[12] and the transition from diffusive to ballistic carrier transport in InAs NWs has been identified.[13] On the other hand, systematic experimental characterization and detailed analysis of the effects of channel-width scaling and channel dimensionality on the transport properties in NWs are still lacking.

Herein, we present a comprehensive method to extract the transport coefficients in NWs as functions of their diameter and vertical (gate) and lateral (drain) fields, thus enabling consistent comparison due to their field dependence.[11] This extraction technique extends earlier studies on the variation of transport properties in NWs as functions of their diameter, which was attributed to either 1) only changes in carrier concentration (Si NWs)[14] or 2) only changes in carrier mobility (GaN NWs).[15] One-dimensional (1D) Schrödinger–Poisson self-consistent solutions for a material structure similar to that used in our experiments, but with different InAs thicknesses, was performed to validate our experimental observations and analysis.

Metal–organic chemical vapor deposition was utilized to grow the InAs NWs on thermally grown SiO_2/Si substrates with 40-nm-diameter Au nanoparticles on top, at a substrate temperature of 350 °C and a chamber pressure of 100 Torr. Trimethylindium and arsine precursors in H_2 carrier gas were used at an input V/III ratio of 50 and for growth times of 13, 20, and 30 min.[16] This results in n-type NWs[6] with lengths of ≈10 μm and diameters of ≈60–120 nm. Following growth, the InAs NWs were suspended in an ethanol solution and transferred to a thermally grown 600-nm SiO_2/n^+-Si substrate with a prepatterned grid for lithography alignment. Electron-beam (e-beam) lithography was then used to pattern source–drain electrodes with variable spacing followed by 15/85 nm Ti/Al deposited by e-beam evaporation and lift-off. This results in ohmic contacts with a contact resistance of ≈1 KΩ. A 73-nm ZrO_2–Y_2O_3 dielectric layer was then deposited, followed by e-beam lithography to define a ≈1-μm-wide gate. A 100-nm-thick Al top-gate metal was sputtered, which left extension regions with the source and drain electrodes as shown in the field-emission scanning electron microscopy (FESEM) image in the inset of Figure 1b.

In electrical measurements, we observe that, as expected, the current capacity of the NW decreases as the NW diameter decreases, as illustrated in Figure 1a, which shows the current–voltage (I–V) characteristics of a selected set of InAs NWs with different diameters taken at an applied gate voltage of $V^0_{GS} = 0$ V. The observed trends in the I–V characteristics as a function of diameter are valid for all V_{GS} values, and $V^0_{GS} = 0$ V is chosen for convenience. However, the measured current at a given value of applied source–drain bias V^0_{DS} depends on both the NW length L_{SD} and the NW cross-sectional area A. Variation of the transport coefficients as a function of NW diameter can be better evaluated through conductance, $\sigma = qn_{av}\mu_{FE} = L_{SD} \Big/ \lfloor A \mathrm{d}V^0_{DS}/\mathrm{d}I^0_{DS}|_{V^0_{GS}=0V} \rfloor$, calculated near $V^0_{DS} = 0$ V, where q is the fundamental charge constant, n_{av} is the average carrier concentration, and μ_{FE} is the effective mobility. Figure 1b shows a plot of conductance versus NW diameter calculated from the I–V curves of Figure 1a. It is evident that the conductance decreases as the NW diameter decreases. For a proper interpretation of the decrease in NW conductance with diameter, however, the effects of diameter reduction on n_{av} and μ_{FE} have to be isolated.

For the underlap top-gate geometry, one can assign a drain series resistance, R_{s1}, which accounts for the contact and gate-to-drain extension region resistances, and a source series resistance, R_{s2}, which accounts for the contact and gate-to-source extension region resistances. The presence of positively charged surface states[17] at the oxide/InAs interface decreases the gate field by Q_{int}/ε_{ox}, where Q_{int} is the interface charge density and ε_{ox} is the oxide dielectric constant, and prevents

[*] S. A. Dayeh,[†] Prof. E. T. Yu, Prof. D. Wang
Department of Electrical and Computer Engineering University of California–San Diego
La Jolla, CA 92093 (USA)
E-mail: ety@ece.ucsd.edu; dwang@ece.ucsd.edu

[†] Present address: Los Alamos National Laboratory PO Box 1663, K771 Los Alamos, NM 87545 (USA)

[**] We thank Prof. Paul K. L. Yu for giving us access to his MOCVD lab to grow the InAs nanowires. We also acknowledge the financial support from the Office of Naval Research (ONR–Nanoelectronics), National Science Foundation (ECS-0506902), and Sharp Labs of America and W. S. C. Chang's fellowship support for S.A.D.

DOI: 10.1002/smll.200800969

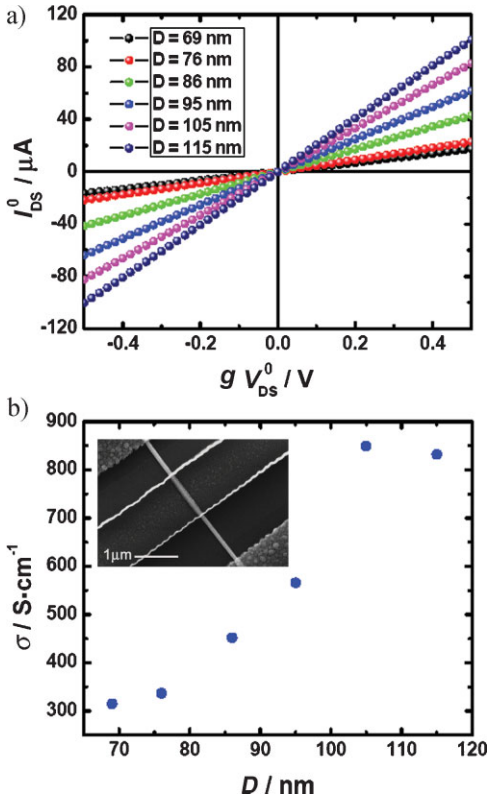

Figure 1. a) Current–voltage (*I–V*) characteristics of several InAs NWFETs with different diameters *D* at $V^0_{GS} = 0$ V. b) Corresponding conductance σ calculated near $V^0_{DS} = 0$ V. Inset: representative FESEM image of a top-gate InAs NWFET used in this study. GS = gate–source, DS = drain–source.

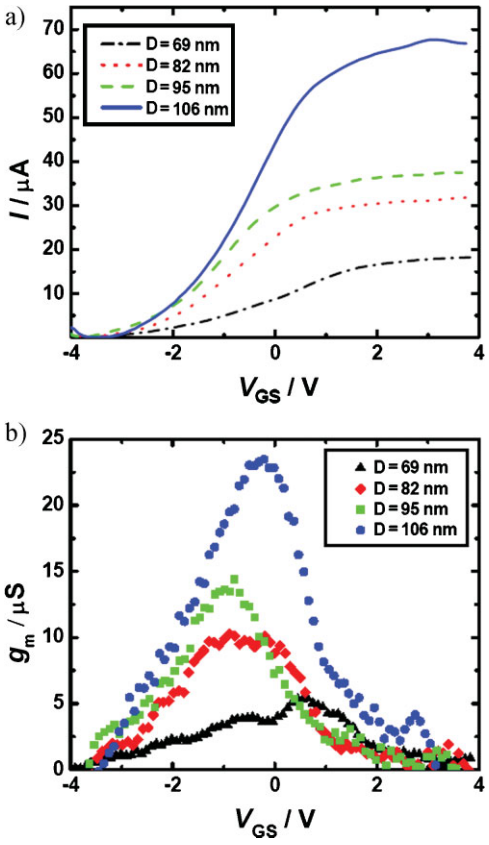

Figure 2. a) Extracted transfer curves for a set of InAs NWs with different diameters at $V^0_{DS} = 0.5$ V and b) their corresponding transconductance as function of gate voltage.

full depletion of the InAs NW channel. Thus, a leakage resistance, R_{leak}, associated with the lowest source–drain current I^0_{DS} through the channel at negative V^0_{GS}, is introduced. Simple circuit analysis can then be used to account for potential and current drops across these parasitic resistances to extract the intrinsic *I–V* characteristics of the active portion of the InAs NWFET according to Equations (1–3):[6]

$$V_{DS} = V^0_{DS} - I^0_{DS}(R_{s1} + R_{s2}) \quad (1)$$

$$I_{DS} = I^0_{DS}\left(1 + \frac{(R_{s1} + R_{s2})}{R_{leak}}\right) - \frac{V^0_{DS}}{R_{leak}} \quad (2)$$

$$V_{GS} = V^0_{GS} - I^0_{DS}R_{s2} \quad (3)$$

where V^0_{DS}, V^0_{GS}, and I^0_{DS} are the applied drain–source and gate–source voltages and the measured drain–source current, respectively, and V_{DS}, V_{GS}, and I_{DS} are the potential and current values at the terminals of the NWFET segment directly under the gate.

The field-effect mobility and the average carrier concentration are typically calculated from the transfer characteristics in the linear operating regime.[6–9] Figure 2a shows a set of intrinsic transfer curves extracted using Equations (1–3), which is then used to calculate the intrinsic transconductance $g_m = \partial I_{DS}/\partial V_{GS}|_{V_{DS}=cst}$ (cst = constant) plotted in Figure 2b. The intrinsic transconductance, which is linearly dependent on μ_{FE},[6] decreases as the NW diameter decreases. Moreover, the transconductance plot develops a plateau as the NW diameter is reduced. It is known that the surface Fermi energy in InAs is pinned in the conduction band,[18] which causes the formation of a surface accumulation layer.[19] The transconductance is thus expected to peak at flat-band voltages, V_{fb}, which are negative due to the presence of positively charged interface states, at which surface accumulation is eliminated.[20] In the depletion regime, at negative gate voltages relative to V_{fb}, coulomb scattering due to fixed oxide charges, interface-state charges, and ionized impurity charges reduces μ_{FE}.[21] Coulomb scattering is reduced in the accumulation regime, at positive gate voltages relative to V_{fb}, due to screening from accumulated electrons; however, surface scattering becomes dominant leading to reduced μ_{FE}.[22,23] As the NW diameter is reduced, surfacelike transport coefficients dominate the transport properties of the InAs NW due to carrier transport predominantly in a surfacelike region, and strong peaking in the transconductance is less likely to occur, which is clearly evident in Figure 2b. This is consistent with variation of transport properties for InAs epitaxial layers with different thicknesses, where the bulk contribution to the

mobility decreases as the thickness of the InAs layer decreases.[24]

For the NW lengths used in this study ($L_{SD} = 3$–$4\ \mu m$, $L_G \approx 1\ \mu m$) ballistic effects can be neglected, as the mean free path determined from scanned probe measurements[25] or estimated from the Fermi wave vector[10,13] is consistently smaller than L_G. From the I–V curves extracted from Equations (1)–(3) one can therefore compute μ_{FE} by using Equation (4):

$$\mu_{FE} = g_m L_G^2 / C V_{DS} \quad (4)$$

where C is the gate-to-channel capacitance and is equal to the oxide capacitance in the linear operating regime.[26] Note that Equation (4) does not account for the effects of interface states and the associated interface-state capacitance correction for C, which leads to an underestimation of μ_{FE}. Also, prior measurements have shown[27] that apparent mobility values are highly dependent on the V_{GS} sweep rate and direction that allow different interface-state dynamic charging and discharging, which leads to different C values. To minimize measurement artifacts, a fixed sweep rate of $\approx 20\ mV\ s^{-1}$ was used in measuring all 26 devices in this study.[10]

Figure 3a shows a plot of the average values of calculated μ_{FE} versus NW diameter computed from extracted I–V characteristics, and accounting for parasitic resistances of each device depending on its particular geometry for all 26 devices. From the extracted I–V characteristics, and for fair comparison between different NW diameters, μ_{FE} was calculated according to Equation (4) at constant $V_{GS} = 0\ V$ and constant $V_{DS} = 0.15\ V$. These values of V_{GS} and V_{DS} are used for consistency in comparison, and do not reflect the highest value of μ_{FE} that can be obtained in each NW. Specifically, it can be seen from Figure 2b that $V_{GS} = 0\ V$ does not necessarily result in the highest obtained transconductance, and consequently the highest μ_{FE}, in each device. The low V_{DS} value chosen here lies within the linear biasing regime where the μ_{FE} is constant and is the low-field mobility. It is evident from Figure 3a that μ_{FE} decreases as the NW diameter decreases, consistent with enhanced surface scattering in smaller-diameter NWs. This is also in agreement with recent mobility–diameter dependence studies in GaN NWs[15] obtained from back-gate geometry.

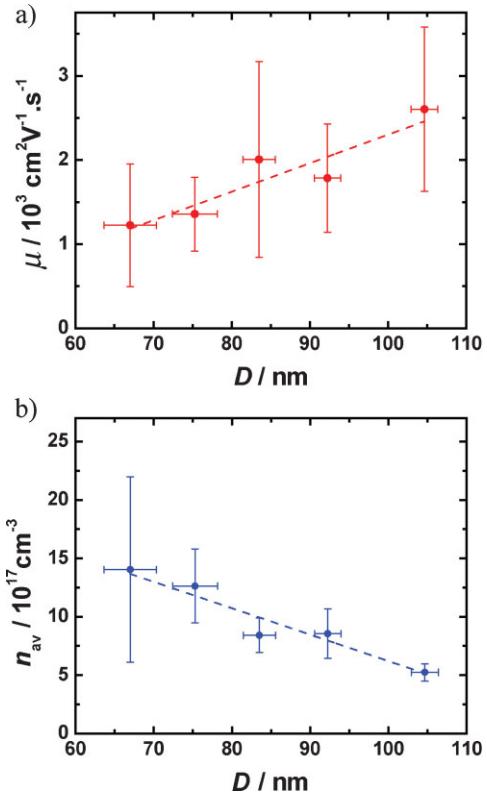

Figure 3. a) Measured field-effect mobility and b) measured average carrier density as functions of InAs NW diameter. Dashed lines are linear fits with statistical weighting for both sets of data.

Another important transport coefficient is the carrier concentration dependence on NW diameter, which can be computed, again at the same fields for fair comparison, according to Equation (5):

$$n_{av} = I_{DS} L_G / q \mu_{FE} V_{DS} A \quad (5)$$

Figure 3b shows a plot of computed n_{av} for different NW diameters, and indicates an increase in n_{av} as the NW diameter decreases. This is due to the presence of an accumulation layer at the InAs surface whose relative contribution to n_{av} increases as the NW diameter decreases. If the Fermi energy were pinned in the bandgap at the NW surface, reduction of n_{av} or p_{av} as the NW diameter decreases is expected (e.g., in Si NWs),[14] where p_{av} is the average hole concentration in a p-type NW. In InAs NWs, reduction of the interface states through proper surface passivation or formation of core–shell heterostructures may lead to unpinning of the Fermi energy in the conduction band and reduction of its detrimental effects on electron mobility.[28]

To validate the observed dependence of μ_{FE} and n_{av} on NW diameter, numerical simulation using Silvaco Atlas in 1D is carried out.[29] For the NW diameters used in this study and due to their cylindrical symmetry, 1D Schrödinger–Poisson solutions for electron wavefunctions, energy bands, and electron distribution in InAs slabs are close to the exact solutions in cylindrical coordinates.[30] A material stack similar to that used in the actual NWFET device was employed to perform the simulations. To account for the presence of surface states at the oxide/InAs interface, a fixed positive interface charge density of $2.7 \times 10^{12}\ cm^{-2}\ eV^{-1}$ [28,31] and a bulk carrier concentration of $5 \times 10^{16}\ cm^{-3}$ were used to match the simulated and the experimentally extracted values. Figure 4a shows the radial distribution of the first four electron wavefunctions in a 70-nm-thick InAs slab at $V_{GS} = 0\ V$. The positive surface potential due to the fixed interface charges pulls the electron wavefunction peaks toward the surface of the InAs slab. The first four subband energies and the energy band-edge profiles across the slab thickness are plotted in Figure 4b, which shows $\approx 270\ meV$ band bending at the slab surface due to the presence of interface charges. Figure 4b also shows a plot of the electron distribution across the slab thickness, and illustrates peaking in the electron distribution near the surface of the NW.

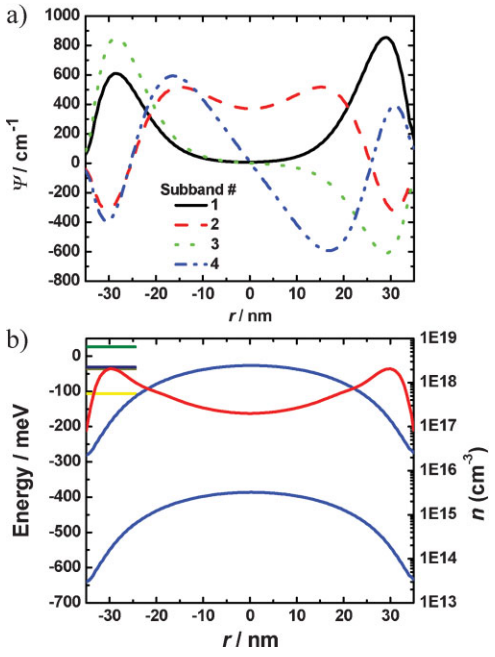

Figure 4. 1D Schrödinger–Poisson solution for a 70-nm-thick InAs slab in the presence of $Q_f/q = 2.7 \times 10^{12}\,cm^{-2}$ surface fixed charge density. a) Distribution of the first four subband wavefunctions across the slab thickness r. b) Energy-band diagram across the slab thickness showing strong surface Fermi energy pinning in the conduction band together with electron accumulation. The first few subband energies are shown to the top left.

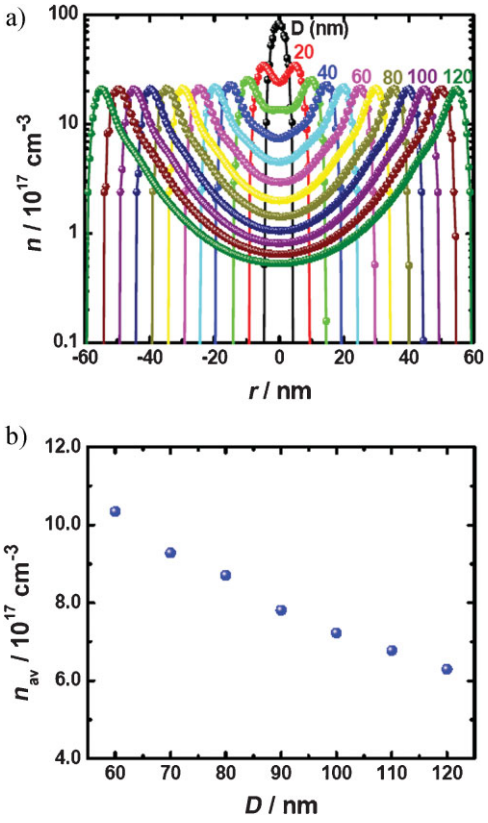

Figure 5. a) Free carrier distribution along the channel for different NW diameters obtained by the Schrödinger–Poisson solver in one dimension. b) Average NW carrier density obtained from (a) by integrating across the radial direction and dividing by the NW area.

Figure 5a shows the calculated electron concentration distribution for different InAs slab thicknesses with the same background doping and fixed charge density of $5 \times 10^{16}\,cm^{-3}$ and $2.7 \times 10^{12}\,cm^{-2}\,eV^{-1}$, respectively. The electron concentration peaks for thinner slabs are higher than those for thicker slabs, due to the dominance of accumulation electrons in thinner slabs. The average carrier concentration for a single NW diameter can be obtained by using Equation (6):

$$n_{av} = \frac{2\pi \int_0^R nr\,dr}{\pi R^2} \qquad (6)$$

Figure 5b shows a plot of the average carrier concentration for different NW diameters, which indicates an increase in the computed n_{av} as the NW diameter decreases. This trend is consistent with the experimentally extracted n_{av} from the InAs NWFETs. Smaller-diameter NWs are thus dominated by accumulated electrons that encounter enhanced surface scattering. The numerical simulations thus support the experimental observation of a μ_{FE} reduction and n_{av} increase with decreasing NW diameter.

In summary, we have discussed the diameter-dependent transport coefficients in InAs NWs at equal vertical and lateral fields and at equal V_{GS} sweep rates for consistent comparison. Smaller-diameter NWs were found to have lower μ_{FE} and higher n_{av} values due to the presence of an electron surface accumulation layer that increases the effect of surface scattering. For larger-diameter wires, bulklike transport properties lead to higher μ_{FE} and lower n_{av} values. Numerical simulations with a 1D Schrödinger–Poisson solver support the presence of the electron accumulation layer near the positive interface-state charges that lead to the observed trends in the transport coefficients of the InAs NWs. We believe that this comprehensive extraction technique of the NW transport properties as function of diameter enables fair and more accurate assessment of the transport properties of NWFETs.

Keywords:

arsenic · charge transport · indium · nanowires · transistors

[1] K. A. Dick, K. Deppert, T. Martensson, B. Mandl, L. Samuelson, W. Seifert, *Nano Lett.* **2005**, *5*, 761.
[2] H. D. Park, S. M. Prokes, R. C. Cammarata, *Appl. Phys. Lett.* **2005**, *87*, 063110.
[3] S. A. Dayeh, E. T. Yu, D. Wang, *Nano Lett.* **2007**, *7*, 2486.
[4] C. Thelander, M. T. Björk, M. W. Larsson, A. E. Hansen, L. R. Wallenberg, L. Samuelson, *Solid State Commun.* **2004**, *131*, 573.
[5] Y. J. Doh, J. A. van Dam, A. L. Roest, E. P. A. M. Bakkers, L. P. Kouwenhoven, S. De Franceschi, *Science* **2005**, *309*, 272.
[6] S. A. Dayeh, D. P. R. Aplin, X. Zhou, P. K. L. Yu, E. T. Yu, D. Wang, *Small* **2007**, *3*, 326.
[7] E. Lind, A. I. Persson, L. Samuelson, L.-E. Wernersson, *Nano Lett.* **2006**, *6*, 1842.

[8] Q.-T. Do, K. Blekker, I. Regolin, W. Prost, F. J. Teugude, *IEEE Electron Device Lett.* **2007**, *28*, 682.
[9] T. Bryllert, L.-E. Wernersson, L. E. Fröberg, L. Samuleson, *IEEE Electron Device Lett.* **2006**, *27*, 323.
[10] S. A. Dayeh, C. Scoi, P. K. L. Yu, E. T. Yu, D. Wang, *J. Vac. Sci. Technol. B* **2007**, *25*, 1432.
[11] S. A. Dayeh, E. T. Yu, D. Wang, *Nano Lett.* **2008**, *8*, 3114.
[12] X. Zhou, S. A. Dayeh, D. Wang, E. T. Yu, *J. Vac. Sci. Technol. B* **2007**, *25*, 1427.
[13] X. Zhou, S. A. Dayeh, D. Aplin, D. Wang, E. T. Yu, *J. Vac. Sci. Technol. B* **2006**, *24*, 2036.
[14] K.-I. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart, T. I. Kamins, *Electrochem. Solid State Lett.* **2006**, *9*, G69.
[15] A. Motayed, M. Vaudin, A. V. Davydov, J. Melngailis, M. He, S. N. Mohammad, *Appl. Phys. Lett.* **2007**, *90*, 043104.
[16] S. A. Dayeh, E. T. Yu, D. Wang, *J. Phys. Chem. C* **2007**, *111*, 13331.
[17] M. J. Lowe, T. D. Veal, C. F. McConville, G. R. Bell, S. Tsukamoto, N. Koguchi, *Surf. Sci.* **2003**, *523*, 179.
[18] C. A. Mead, W. G. Spitzer, *Phys. Rev. Lett.* **1963**, *10*, 471.
[19] M. Noguchi, K. Hirakawa, T. Ikoma, *Phys. Rev. Lett.* **1991**, *66*, 2243.
[20] H. H. Wieder, *Appl. Phys. Lett.* **1974**, *25*, 206.
[21] J. R. Brews, *J. Appl. Phys.* **1975**, *46*, 2193.
[22] S. C. Sun, J. D. Plummer, *IEEE Trans. Electron Devices* **1980**, *27*, 1497.
[23] K. Lee, J.-S. Choi, S.-P. Sim, C.-K. Kim, *IEEE Trans. Electron Devices* **1991**, *38*, 1905.
[24] C. Affentauschegg, H. H. Wieder, *Semicond. Sci. Technol.* **2001**, *16*, 708.
[25] X. Zhou, S. A. Dayeh, D. Aplin, D. Wang, E. T. Yu, *Appl. Phys. Lett.* **2006**, *89*, 053113.
[26] Y. Taur, T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, New York 1998.
[27] S. A. Dayeh, C. Soci, P. K. L. Yu, E. T. Yu, D. Wang, *Appl. Phys. Lett.* **2007**, *90*, 162112.
[28] X. Jiang, Q. Xiong, S. Nam, F. Qian, Y. Li, C. M. Lieber, *Nano Lett.* **2007**, *7*, 3214.
[29] http://www.silvaco.com/products/device_simulation/atlas.html.
[30] L. Wang, D. Wang, P. M. Asbeck, *Solid State Electron.* **2006**, *50*, 1732.
[31] E. Lind, A. I. Persson, L. Samuelson, L.-E. Wernerssson, *Nano Lett.* **2006**, *6*, 1842.

Received: July 8, 2008
Published online: November 28, 2008

