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A Low-Leakage Epitaxial High-κ Gate Oxide for Germanium Metal–Oxide–Semiconductor Devices

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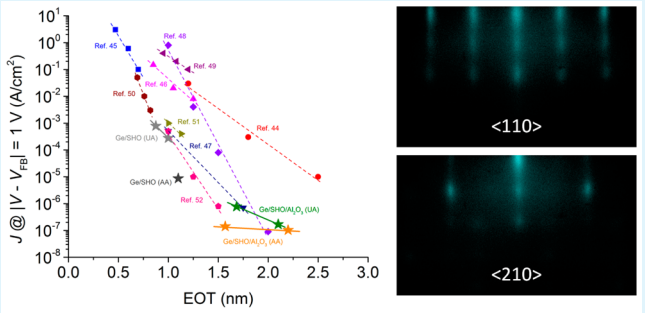
Supporting Information

ABSTRACT: Germanium (Ge)-based metal–oxide–semiconductor field-effect transistors are a promising candidate for high performance, low power electronics at the 7 nm technology node and beyond. However, the availability of high quality gate oxide/Ge interfaces that provide low leakage current density and equivalent oxide thickness (EOT), robust scalability, and acceptable interface state density (D_{it}) has emerged as one of the most challenging hurdles in the development of such devices. Here we demonstrate and present detailed electrical characterization of a high-κ epitaxial oxide gate stack based on crystalline $SrHfO_3$ grown on Ge (001) by atomic layer deposition. Metal–oxide–Ge capacitor structures show extremely low gate leakage, small and scalable EOT, and good and reducible D_{it}. Detailed growth strategies and postgrowth annealing schemes are demonstrated to reduce D_{it}. The physical mechanisms behind these phenomena are studied and suggest approaches for further reduction of D_{it}.



KEYWORDS: *epitaxial oxides, high-κ dielectrics, germanium, semiconductor–oxide interfaces, interface traps, perovskites*

INTRODUCTION

With recent advances in high-κ/metal-gate technology,[1] interest in germanium as a transistor channel material has resurged owing to its higher bulk electron and hole mobilities compared with those of silicon.[2−11] However, there remain several critical technical issues to be solved before Ge-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) can be integrated with mainstream Si complementary MOS technology.[2−11] An outstanding problem among these is the need for a high-quality and scalable gate dielectric on Ge. Unlike Si, the native oxide of Ge is thermally and chemically unstable and can readily decompose into several suboxides, potentially creating a high density of Ge dangling bonds and a high degree of surface roughness at the GeO_x/Ge interface that act as scattering sources.[2,4,5,8] These interfacial trap states, unfortunately, cannot be hydrogen passivated by using conventional forming gas anneals.[8]

Over the past few years, several approaches have proved successful to reduce interface trap density (D_{it}) of Ge-based MOSFETs. The first employs a thin epitaxial Si passivation layer deposited on the Ge surface, which is then partially oxidized to form a tensile-strained Si/SiO_2 interfacial layer (IL).[2,4] In such a way, the problem of Ge passivation is converted to the passivation of Si, which is much better understood. However, among several other issues, there exists an optimum Si cap thickness (~8 ML), which is limited by thickness-dependent strain relaxation of Si on Ge and Si oxidation as well as diffusion of Ge into the epitaxial Si layer.[4] The other approach uses a GeO_2 passivation layer on Ge, which can yield a midgap D_{it} as low as $\sim 10^{11}$ cm^{-2} eV^{-1}.[4,5] However, GeO_2 is water-soluble, and a H_2O-free gate-stack deposition process is needed.[4,8] In addition, GeO_2 has a relative dielectric constant of 7,[8] and Ge atoms can diffuse into the high-κ material if the GeO_2 IL is too thin.[2] These issues present a significant challenge for both approaches when it comes to scalability,[4] and intense research efforts are currently devoted to a search for alternative passivation layers or processing schemes.[11] More recently, approaches such as plasma postoxidation[12] and Y-SiO_2[13] show good promise for Ge passivation.

Concurrently, owing to the richness of their electronic, ionic, and magnetic properties, functional epitaxial binary oxides, perovskites, and oxide heterostructures have been under investigation for monolithic integration on mainstream semiconductor substrates such as Si (001) and Ge (001).[14] To date, a variety of functionalities such as magnetoresistance,[15−19]

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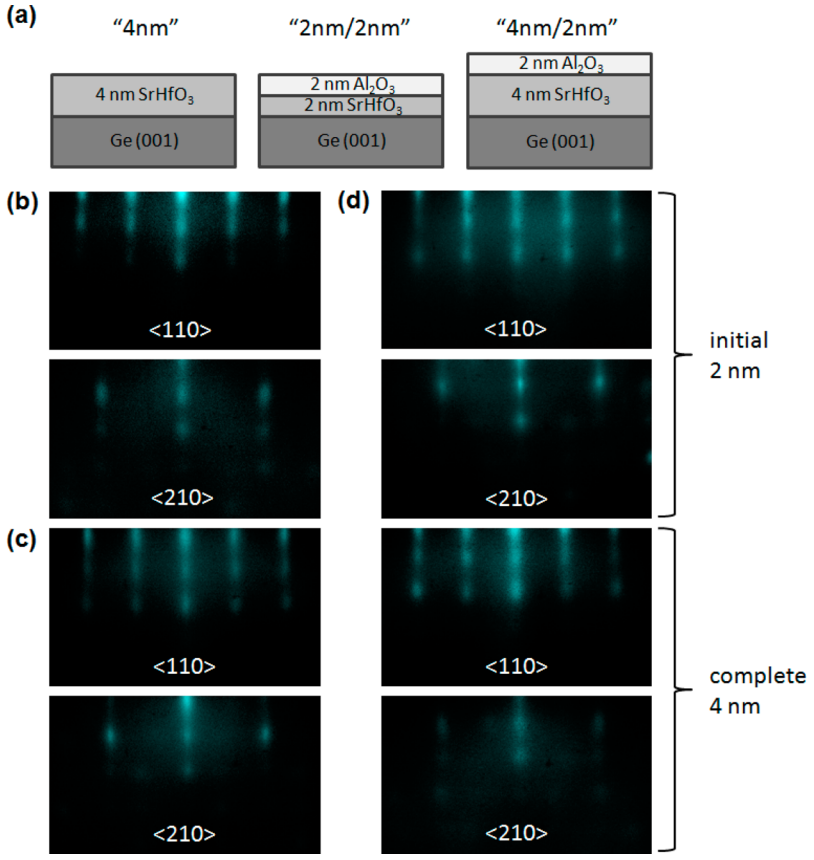

Figure 1. (a) Schematic diagrams of the 4 nm, the 2 nm/2 nm, and the 4 nm/2 nm samples. RHEED images obtained from as-crystallized (b) 4 nm $SrHfO_3$ film for the 4 nm sample, (c) 2 nm $SrHfO_3$ film for the 2 nm/2 nm sample, and (d) the initial 2 nm $SrHfO_3$ film (upper two images) and the complete 4 nm $SrHfO_3$ film (lower two images) for the 4 nm/2 nm sample. For each set of images taken, the beam is aligned along the [110] (top image) and the [210] (bottom image) azimuth.

resistive switching,[20−22] ferroelectricity,[23−27] and gate dielectrics[28,29] have been achieved with epitaxial oxides integrated monolithically on Si (001). Moreover, in a report by McKee et al., it has been shown that epitaxial oxides grown on Ge enable the formation of commensurate interface structures while maintaining continuity in dielectric displacement and systematic control of inversion charge based on which a high-mobility MOSFET can be realized.[30] Regarding practical applications, it should be noted that though the epitaxial perovskite gate oxides can only be grown on Si (001) and Ge (001) and may not be applicable to FinFET structures for which the crystal orientation for the fin side-walls is different from that of the fin top surface, epitaxial oxides as a gate dielectric can be applied to other alternative state-of-the-art schemes such as the fully depleted silicon/germanium on insulator.[31] In earlier work, we demonstrated the growth of single-crystal $SrTiO_3$ directly on Ge by atomic layer deposition (ALD),[32,33] and the structure shows excellent crystallinity of the $SrTiO_3$ film as well as an abrupt $SrTiO_3$/Ge interface.[34] Although the $SrTiO_3$ film possesses a high dielectric constant, the negligible conduction band offset at the $SrTiO_3$/Ge interface makes $SrTiO_3$ an inappropriate choice as the gate oxide for Ge-based MOSFETs. Unlike $SrTiO_3$, the large conduction band and valence band offsets of $SrHfO_3$ with Si and Ge enable it to be a promising candidate as a gate oxide material.[35−37] Recently, we reported the ALD growth and materials characterization of epitaxial $SrHfO_3$ on Ge with excellent crystallinity and favorable electronic properties as a high-κ oxide.[38] A systematic study of the feasibility of using epitaxial $SrHfO_3$-based gate stacks for Ge MOS devices as well as process optimization for D_{it} reduction, however, has yet to be presented. Here we report detailed analysis of several high-κ gate stacks composed of epitaxial crystalline $SrHfO_3$ grown directly on Ge by ALD, which show low leakage, small equivalent oxide thickness (EOT), and a reasonable and improvable D_{it}. The postgrowth annealing atmosphere is found to be essential in the reduction of D_{it}. In contrast to GeO_2- or epitaxial Si-based passivation schemes,[2,4] the high-κ gate-oxide stacks demonstrated here require no minimum thickness (except as imposed by the maximum allowable leakage current and by the minimum allowable Ge channel mobility[5]), which makes them highly suitable for deep scaling.

RESULTS AND DISCUSSION

MOS capacitor structures were created for three high-κ gate stack structures based on epitaxial $SrHfO_3$ grown directly on n-type Ge (001) substrates by ALD. Typical substrate resistivities were $\rho \approx 0.029-0.054\ \Omega$ cm. For each stack, amorphous $SrHfO_3$ films were deposited on the clean, 2 × 1 reconstructed Ge (001) surface[38] at a substrate temperature of 225 °C using strontium bis(triisopropylcyclopentadienyl) [$Sr(^iPr_3Cp)_2$] (Absolut-Sr), hafnium formamidinate (Hf-FAMD), and purified water as coreactants. The films were subsequently crystallized at temperatures between 650 and 725 °C in vacuum (<2×10^{-9} Torr) with a temperature ramp rate of 20 °C/min. The first gate stack consisted of a 4 nm $SrHfO_3$ film (referred to herein

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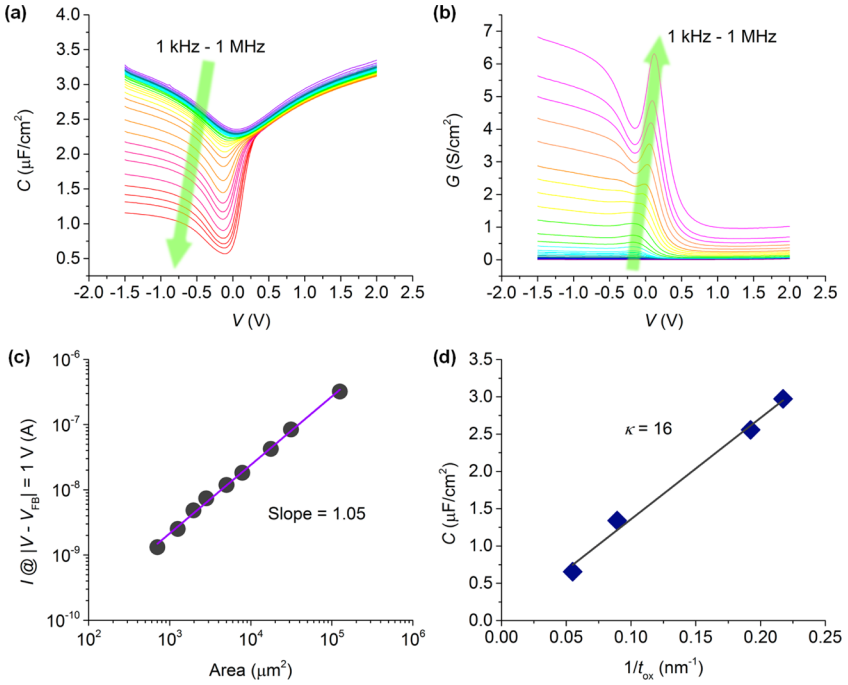

Figure 2. (a) Capacitance−voltage and (b) conductance−voltage characteristics of the 4 nm sample for frequencies from 1 kHz to 1 MHz; (c) leakage current as a function of device area for the 4 nm sample; (d) capacitance measured at 1 MHz in the accumulation regime for the $SrHfO_3$ films of different thickness for extraction of the dielectric constant of $SrHfO_3$.

as the 4 nm sample) that was crystallized by postdeposition vacuum annealing at 725 °C for 5 min. The second gate stack consisted of a 4 nm $SrHfO_3$ film capped with 2 nm of amorphous Al_2O_3 (referred to as the 4 nm/2 nm sample). In this case, the 4 nm $SrHfO_3$ film was grown in a two-step growth and anneal process where 2 nm of $SrHfO_3$ was deposited during each step and subsequently crystallized in vacuum at 700 °C for 5 min. In general, thinner $SrHfO_3$ films allowed for reduced annealing temperature for crystallization. For the third gate stack, 2 nm of $SrHfO_3$ was capped with 2 nm of amorphous Al_2O_3 (referred to as the 2 nm/2 nm sample). For this sample, the $SrHfO_3$ film was crystallized at 650 °C for 5 min, which was the lowest anneal temperature for which crystallization of the ALD-deposited $SrHfO_3$ layer was observed. Here in this work, the 2 nm Al_2O_3 capping layer is employed to further decrease leakage current, as will be discussed in detail later in this work. For each structure, a 30 min postgrowth annealing in dry air at 300 °C was performed to reduce D_{it}.

Figure 1, panel a shows schematics of the different gate stack structures for the 4 nm sample, the 2 nm/2 nm sample, and the 4 nm/2 nm sample, respectively. Figure 1, panels b−d show reflection high-energy electron diffraction (RHEED) images of the 4 nm sample, the 2 nm/2 nm sample, and the 4 nm/2 nm sample, respectively, before deposition of the top amorphous Al_2O_3 layer (if any). For the 4 nm/2 nm sample, RHEED images taken after crystallization of the initially deposited 2 nm $SrHfO_3$ (upper two images) and after crystallization of the latter 2 nm $SrHfO_3$ (lower two images) are both shown in Figure 1, panel d. Streak patterns can be seen for all three structures, indicative of the high crystalline quality of the $SrHfO_3$ film upon postdeposition vacuum annealing. Circular top electrode contacts with radius ranging from 15−200 μm were formed by sputtering of 200 nm TaN, photolithographic patterning, and SF_6-based inductively coupled plasma etching. The scratched backside of the n-type Ge substrate was coated with silver paste and then attached to a metal specimen disc. Electrical measurements for these $SrHfO_3$-crystallized samples (both before and after 30 min postgrowth annealing in dry air at 300 °C) were performed on a Cascade Microtech probe station in ambient conditions by applying voltage to the top electrode with the sample bottom grounded using an Agilent B1500A semiconductor device parameter analyzer. For the electrical measurements, we focused on devices with radius of 15 μm unless otherwise indicated.

Figure 2, panels a and b show the capacitance−voltage (C−V) and conductance−voltage (G−V) characteristics of the 4 nm sample measured at frequencies ranging from 1 kHz to 1 MHz. C−V and G−V curves for the 4 nm sample after postgrowth annealing and for the 2 nm/2 nm sample and 4 nm/2 nm sample before and after postgrowth annealing are shown in Figure S1 in the Supporting Information. The frequency dispersion of the C−V curves shows a clear signature of high-rate generation-recombination of minority carriers via midgap bulk traps in the Ge depletion layer (in the strong inversion regime) and via interface states (in the depletion and weak inversion regime) as well as a very short minority carrier response time, both due to the smaller band gap of Ge ($E_{g,Ge}$ = 0.67 eV) as compared to Si ($E_{g,Si}$ = 1.12 eV).[39,40] This behavior is also indicated in the G−V curves shown in Figure 2, panel b, from which conductance plateaus in strong inversion and outstanding conductance peaks in depletion and weak inversion are observed. C increases as V becomes more negative in the strong inversion regime even at 1 MHz, suggesting impurity (e.g., hafnium atom) diffusion into the Ge substrate or Ge diffusion into the $SrHfO_3$ layer near the Ge/$SrHfO_3$ interface, which act as bulk traps assisting generation/recombination of minority carriers within the depletion layer in the strong inversion regime or as fixed charge in the gate oxide.[39]

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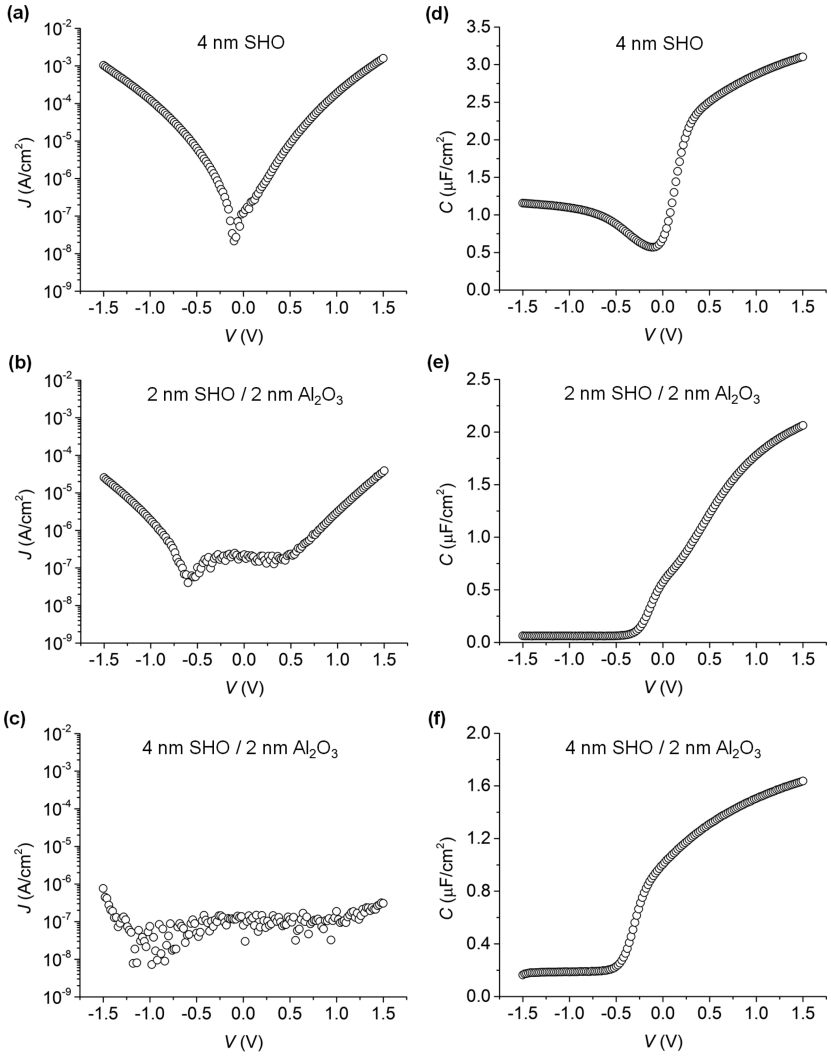

Figure 3. Leakage current density as a function of voltage for (a) the 4 nm, (b) the 2 nm/2 nm, and (c) the 4 nm/2 nm samples, with their corresponding capacitance–voltage characteristics measured at 1 MHz shown in panels d–f, respectively.

Such behavior together with the large conductance plateaus in strong inversion was not seen for the 2 nm/2 nm sample and the 4 nm/2 nm sample (Figure S1 in the Supporting Information), which were crystallized at lower temperatures. This indicates that crystallization temperature plays a significant role in the occurrence and degree of impurity diffusion from the gate dielectric to the Ge substrate (or Ge diffusion into the gate dielectric), as also reflected in a comparison of the transmission electron microscopy (TEM) images of these samples reported elsewhere.[38] Figure 2, panel c shows that the dielectric leakage current of the 4 nm sample scales almost linearly with the device area, indicative of an area-distributed leakage current through the 4 nm $SrHfO_3$ layer rather than a localized one. An additional series of samples with different thicknesses (4.6, 5.2, 11.2, and 18.2 nm) was grown with the same growth and in situ crystallization annealing condition as that for the 4 nm $SrHfO_3$ sample to determine the dielectric constant of the $SrHfO_3$. Figure 2, panel d shows the capacitance per unit area measured in the accumulation regime for different thicknesses of the crystallized $SrHfO_3$ film, from which the capacitance at infinitely large thickness is found to be zero and a dielectric constant κ = 16 can be extracted, consistent with previous reports.[35,37]

Figure 3, panels a–c show the current density–voltage (J–V) characteristics for the 4 nm, 2 nm/2 nm, and 4 nm/2 nm samples, respectively, all measured from the same 15 μm-radius devices used for C–V and G–V measurements, with their corresponding C–V curves obtained at 1 MHz shown in Figure 3, panels d–f. The 2 nm/2 nm sample is more insulating than the 4 nm sample, which can be understood from the fact that Al_2O_3 has a large band gap of 8.8 eV and a conduction band offset (CBO) of at least 2.6 eV with Ge,[41] whereas $SrHfO_3$ has a band gap of 6.1 eV and a CBO of 2.17 eV with Ge.[38] In the structures employed here, the $SrHfO_3$ layer is under ~1.6% lateral compressive strain, which is likely to affect the conduction and valence band offsets and leakage currents. Given the large magnitudes of the band offsets, however, strain-induced band-edge energy shifts would not be expected to dramatically influence the observed leakage currents. On the other hand, since the $SrHfO_3$ crystallization temperature of the 2 nm/2 nm sample is 75 °C lower than that of the 4 nm sample, and a higher degree of intermixing at the $SrHfO_3$/Ge interface due to the higher crystallization temperature can typically lead to more grain boundaries and therefore current leakage paths originating from the interface, the higher leakage current observed for the 4 nm sample can also be partly

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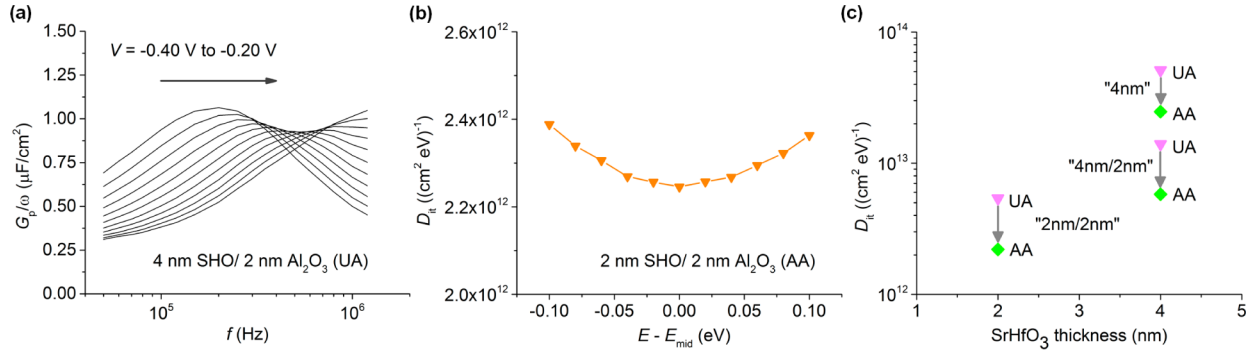

Figure 4. (a) Parallel conductance loss peaks in the frequency domain for the unannealed 4 nm/2 nm sample; (b) energy profile of interface trap density extracted for the air-annealed 2 nm/2 nm sample; (c) midgap (minimum) interface trap density for the 4 nm sample, 4 nm/2 nm sample, and 2 nm/2 nm sample before and after air-anneal. "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

attributed to the higher crystallization temperature that the sample underwent. As shown in Figure 3, panel c, the 4 nm/2 nm sample is the most insulating among the three samples, further verifying the high quality of the as-grown and crystallized $SrHfO_3$ film. Note that the flattened $J-V$ curves around 0 V shown in Figure 3, panels b and c are due to the minimum current level detectable by the testing equipment for the 15 μm-radius devices and therefore are likely to overestimate the leakage current for the corresponding voltage range. Nevertheless, the current densities shown in Figure 3 are well below the level required for these oxide stacks to be used as a gate dielectric.

The interface trap density D_{it} has also been extracted for all the samples under study using the conductance method,[42] and detailed studies of the dependence of D_{it} on postgrowth annealing conditions have been performed. Note that since all the electrical measurements were performed at room temperature, the presence of weak and strong inversion responses at room temperature typically leads to an overestimate of D_{it}, so the actual D_{it} values for the samples under study are likely to be smaller than the values reported in this work. It should also be noted that the discussion and conclusion made in this work regarding the D_{it} reduction trends are not affected by the overestimate of D_{it} values because the thermally induced effects are present and therefore increase the measured D_{it} for all the samples under study. Shown in Figure 4, panel a are the parallel conductance loss peaks (G_p) in the frequency domain for the unannealed 4 nm/2 nm sample as an example. Figure 4, panel b shows the energy profile of D_{it} for the air-annealed 2 nm/2 nm sample. It should be noted that the energy dependence of D_{it} is similar for all the samples under study. For the samples with an Al_2O_3 capping layer, it is expected that the Al_2O_3 layer would not affect D_{it} due to the underlying $SrHfO_3$ layer, which is at least 2 nm thick. The unannealed 4 nm/2 nm sample shows a midgap (minimum) D_{it} of 1.4×10^{13} cm^{-2} eV^{-1} (Figure 4c), much lower than that of the unannealed 4 nm sample (5.1×10^{13} cm^{-2} eV^{-1} as shown in Figure 4c). It is noteworthy that the crystallization temperature for the 4 nm/2 nm sample is 25 °C lower than the 4 nm sample, reducing the possibility of excessive intermixing at the $SrHfO_3$/Ge interface,[38] which is known to cause high D_{it}.[2−10]

The improvement in D_{it} from the 4 nm sample to the 4 nm/2 nm sample is believed to be related to the two-step growth technique, allowing for lower crystallization temperature to be employed after $SrHfO_3$ growth of the 4 nm/2 nm stack. As shown in Figure 1, the RHEED images for the as-crystallized initial 2 nm $SrHfO_3$ (Figure 1d) show sharper lines than that of the one-step grown and as-crystallized 4 nm $SrHfO_3$ (Figure 1b), indicating that higher crystallinity (less disorder) can be achieved by annealing a thinner 2 nm $SrHfO_3$ film. The improvement in D_{it} with lower crystallization temperature can be further justified in Figure 4, panel c through the comparison between the unannealed 4 nm/2 nm sample and the unannealed 2 nm/2 nm sample, for which the midgap D_{it} is 5.4×10^{12} cm^{-2} eV^{-1} and for which the crystallization temperature is 50 °C lower than the former. Previous studies have indicated that lower annealing temperature may result in small, isolated amorphous regions in the $SrHfO_3$ film.[38] However, our measurements of the $SrHfO_3$ dielectric constant, shown in Figure 2, panel d, indicate that any formation of such small and isolated amorphous regions that occurs here does not increase EOT despite the fact that the dielectric constant of as-deposited amorphous $SrHfO_3$ is determined to be ~7 based on $C-V$ measurements (not shown).

The influence of additional annealing procedures on D_{it} has also been investigated. As indicated in Figure 4, panel c, 30 min annealing in dry air (typical air conditions in a Class 100 clean room) at 300 °C after the sample growth and before the device fabrication lowers the minimum D_{it} for the 4 nm sample, the 4 nm/2 nm sample, and the 2 nm/2 nm sample to 2.4×10^{13} cm^{-2} eV^{-1}, 5.8×10^{12} cm^{-2} eV^{-1}, and 2.2×10^{12} cm^{-2} eV^{-1}, respectively, all by 50−60%, as summarized in Table S1 in the Supporting Information. While the dry air anneal is clearly very effective in reducing D_{it}, it was experimentally verified that other annealing schemes such as a wet oxidation (bubbling O_2 through deionized water at 95 °C) anneal or forming gas (4% H_2 and 96% N_2) anneal at temperatures ~300 °C did not reduce D_{it} of our $SrHfO_3$-based gate oxide structures (not shown). We note here that though forming gas anneal has no effect on D_{it} reduction for our samples as is consistent with most previous reports;[8] a recent report suggests that forming gas anneal can successfully passivate some structures such as Al_2O_3/Ge.[43]

The role of each gaseous component in the annealing and interface passivation process is therefore speculated to be as follows. The epitaxial growth of $SrHfO_3$ on Ge starts with SrO as the first atomic layer (followed by HfO_2 as the second atomic layer). TEM analysis has revealed that for a sufficiently low in situ vacuum crystallization temperature, the Ge diffusion into the gate dielectric or Hf diffusion into the Ge substrate and the resultant formation of an intermixing interlayer at the $SrHfO_3$/Ge interface can be suppressed.[38] On the other hand,

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it is well established that Ge can readily diffuse into HfO_2, which results in increased leakage current and D_{it} and makes HfO_2 unsuitable as a gate dielectric directly on Ge.[8,40] It is then reasonable to conclude that the SrO atomic plane can reduce such interdiffusion (or intermixing). However, it should also be noted that though the epitaxial $SrHfO_3$ film employed in this work is believed to have a single crystallographic orientation throughout the film, crystal defects, distortions, and resultant grain boundaries can still form during the film crystallization process that nevertheless follows thermodynamics and is also limited by the lattice mismatch between $SrHfO_3$ and Ge.[38] As noted previously, the formation of grain boundaries is also facilitated by the Hf and/or Ge interdiffusion (or intermixing) at the $SrHfO_3$/Ge interface so a higher crystallization temperature typically leads to more grain boundaries originating from the interface. It is well-known that fast diffusion of atoms occurs at grain boundaries.[8] Once Ge atoms diffuse through the grain boundaries of the adjacent SrO atomic layer, they can easily diffuse through the HfO_2 atomic layer and reach the next SrO plane. Therefore, it is believed that these grain boundaries present in the epitaxial $SrHfO_3$ film that extend to the $SrHfO_3$/Ge interface are mainly responsible for the high D_{it} observed for the as-crystallized and unannealed samples. Since in this work, dielectric growth on the Ge surface was in situ and the Ge surface was thoroughly cleaned prior to the ALD growth and in situ crystallization of $SrHfO_3$, no amorphous GeO_2, the ideal barrier for Ge or Hf diffusion, was formed at the $SrHfO_3$/Ge interface during the $SrHfO_3$ deposition process. O_2 is then needed as the critical ingredient of the postcrystallization annealing atmosphere to form an ultrathin (ideally less than 0.3 nm thick) amorphous GeO_2 layer at the $SrHfO_3$/Ge interface that passivates the Ge surface.[2−4,8] Here, it should be first noted that N_2 does not play any role at the annealing temperatures employed (~300 °C) except to dilute the active gaseous components. Therefore, a conventional forming gas anneal makes no contribution to the Ge surface passivation and D_{it} reduction, consistent with other reports.[5,8] The O_2 anneal, however, must be H_2O- or air moisture-free because GeO_2 is soluble upon exposure to water or air moisture and that readily degrades the interfacial quality,[2−4,8] which explains why the wet oxidation anneal was not capable of reducing D_{it}. The dry air anneal performed in this work did not cause any significant degradation of the gate oxide capacitance and therefore EOT. Specifically, EOT values for the unannealed 4 nm, 2 nm/2 nm, and 4 nm/2 nm samples are 1, 1.7, and 2.1 nm, respectively, whereas EOTs for the air-annealed 4 nm, 2 nm/2 nm, and 4 nm/2 nm samples are 1.1, 1.6, and 2.2 nm, respectively (Table S1 in the Supporting Information). Compared with the conventional GeO_2-based passivation approach, our approach demonstrated in this work requires in principle no minimum thickness of the gate dielectric but still takes advantage of the passivation capability of the interfacial amorphous GeO_2 layer, because with the introduction of an ultrathin interfacial GeO_2 layer that significantly lowers the probability of Ge or Hf diffusion, even if the SrO layers in the $SrHfO_3$ contain grain boundaries, these layers can still work effectively in a statistical sense as secondary diffusion barriers.

Our results also yield combinations of leakage current suppression and EOT that compare very favorably with the current state of the art. Figure 5 shows J versus EOT found in recent reports that represent the state of the art of gate stack development for Ge-based MOSFETs,[44−52] along with our results in this work (indicated by stars). Leakage currents measured for both the unannealed and the air-annealed $SrHfO_3$ films or $SrHfO_3/Al_2O_3$ stacks in this work define the lower bound of J for their corresponding ranges of EOT in Figure 5, respectively. Moreover, with further scaling of the gate dielectric stacks, it is expected that the advantage of using the gate stacks developed in this work regarding the attainable combinations of J and EOT would be even more pronounced. It should also be noted that for the previous publications shown in Figure 5 that reported a D_{it} minimum,[44,45,47,50−52] the D_{it} values are mainly on the order of lower 10^{11} cm^{-2} eV^{-1}, which is about 10-times lower than the best D_{it} achieved in this work. Therefore, for our $SrHfO_3$-based gate stacks, a D_{it} comparable to the current state of the art remains to be achieved. Since the formation of grain boundaries during the crystallization process, largely originating from the lattice mismatch between the epitaxial $SrHfO_3$ and Ge, is believed to cause a high D_{it}, it is therefore expected that D_{it} can be improved by further decreasing or eliminating the lattice mismatch,[53] which may be possible with materials such as $Sr(Hf,Ti)O_3$ or $CaHfO_3$.

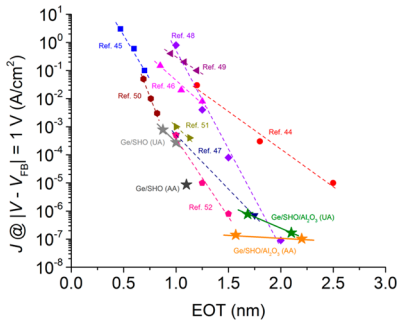

Figure 5. Leakage current versus EOT reported as the state of the art in recently published work together with our results in this work (star symbols). "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

CONCLUSION

In summary, we demonstrate the use of gate dielectric stacks based on ALD-grown epitaxial $SrHfO_3$ for Ge-based MOS applications. The gate stacks developed in this work yield combinations of ultralow leakage current and a small EOT, which are comparable or superior to the state of the art published so far in the gate stack development for Ge-based MOSFETs. While interface state densities D_{it} of ~2×10^{12} cm^{-2} eV^{-1} must still be improved, our work shows that D_{it} can be very substantially reduced by using (i) a two-step technique for the epitaxial growth; (ii) a lower crystallization temperature for minimized intermixing at the $SrHfO_3$/Ge interface; and (iii) postgrowth dry air annealing. A detailed analysis of the physical mechanism explaining the role of postgrowth annealing atmosphere in D_{it} reduction is presented. Findings of this work hold a great promise of using epitaxial gate dielectrics for Ge MOSFETs and suggest possible routes to further optimizing the electrical properties of these gate stacks.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b10661.

Figures showing $C-V$ and $G-V$ curves for the 4 nm sample after air anneal, the 4 nm/2 nm sample before

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and after air anneal, and the 2 nm/2 nm sample before and after air anneal; table summarizing the midgap D_{it} and EOT for the 4 nm sample, the 4 nm/2 nm sample, and the 2 nm/2 nm sample both before and after air anneal (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Chau, R.; Datta, S.; Doczy, M.; Doyle, B.; Kavalieros, J.; Metz, M. High-κ/Metal-Gate Stack and Its MOSFET Characteristics. *IEEE Electron Device Lett.* **2004**, *25*, 408−410.

(2) Goley, P. S.; Hudait, M. K. Germanium Based Field-Effect Transistors: Challenges and Opportunities. *Materials* **2014**, *7*, 2301−2339.

(3) Claeys, C.; Mitard, J.; Hellings, G.; Eneman, G.; De Jaeger, B.; Witters, L.; Loo, R.; Delabie, A.; Sioncke, S.; Caymax, M.; Simoen, E. Status and Trends in Ge CMOS Technology. *ECS Trans.* **2013**, *54*, 25−37.

(4) Simoen, E.; Mitard, J.; Hellings, G.; Eneman, G.; De Jaeger, B.; Witters, L.; Vincent, B.; Loo, R.; Delabie, A.; Sioncke, S.; Caymax, M.; Claeys, C. Challenges and Opportunities in Advanced Ge pMOSFETs. *Mater. Sci. Semicond. Process.* **2012**, *15*, 588−600.

(5) Pillarisetty, R. Academic and Industry Research Progress in Germanium Nanodevices. *Nature* **2011**, *479*, 324−328.

(6) Toriumi, A.; Lee, C. H.; Wang, S. K.; Tabata, T.; Yoshida, M.; Zhao, D. D.; Nishimura, T.; Kita, K.; Nagashio, K. Material Potential and Scalability Challenges of Germanium CMOS. *IEEE Int. Electron Devices Meet.* **2011**, 646−649.

(7) Caymax, M.; Eneman, G.; Bellenger, F.; Merckling, C.; Delabie, A.; Wang, G.; Loo, R.; Simoen, E.; Mitard, J.; De Jaeger, B.; Hellings, G.; De Meyer, K.; Meuris, M.; Heyns, M. Germanium for Advanced CMOS Anno 2009: a SWOT Analysis. *IEEE Int. Electron Devices Meet.* **2009**, 461−464.

(8) Kamata, Y. High-k/Ge MOSFETs for Future Nanoelectronics. *Mater. Today* **2008**, *11*, 30−38.

(9) Brunco, D. P.; De Jaeger, B.; Eneman, G.; Mitard, J.; Hellings, G.; Satta, A.; Terzieva, V.; Souriau, L.; Leys, F. E.; Pourtois, G.; Houssa, M.; Winderickx, G.; Vrancken, E.; Sioncke, S.; Opsomer, K.; Nicholas, G.; Caymax, M.; Stesmans, A.; Van Steenbergen, J.; Mertens, P. W.; Meuris, M.; Heyns, M. M. Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance. *J. Electrochem. Soc.* **2008**, *155*, H552−H561.

(10) Shang, H.; Frank, M. M.; Gusev, E. P.; Chu, J. O.; Bedell, S. W.; Guarini, K. W.; Ieong, M. Germanium Channel MOSFETs: Opportunities and Challenges. *IBM J. Res. Dev.* **2006**, *50*, 377−386.

(11) Gupta, S.; Gong, X.; Zhang, R.; Yeo, Y.-C.; Takagi, S.; Saraswat, K. C. New Materials for Post-Si Computing: Ge and GeSn Devices. *MRS Bull.* **2014**, *39*, 678−686.

(12) Zhang, R.; Iwasaki, T.; Taoka, N.; Takenaka, M.; Takagi, S. High-Mobility Ge pMOSFET with 1-nm EOT Al_2O_3/GeO_x/Ge Gate Stack Fabricated by Plasma Post Oxidation. *IEEE Trans. Electron Devices* **2012**, *59*, 335−341.

(13) Lu, C.; Lee, C. H.; Zhang, W.; Nishimura, T.; Nagashio, K.; Toriumi, A. Structural and Thermodynamic Consideration of Metal Oxide Doped GeO_2 for Gate Stack Formation on Germanium. *J. Appl. Phys.* **2014**, *116*, 174103.

(14) Demkov, A. A.; Posadas, A. B.; Seo, H.; Choi, M.; Kormondy, K. J.; Ponath, P.; Hatch, R. C.; McDaniel, M. D.; Ngo, T. Q.; Ekerdt, J. G. Monolithic Integration of Oxides on Semiconductors. *ECS Trans.* **2013**, *54*, 255−269.

(15) Ramesh, R.; Spaldin, N. A. Multiferroics: Progress and Prospects in Thin Films. *Nat. Mater.* **2007**, *6*, 21−29.

(16) Kim, J.-H.; Khartsev, S. I.; Grishin, A. M. Epitaxial Colossal Magnetoresistive $La_{0.67}(Sr,Ca)_{0.33}MnO_3$ Films on Si. *Appl. Phys. Lett.* **2003**, *82*, 4295−4297.

(17) Pradhan, A. K.; Mohanty, S.; Zhang, K.; Dadson, J. B.; Jackson, E. M.; Hunter, D.; Rakhimov, R. R.; Loutts, G. B.; Zhang, J.; Sellmyer, D. J. Integration of Epitaxial Colossal Magnetoresistive Films onto Si(100) Using $SrTiO_3$ as a Template Layer. *Appl. Phys. Lett.* **2005**, *86*, 012503.

(18) Martin, L. W.; Chu, Y.-H.; Zhan, Q.; Ramesh, R.; Han, S.-J.; Wang, S. X.; Warusawithana, M.; Schlom, D. G. Room Temperature Exchange Bias and Spin Valves Based on $BiFeO_3/SrRuO_3/SrTiO_3$/Si (001) Heterostructures. *Appl. Phys. Lett.* **2007**, *91*, 172513.

(19) Hu, C.; Park, K. W.; Posadas, A.; Jordan-Sweet, J. L.; Demkov, A. A.; Yu, E. T. Voltage-Controlled Ferromagnetism and Magnetoresistance in $LaCoO_3/SrTiO_3$ Heterostructures. *J. Appl. Phys.* **2013**, *114*, 183909.

(20) Hu, C.; McDaniel, M. D.; Ekerdt, J. G.; Yu, E. T. High ON/OFF Ratio and Quantized Conductance in Resistive Switching of TiO_2 on Silicon. *IEEE Electron Device Lett.* **2013**, *34*, 1385−1387.

(21) Hu, C.; McDaniel, M. D.; Posadas, A.; Demkov, A. A.; Ekerdt, J. G.; Yu, E. T. Highly Controllable and Stable Quantized Conductance and Resistive Switching Mechanism in Single-Crystal TiO_2 Resistive Memory on Silicon. *Nano Lett.* **2014**, *14*, 4360−4367.

(22) Yu, E. T.; Hu, C.; McDaniel, M. D.; Posadas, A.; Demkov, A. A.; Ekerdt, J. G. Resistive Switching Characteristics and Controllable Quantized Conductance in Single-Crystal Anatase TiO_2 on Si (001). *ECS Trans.* **2014**, *64*, 147−152.

(23) Ahn, C. H.; Rabe, K. M.; Triscone, J.-M. Ferroelectricity at the Nanoscale: Local Polarization in Oxide Thin Films and Heterostructures. *Science* **2004**, *303*, 488−491.

(24) Ponath, P.; Fredrickson, K.; Posadas, A. B.; Ren, Y.; Wu, X.; Vasudevan, R. K.; Baris Okatan, M.; Jesse, S.; Aoki, T.; McCartney, M. R.; Smith, D. J.; Kalinin, S. V.; Lai, K.; Demkov, A. A. Carrier Density Modulation in a Germanium Heterostructure by Ferroelectric Switching. *Nat. Commun.* **2015**, *6*, 6067.

(25) Lee, H. N.; Hesse, D.; Zakharov, N.; Gösele, U. Ferroelectric $Bi_{3.25}La_{0.75}Ti_3O_{12}$ Films of Uniform a-Axis Orientation on Silicon Substrates. *Science* **2002**, *296*, 2006−2009.

(26) Warusawithana, M. P.; Cen, C.; Sleasman, C. R.; Woicik, J. C.; Li, Y.; Kourkoutis, L. F.; Klug, J. A.; Li, H.; Ryan, P.; Wang, L.-P.; Bedzyk, M.; Muller, D. A.; Chen, L.-Q.; Levy, J.; Schlom, D. G. A Ferroelectric Oxide Made Directly on Silicon. *Science* **2009**, *324*, 367−370.

(27) Dubourdieu, C.; Bruley, J.; Arruda, T. M.; Posadas, A.; Jordan-Sweet, J.; Frank, M. M.; Cartier, E.; Frank, D. J.; Kalinin, S. V.; Demkov, A. A.; Narayanan, V. Switching of Ferroelectric Polarization in Epitaxial $BaTiO_3$ Films on Silicon without a Conducting Bottom Electrode. *Nat. Nanotechnol.* **2013**, *8*, 748−754.

(28) Yu, Z.; Ramdani, J.; Curless, J. A.; Overgaard, C. D.; Finder, J. M.; Droopad, R.; Eisenbeiser, K. W.; Hallmark, J. A.; Ooms, W. J.; Kaushik, V. S. Epitaxial Oxide Thin Films on Si(001). *J. Vac. Sci. Technol., B: Microelectron. Process. Phenom.* **2000**, *18*, 2139.

(29) Ngo, T. Q.; Posadas, A. B.; McDaniel, M. D.; Hu, C.; Bruley, J.; Yu, E. T.; Demkov, A. A.; Ekerdt, J. G. Epitaxial c-Axis Oriented $BaTiO_3$ Thin Films on $SrTiO_3$-Buffered Si(001) by Atomic Layer Deposition. *Appl. Phys. Lett.* **2014**, *104*, 082910.

DOI: 10.1021/acsami.5b10661
ACS Appl. Mater. Interfaces 2016, 8, 5416−5423

(30) McKee, R. A.; Walker, F. J.; Chisholm, M. F. Physical Structure and Inversion Charge at a Semiconductor Interface with a Crystalline Oxide. *Science* **2001**, *293*, 468−471.
(31) Vitale, S. A.; Wyatt, P. W.; Checka, N.; Kedzierski, J.; Keast, C. L. FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics. *Proc. IEEE* **2010**, *98*, 333−342.
(32) Leskelä, M.; Ritala, M. Atomic Layer Deposition (ALD): from Precursors to Thin Film Structures. *Thin Solid Films* **2002**, *409*, 138−146.
(33) George, S. M. Atomic Layer Deposition: an Overview. *Chem. Rev.* **2010**, *110*, 111−131.
(34) McDaniel, M. D.; Ngo, T. Q.; Posadas, A.; Hu, C.; Lu, S.; Smith, D. J.; Yu, E. T.; Demkov, A. A.; Ekerdt, J. G. A Chemical Route to Monolithic Integration of Crystalline Oxides on Semiconductors. *Adv. Mater. Interfaces* **2014**, *1*, 1400081.
(35) Rossel, C.; Mereu, B.; Marchiori, C.; Caimi, D.; Sousa, M.; Guiller, A.; Siegwart, H.; Germann, R.; Locquet, J.-P.; Fompeyrine, J.; Webb, D. J.; Dieker, Ch.; Seo, J. W. Field-Effect Transistors with $SrHfO_3$ as Gate Oxide. *Appl. Phys. Lett.* **2006**, *89*, 053506.
(36) Sousa, M.; Rossel, C.; Marchiori, C.; Siegwart, H.; Caimi, D.; Locquet, J.-P.; Webb, D. J.; Germann, R.; Fompeyrine, J.; Babich, K.; Seo, J. W.; Dieker, Ch. Optical Properties of Epitaxial $SrHfO_3$ Thin Films Grown on Si. *J. Appl. Phys.* **2007**, *102*, 104103.
(37) Rossel, C.; Sousa, M.; Marchiori, C.; Fompeyrine, J.; Webb, D.; Caimi, D.; Mereu, B.; Ispas, A.; Locquet, J. P.; Siegwart, H.; Germann, R.; Tapponnier, A.; Babich, K. $SrHfO_3$ as Gate Dielectric for Future CMOS Technology. *Microelectron. Eng.* **2007**, *84*, 1869−1873.
(38) McDaniel, M. D.; Hu, C.; Lu, S.; Ngo, T. Q.; Posadas, A.; Jiang, A.; Smith, D. J.; Yu, E. T.; Demkov, A. A.; Ekerdt, J. G. Atomic Layer Deposition of Crystalline $SrHfO_3$ Directly on Ge (001) for High-*k* Dielectric Applications. *J. Appl. Phys.* **2015**, *117*, 054101.
(39) Batude, P.; Garros, X.; Clavelier, L.; Le Royer, C.; Hartmann, J. M.; Loup, V.; Besson, P.; Vandroux, L.; Campidelli, Y.; Deleonibus, S.; Boulanger, F. Insights on Fundamental Mechanisms Impacting Ge Metal Oxide Semiconductor Capacitors with High-*k*/Metal Gate Stacks. *J. Appl. Phys.* **2007**, *102*, 034514.
(40) Martens, K.; Chui, C. O.; Brammertz, G.; De Jaeger, B.; Kuzum, D.; Meuris, M.; Heyns, M. M.; Krishnamohan, T.; Saraswat, K.; Maes, H. E.; Groeseneken, G. On the Correct Extraction of Interface Trap Density of MOS Devices with High-Mobility Semiconductor Substrates. *IEEE Trans. Electron Devices* **2008**, *55*, 547−556.
(41) Robertson, J. Band Offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices. *J. Vac. Sci. Technol., B: Microelectron. Process. Phenom.* **2000**, *18*, 1785−1791.
(42) Nicollian, E. H.; Brews, J. R. *MOS (Metal Oxide Semiconductor) Physics and Technology*; John Wiley & Sons: New York, 1982; Ch. 5, pp 212−221.
(43) Zhang, L.; Li, H.; Guo, Y.; Tang, K.; Woicik, J.; Robertson, J.; McIntyre, P. C. Selective Passivation of GeO_2/Ge Interface Defects in Atomic Layer Deposited High-*k* MOS Structures. *ACS Appl. Mater. Interfaces* **2015**, *7*, 20499−20506.
(44) Swaminathan, S.; Shandalov, M.; Oshima, Y.; McIntyre, P. C. Bilayer Metal Oxide Gate Insulators for Scaled Ge-Channel Metal-Oxide-Semiconductor Devices. *Appl. Phys. Lett.* **2010**, *96*, 082904.
(45) Lee, C. H.; Lu, C.; Tabata, T.; Zhang, W. F.; Nishimura, T.; Nagashio, K.; Toriumi, A. Oxygen Potential Engineering of Interfacial Layer for Deep Sub-nm EOT High-k Gate Stacks on Ge. *IEEE Int. Electron Devices Meet.* **2013**, 40−43.
(46) Mitard, J.; Shea, C.; DeJaeger, B.; Pristera, A.; Wang, G.; Houssa, M.; Eneman, G.; Hellings, G.; Wang, W.-E.; Lin, J. C.; Leys, F. E.; Loo, R.; Winderickx, G.; Vrancken, E.; Stesmans, A.; DeMeyer, K.; Caymax, M.; Pantisano, L.; Meuris, M.; Heyns, M. Impact of EOT Scaling down to 0.85nm on 70nm Ge-pFETs Technology with STI. *Technol. Dig. − VLSI Symp. Technol.* **2009**, 82−83.
(47) Xie, R.; Phung, T. H.; He, W.; Yu, M.; Zhu, C. Interface-Engineered High-Mobility High-k/Ge pMOSFETs with 1-nm Equivalent Oxide Thickness. *IEEE Trans. Electron Devices* **2009**, *56*, 1330−1337.
(48) Kamata, Y.; Ikeda, K.; Kamimuta, Y.; Tezuka, T. High-k/Ge p- & n-MISFETs with Strontium Germanide Interlayer for EOT Scalable CMIS Application. *2010 IEEE Symposium on VLSI Technology* **2010**, 211−212.
(49) Chen, W. B.; Shie, B. S.; Chin, A.; Hsu, K. C.; Chi, C. C. Higher k Metal-Gate/High-k/Ge n-MOSFETs with < 1 nm EOT Using Laser Annealing. *IEEE Int. Electron Devices Meet.* **2010**, 420−423.
(50) Zhang, R.; Huang, P. C.; Taoka, N.; Takenaka, M.; Takagi, S. High Mobility Ge pMOSFETs with 0.7 nm Ultrathin EOT Using HfO2/Al2O3/GeOx/Ge Gate Stacks Fabricated by Plasma Post Oxidation. *2012 IEEE Symposium on VLSI Technology* **2012**, 161−162.
(51) Zhang, R.; Iwasaki, T.; Taoka, N.; Takenaka, M.; Takagi, S. High Mobility Ge pMOSFETs with ∼ 1nm Thin EOT Using Al_2O_3/GeO_x/Ge Gate Stacks Fabricated by Plasma Post Oxidation. *IEEE Trans. Electron Devices* **2012**, *59*, 56−57.
(52) Lee, C. H.; Lu, C.; Tabata, T.; Nishimura, T.; Nagashio, K.; Toriumi, A. Enhancement of High-N_s Electron Mobility in Sub-nm EOT Ge n-MOSFETs. *Technol. Dig. − VLSI Symp. Technol.* **2013**, 28−29.
(53) Wang, X.; Dong, L.; Zhang, J.; Liu, Y.; Ye, P. D.; Gordon, R. G. Heteroepitaxy of La_2O_3 and $La_{2-x}Y_xO_3$ on GaAs (111)A by Atomic Layer Deposition: Achieving Low Interface Trap Density. *Nano Lett.* **2013**, *13*, 594−599.

DOI: 10.1021/acsami.5b10661
ACS Appl. Mater. Interfaces 2016, 8, 5416−5423