

# Localized dielectric breakdown and antireflection coating in metal–oxide–semiconductor photoelectrodes

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Sections	Page
I. Materials and Fabrication Methods	
<i>Substrate preparation</i> .....	2
<i>Metal oxide growth</i> .....	2
<i>Metallization</i> .....	3
II. Dielectric Breakdown	
<i>Brief theory of dielectric breakdown</i> .....	3
<i>Compliance current effect</i> .....	4
<i>Read voltage range effect</i> .....	5
<i>Oxide quality effect</i> .....	5
<i>Metal catalyst pad size effect</i> .....	6
III. Permalloy (Ni <sub>81</sub> Fe <sub>19</sub> ) as OER catalyst	
<i>Preparation methods</i> .....	6
<i>Electrochemical Measurements</i> .....	7
<i>XPS results</i> .....	8
<i>Benchmarks of OER catalysts</i> .....	9
IV. Antireflection functionality	
<i>Simulation methods</i> .....	9
<i>Optimization of thickness</i> .....	10
V. PEC characterization	
<i>SECM results</i> .....	11

## I. Materials and fabrication methods

### Substrate preparation

Two types of 4 inch Si (001) wafers were used as substrates in this study. n-Si (phosphorus doped,  $\rho = 0.5\text{--}1\ \Omega\ \text{cm}$ ) substrates were used for photoanodes and p-Si (boron doped,  $\rho = 1\text{--}5\ \Omega\ \text{cm}$ ) for photocathodes. The Si wafers were first cleaved into  $1\text{cm} \times 1\text{cm}$  square pieces, followed by cleaning with piranha solution ( $\text{H}_2\text{O}:\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ ), buffered oxide etch solution (BOE,  $\text{HF}:\text{HCl}:\text{NH}_4\text{F}$ ) and deionized water (DI), in succession. The back contact was formed by e-beam evaporation of 5nmCr/100nmAu.

n-GaAs (100)-oriented (Te-doped,  $1 \times 10^{17}\ \text{cm}^{-3}$ ) polished substrates were used for the GaAs-based photoanode. The wafers were cleaned by BOE, acetone, isopropyl alcohol (IPA), deionized water, in succession. The back contact was formed by e-beam evaporation of 10nmNi/50nmAu<sub>88</sub>Ge<sub>12</sub>.

### Metal oxide growth

#### 1. SiO<sub>2</sub>

SiO<sub>2</sub> thin films were grown by three methods.

First, high quality thermal SiO<sub>2</sub> films were grown at 950 °C in an oxidation furnace (MRL 8' furnace, Sandvik Thermal Process Inc) in dry O<sub>2</sub> ambient. This method has been widely used to fabricate gate oxides in MOSFETs with good interfacial quality and low defect density. The p or n-Si/SiO<sub>2</sub> samples shown in the main manuscript were all grown by this method.

Second, ebeam evaporation was used to deposit SiO<sub>2</sub> on Si substrates as a reference samples, in order to investigate the dependence of dielectric breakdown properties on the quality of metal oxides, as discussed in detail in *Section II*.

For structures in which GaAs was used for the photoanode, high quality silicon oxides were grown by plasma-enhanced-atomic-layer-deposition (PEALD) (1-4). In addition, before the deposition of SiO<sub>2</sub>, a 1.5 nm thick Al<sub>2</sub>O<sub>3</sub> was first grown by thermal ALD on the GaAs substrate to reduce the interfacial defect density and stabilized the substrate, a standard process developed by Ye *et. al.* (5). The silicon oxide PEALD was performed in a Fiji ALD with remote plasma & ozone generator system (Cambridge Nanotech), with tris-dimethylamino-silane and plasma ozone as precursors. The growth temperature was 100 °C and the growth rate was  $\sim 0.8\ \text{\AA}/\text{cycle}$ . Remote mode was used, in which the plasma sources were located remotely from the substrate stage to improve control of plasma properties.

#### 2. TiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>

Thermal ALD of TiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> have been widely studied. Here in this work, we used standard recipes, as described below, in a ALD SavannahTM 200 system (Cambridge NanoTech). The growth temperatures were all set to 200 °C. For TiO<sub>2</sub>, the pulse time for H<sub>2</sub>O and tetrakis-titanium were 0.015s and 0.1s, respectively. For Al<sub>2</sub>O<sub>3</sub>, the pulse time for H<sub>2</sub>O and trimethylaluminum were 0.015s and 0.015s, respectively.

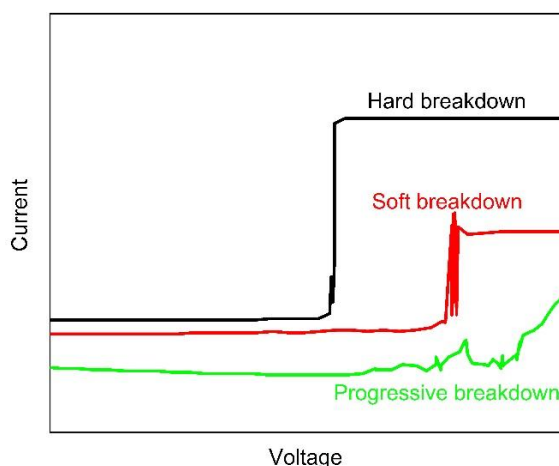
### Metallization

Permalloy (Py) was used as the OER catalyst for all photoanodes and Ti/Pt bilayers were used as HER catalysts for all photocathodes. A series of standard photolithography, e-beam evaporation and lift-off processes were performed to pattern regular array structures on photoelectrodes with various pitch sizes. The thicknesses of Py and Ti/Pt were 150 nm and 30nm/20nm, respectively. AZ5209 was used as positive photoresist for photolithography and Remover PG (MicroChem) was used for lift-off. Then the samples were rinsed by acetone, IPA and DI water with ultrasonic agitation for 5 mins each.

## II. Dielectric Breakdown

### *Brief theory of dielectric breakdown*

Electrical breakdown of dielectric layers in metal-oxide-semiconductor devices has been studied for decades in the context of reliability and device failure, and more recently has been investigated for applications in non-volatile memory.



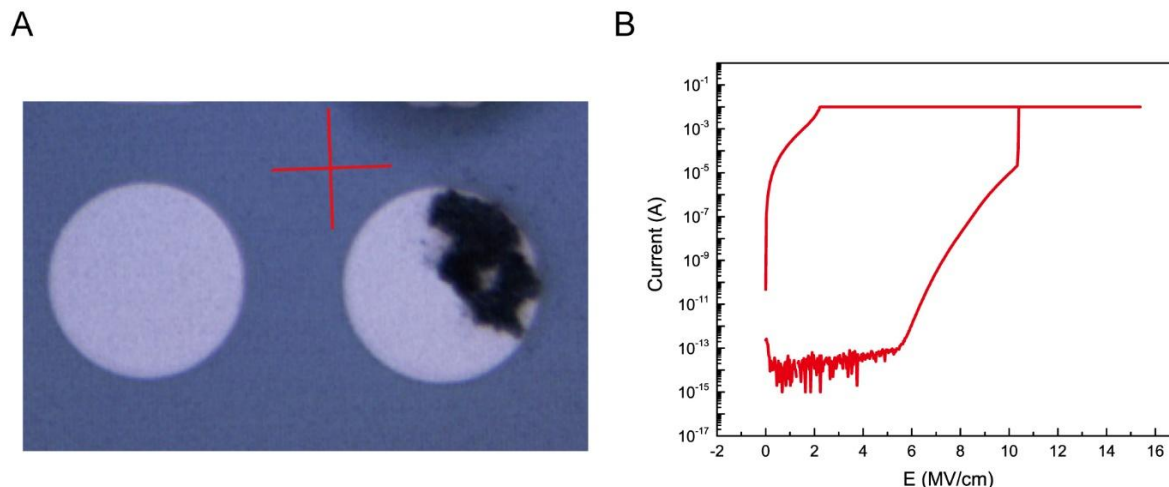
**Fig. S1.** Schematic of the three different kinds of breakdown occurrences by ramp voltage sweep.

There are different modes of breakdown that can occur in dielectric thin films, including hard breakdown (HBD), soft breakdown (SBD) and progressive breakdown (PBD)(6-14). Under electrical stressing at constant voltage, they show different behaviors as illustrated in Fig. S1. When soft or hard breakdown occurs, the current rapidly increases. The magnitude of current after breakdown distinguishes SBD from HBD, and the different current levels are attributed to a difference of conduction path created in the oxide by defect percolation. PBD does not show a sharp transient and typically only occurs in oxides thinner than  $\sim 25$  Å. For the purpose of this work, high current after breakdown is desired, and we therefore attempt to induce HBD.

Much less is known about the post-breakdown conduction mechanism mainly because of the random nature of breakdown and sample-to-sample-variation. Several models have been proposed, such as junction-like conduction, variable-range hopping, direct tunneling and trap-assisted tunneling. Regarding the nature of the breakdown process, what is currently accepted is that oxide breakdown

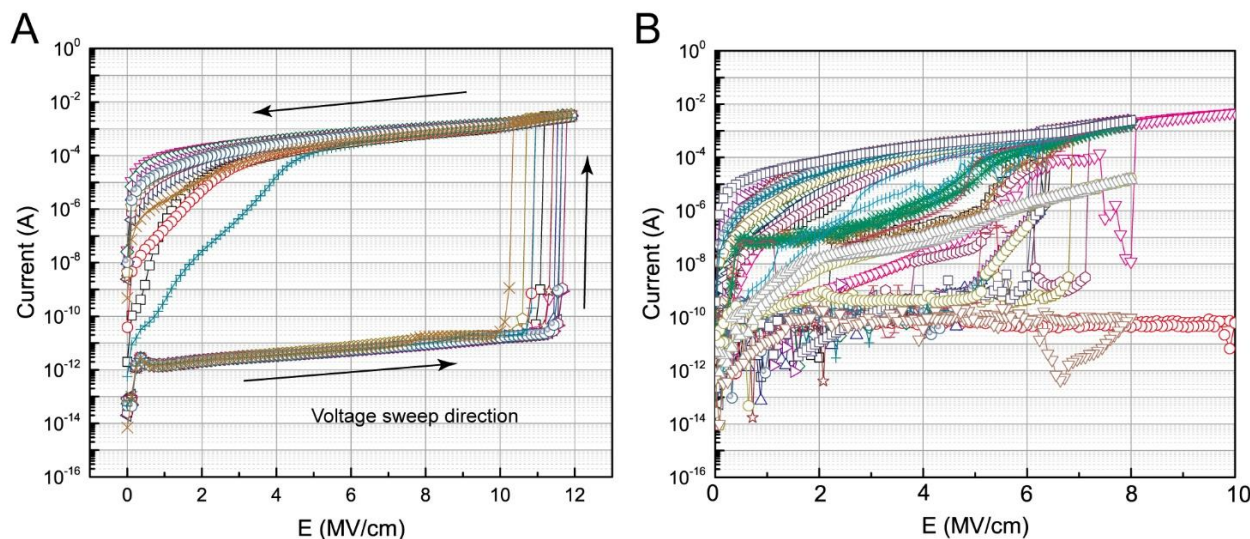
arises from the generation and accumulation of defects in the oxides. There is a general consensus that a critical density of defects generated at random locations eventually leads to the formation of a localized highly conductive leakage path, or filament, across the oxide layer.

Compliance current



**Fig. S2** (A) Optical microscope image of burned and not burned metal pad. (B) I-E characteristics of nSi/30nmSiO<sub>2</sub>/Py devices with forward bias applied to the top metal contact (Py) with 10 mA compliance current.

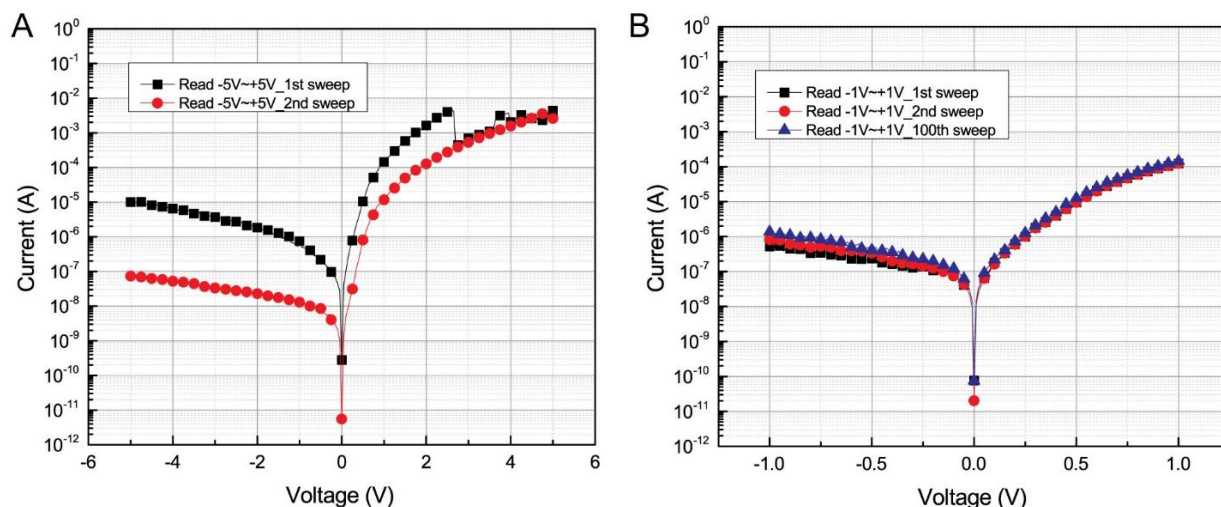
In an HBD process, the high current flow after breakdown can damage or destroy the metal contact that in our work serves as a catalyst. As shown in Fig. S2(A), if no compliance current is set during voltage sweep breakdown, the total current flow across the metal pad can be so high that the metal pad is burned, as shown in the right metal dot in Fig. S2(A). Thus, a compliance current is required during the BD process to preserve the integrity of the metal catalyst. We have found that 5 mA compliance current is sufficient to protect the catalysts while providing enough current flow for the robust growth of conducting filaments. Fig. S2 (B) is a typical breakdown curve.



**Fig. S3** Breakdown of n-Si/30nmSiO<sub>2</sub> samples with oxides grown by (A) thermally oxidation and (B) e-beam evaporation. The different curves in each plot represent different devices. The voltage sweep direction is as indicated as the arrows in (A)

### Oxide quality effect

Since breakdown is a dynamic process, the variations from sample to sample or even device to device on the same wafer can be large. The quality of the oxide has a pronounced effect on the breakdown behavior. To study the effect of oxide quality on BD, we prepared silicon oxides by two methods, thermal oxidation, which produces low defect concentration, and e-beam evaporation, which results in much higher defect concentrations. The negative bias breakdown results are shown in Fig. S3. For thermally grown oxides, the breakdown field has a much narrower distribution than for e-beam evaporated oxides. The current levels for thermal oxides with after breakdown are overall higher than of the more defective oxides.



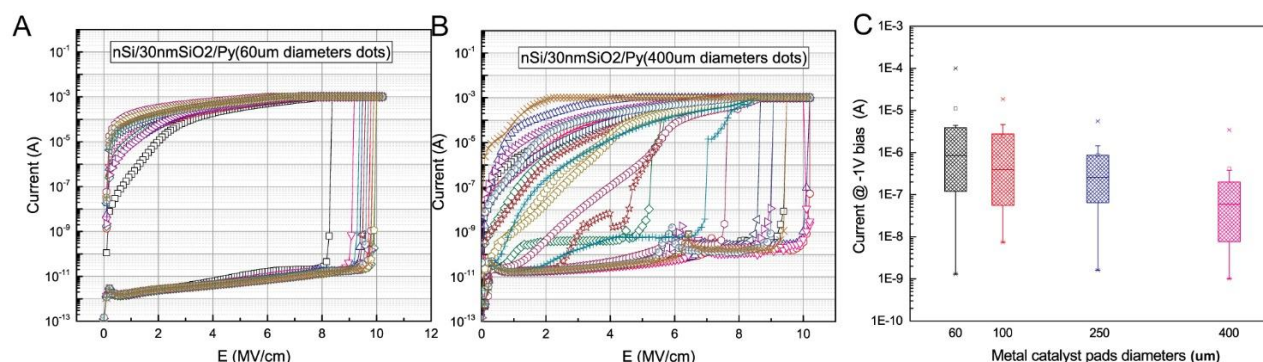
**Fig. S4** I-V characteristics of nSi/30nm thermal SiO<sub>2</sub>/Py devices after breakdown with different voltage sweep ranges, (A) -5 V ~ 5 V and (B) -1 V ~ 1 V.

### Read voltage range effect

After breakdown, robust device operation under extended cycling over the expected range of operating voltages is essential. Our previous work on resistive switching in intrinsic silicon oxides has shown that unipolar switching behavior occurs. Joule heating can disrupt the localized conducting path leading to a sharp decrease in electrical conduction during the reset process (15). As shown in Fig. S4(A), if the voltage is swept from -5 to 5 V, the power is high enough to produce joule heating and disconnect the filament, as indicated by the sharp decrease in current around 3 V. The current density is then reduced by one to two orders of magnitude when performing the 2<sup>nd</sup> sweep. If the sweep range is limited to -1 V ~ 1 V, as in Fig. S4(B), no decrease is observed after even 100 sweeps.

### Metal catalyst pad size effect





**Fig. S5** Breakdown voltage sweeps of I-V characteristics for nSi/30nmSiO<sub>2</sub>/Py with (A) 60 um and (B) 400 um diameter metal contact sizes. Different curves represent different devices. (C) Statistical distribution of electrical current at -1V bias after breakdown for metal pad diameters of 60 um, 100 um, 250 um and 400 um.

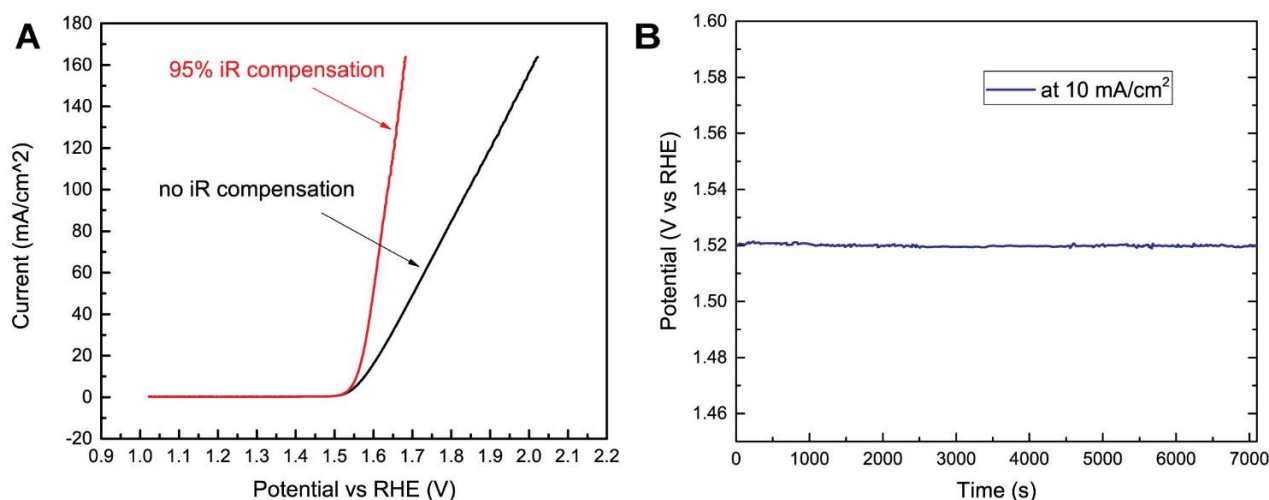
The proposed filament model assumes the formation of a localized conducting path underneath metal pads, in which case conduction should be independent of the pad size. Fig. S5(A) and (B) show breakdown curves for n-Si/30nmSiO<sub>2</sub>/Py with 60 um and 400 um diameter metal pads, respectively. There is a wide variations in BD field for 400 um diameter pads compared with those for 60 um pads, which we attribute to the increased number of defects for large pads. However, Fig. S5(C) shows that the electrical current at -1V after breakdown does not scale in proportion to the metal pad size, confirming the filament model. This results also suggests that the PEC performance can be improved by further reducing the metal catalysts sizes.

### III. Permalloy (Ni<sub>81</sub>Fe<sub>19</sub>) as OER catalyst

#### Preparation methods

Ni based OER catalysts have been studied extensively. The first study of the effect of Fe impurities in Ni-based catalysts on OER performance was by Corrigan *et.al.* in 1988 using electrodeposited catalysts(16). Since then, the majority of studies have used electrodeposition to prepare NiFe or NiFeO<sub>x</sub> catalysts. Besides electrodeposition, NiFe alloys have also been prepared by mechanically mixing metallic Ni and Fe into a NiFe alloy(17, 18). However, this method suffered from poor film quality.

In this work, Ni (99.995%, Alfa Aesar) and Ni<sub>81</sub>Fe<sub>19</sub> (99.95%, Alfa Aesar) films were directly deposited by e-beam evaporation (CHA Industries). The deposited thin films were polycrystalline(19), instead of amorphous structures prepared by mechanically mixing(20). The substrates were silicon wafers covered with 1600nm SiO<sub>2</sub>. During the deposition, a vacuum was maintained with a base pressure  $< 2.0 \times 10^{-6}$  Torr. A quartz-crystal monitor was used to monitor the deposition rates, which were kept at  $\sim 0.5$  Å/s. The total metal film thickness for both samples was 150 nm.



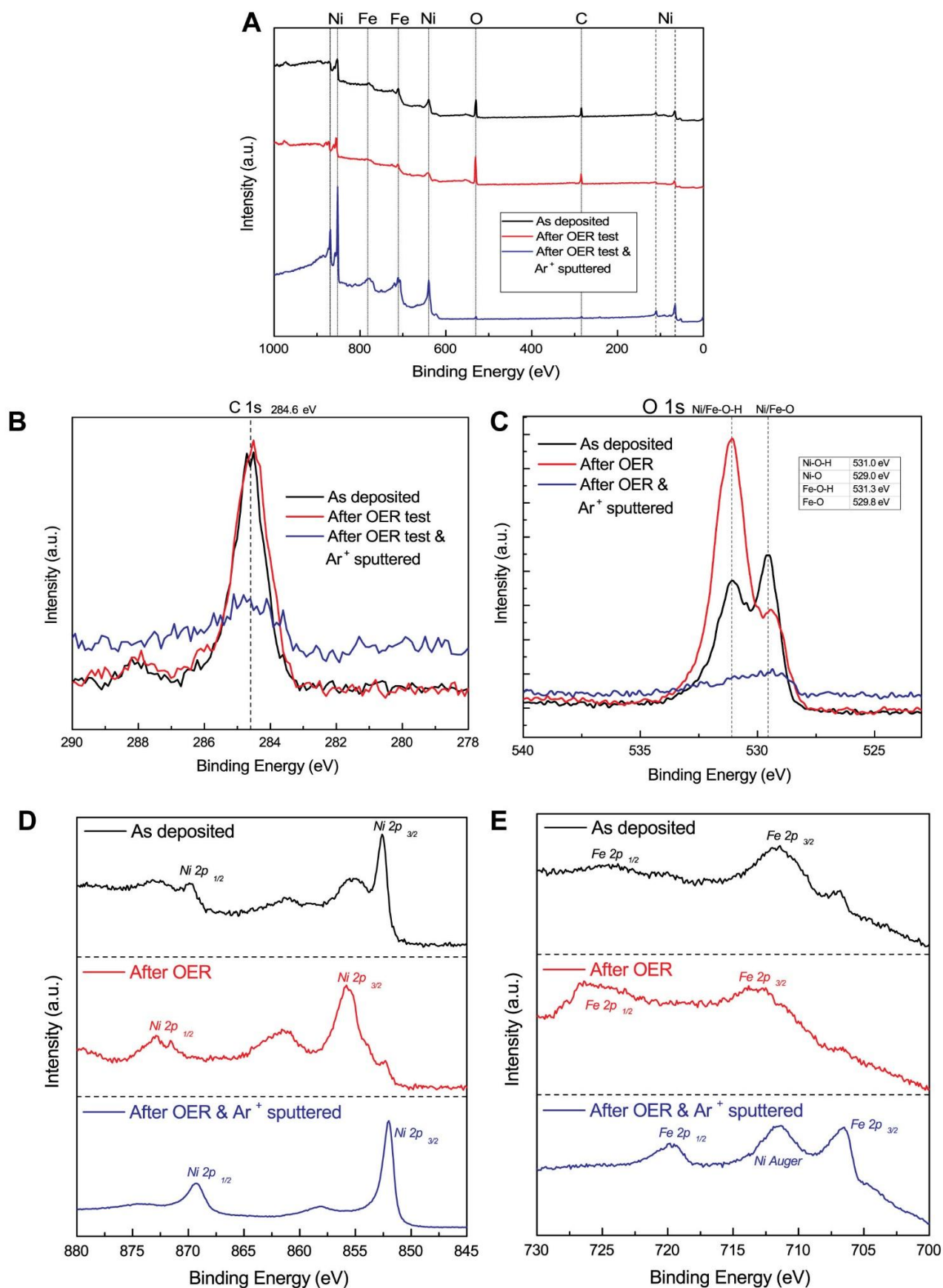
**Fig. S6** (A) Linear sweep voltammetry (LSV) with and without iR-compensation, and (B) 2 h chronopotentiometry (CP) of Ni<sub>81</sub>Fe<sub>19</sub> catalysts in 1M KOH. The scan rate for the LSV measurement was 5 mV/s and the current density for CP was at 10 mA/cm<sup>2</sup>.

### Electrochemical measurements

All electrochemical measurements were carried out with a CHI 760E electrochemical workstation (CH Instruments, Austin, United States) in a standard three-electrode electrochemical cell. A Pt wire and Ag/AgCl (3M KCL) were used as counter electrode and reference electrode, respectively. Deionized water with 18.1 MΩ resistivity was used to prepare a 1M KOH (semiconductor grade, Sigma-Aldrich, 99.99% trace metal basis) solution in which the OER characterization was carried out. All measured potentials were calibrated to RHE using the following equation:

$$E_{\text{RHE}} = E_{\text{Ag/AgCl}} + 0.197 \text{ V} + 0.059 \times \text{pH} - iR_u \quad (1)$$

where  $R_u$  is the uncorrected resistance. The prepared electrodes were cycled ~100 times by cyclic voltammetry (CV) until stable CV curves were obtained. The electrolyte resistance was measured to be 11.1 Ω by the AC impedance method, which is a typical value for high concentration KOH solutions. Linear sweep voltammetry (LSV) of Ni<sub>81</sub>Fe<sub>19</sub> with and without iR-compensation is shown in Fig. S6 (A). Fig. S6(B) shows a chronopotentiometry measurement of Ni<sub>81</sub>Fe<sub>19</sub> for 2 h held at a constant current density of 10 mA/cm<sup>2</sup>. No degradation was observed.





**Fig. S7** XPS characterization of catalyst films (A) Survey scan, (B) C 1s and (C) O 1s (D) Ni 2p and (E) Fe 2p high resolution scan of Ni<sub>81</sub>Fe<sub>19</sub> catalysts under different conditions: as deposited, after OER test and after OER and 60 s Ar<sup>+</sup> sputtering. The sputter etch rate was approximately 0.5 nm/s. The OER test included 100 cycles CV, Tafel test and 2h chronopotentiometry at a constant current density of 10 mA/cm<sup>2</sup>.

### X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) was performed on a Kratos Axis Ultra spectrometer XPS system. The spectra were acquired using a monochromatic Al K<sub>α</sub> source with a base pressure of 10<sup>-9</sup> Torr. Charge neutralization was used during spectrum acquisition for all measurements. A survey scan (0-1000 eV) was performed first to determine the elemental composition, as shown in Fig. S7(A), indicating the presence of Ni, Fe, O and C. High resolution spectra of the C 1s, Ni 2p, Fe 2p and O 1s peaks were then obtained with dwell times from 500-1500 ms. The C 1s peak (284.6 eV) was used for charge correction, as shown in Fig S7(B). The presence of carbon resulted from surface contamination, as ion-sputtering of the sample surface resulted in the removal of the carbon peak. The as deposited sample exhibited a mixture of Ni/Fe hydroxides and Ni/Fe oxides. After the OER test, which included cycled CV (activation process of catalysts), Tafel test and 2h chronopotentiometry, most oxide states were transformed to hydroxide states. The O 1s spectra in Fig. S7(B) also confirm the large ratio of hydroxides to oxides, which accords well with recent findings that, under potential cycling in alkaline solutions, the oxide phase slowly transforms to Ni(OH)/NiOOH, which are active sites for OER. For samples after OER test and Ar ion sputtering, the carbon and oxygen peaks are greatly reduced. This confirms that only the surface is oxidized, film is well protected, and expected to maintain high conductivity.

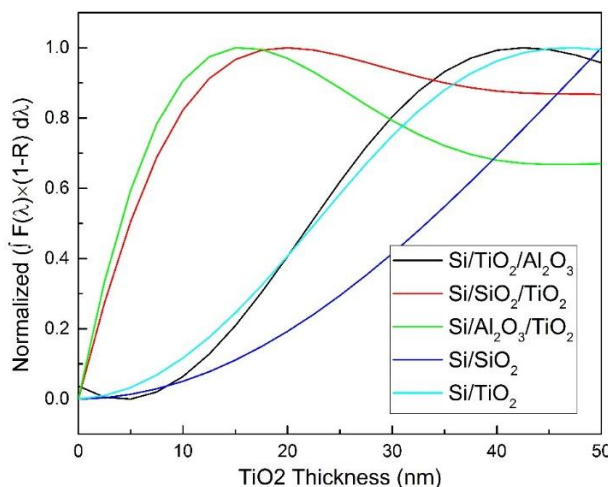
**Supplementary Table S1** Benchmarks of OER catalysts in KOH with a current density of 10 mA/cm<sup>2</sup>.

Materials	Electrolyte	$\eta$ /mV	Reference
NiFe(permalloy)	1 M KOH	300	This work
NiFe-LDH/3D Ni foil	1 M KOH	215	Ref(21)
Co <sub>3</sub> O <sub>4</sub> /Graphene	1 M KOH	310	Ref(22)
Ni <sub>0.9</sub> Fe <sub>0.1</sub> O <sub>x</sub>	1 M KOH	336	Ref(23)
IrO <sub>x</sub>	0.1 M KOH	380	Ref(24)
RuO <sub>x</sub>	0.1 M KOH	390	Ref(24)
Mn oxide	0.1 M KOH	540	Ref(24)
Mn <sub>3</sub> O <sub>4</sub> /CoSe <sub>2</sub>	0.1 M KOH	450	Ref(25)
NiFe-LDH/CNT	1 M KOH	247	Ref(26)

#### IV. Antireflection Functionality

##### Simulation methods

Numerical simulations were performed using the Rsoft Diffractmod software package (Rsoft Design Group, Inc. Ossining, NY, USA). A plane wave is used as light source perpendicular to the sample surface. The global environment was set as water to mimic the real condition of PEC measurements.



**Fig. S8** Normalized integration of  $(1-R)$  over the solar spectrum.  $R$  is reflection as a function of wavelength  $\lambda$ . The total thickness of oxides for all samples are fixed to 50 nm, and optical absorption in the oxide is assumed to be negligible over the wavelength range of interest.

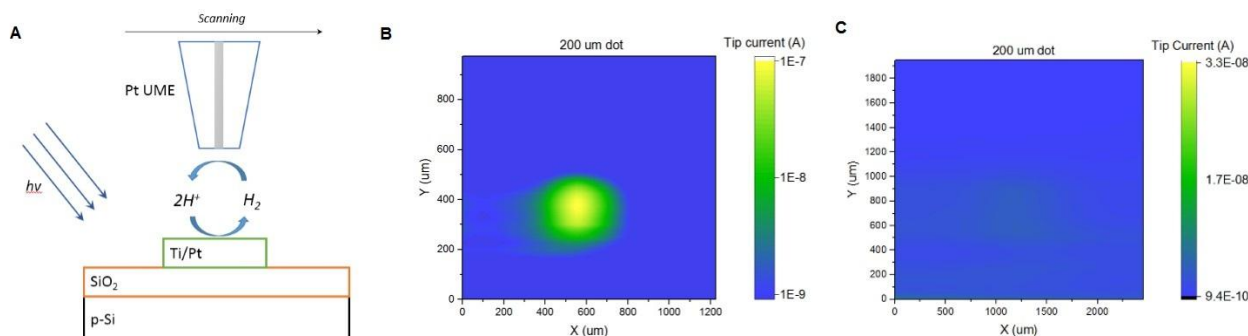
##### Optimized thickness combination

The optimized thickness combination can be obtained by maximizing the optical absorption  $A$ , given by:

$$A = \int F(\lambda) \times (1 - R(\lambda)) d\lambda$$

where  $F(\lambda)$  is the solar spectrum and  $R$  is the reflectance. Fig. S8 shows the normalized results and the thicknesses at maximum values are the optimized thicknesses.

## V. PEC characterizations



**Fig S9.** (A) Schematic of SECM setup. The ultramicro electrode is 10 μm Pt UME. Light is from side of sample and is not calibrated. (B) and (C) are SECM mappings of a 200 μm dot with different breakdown treatment for p-Si/30 nm SiO<sub>2</sub>/30 nm Ti/20 nm Pt sample. (B) is for device with high conductivity after breakdown and (C) is for device with low conductivity after breakdown.

### Results

Fig S9 (A) is the schematic of SECM measurements. The tip of an untramicroelectrode (10 μm Pt UME) is positioned close to the surface of the working electrode, while its potential is held more positive than the RHE for H<sub>2</sub> evolution. The tip oxidation current is a measure of the rate of local H<sub>2</sub> evolution. To eliminate influence from adjacent dots, the metallic catalysts is patterned to 200 μm diameter dots with spacing of 1600 μm. To avoid dramatically bubble generation on surface, which would block the tip current, a small bias is applied to the substrate. Two devices were pre-treated to present different conductivity. Device in Fig. S9 (B) has 1 mA/cm<sup>2</sup> current density in dry I-V measurements at 1 V bias. In SECM mapping, we can see clearly the hydrogen evolution on metal pads. In comparison, device in Fig. S9 (C) has 1 μA/cm<sup>2</sup> current density in dry I-V measurements. And in SECM mapping, no obvious hydrogen evolution is observed.

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