Improved Performance of Zinc Oxide Thin Film Transistor Pressure Sensors and a Demonstration of a Commercial Chip Compatibility with the New Force Sensing Technology

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A zinc oxide thin film transistor is developed and optimized that simultaneously functions as a transistor and a force sensor, thus allowing for scalable integration of sensors into arrays without the need for additional addressing elements. Through systematic material deposition, microscopy, and piezoelectric characterization, it is determined that an O_2 rich deposition condition improves the transistor performance and pressure sensing characteristics. With these optimizations, a sensitivity of 4 nA kPa^{-1} and a latency of below 1 ms are achieved, exceeding the criteria for successful commercialization of arrayed pressure sensors. The functionality of 16 × 16 pressure sensor arrays on thin bendable glass substrates for integrated low weight and flexible touchscreen displays is fabricated and demonstrated and read-out electronics to interface with the arrays and to record their response in real-time are developed. Finally, the application of these sensors for mobile displays via their operation with an existing commercial touch integrated circuit controller is demonstrated.

1. Introduction

Recently, there has been a lot of interest in developing new pressure sensing techniques, such as piezotronic sensors,[1] rubrene-based transistors with microstructured gate electrodes,[2] microelectromechanical systems with strain gauges,[3] and other methods.[4,5] With the introduction of force sensing into mobile handheld devices, it becomes critical to develop force sensing solutions that are scalable, thin, light, and cost-effective. Force sensing functionality has been pursued using various methods that include strain sensors,[6] light emitters and detectors,[7] and surface acoustic wave sensors among others.[8–11] A powerful approach in pressure sensor development is the incorporation of both pressure sensing and switching functionalities into a single array element.[12] This allows the use of miniature sensor elements with high sensitivity and scalability to large areas. Zinc oxide (ZnO) is semiconducting, suitable for transistor fabrication in a vertically integrated process, transparent, and has a high piezoelectric coefficient that confers excellent pressure sensitivity,[13,14] positioning it as a forefront candidate for integration into in-cell touchscreen technologies.[15] A large portion of the emerging display technologies use materials based on ZnO, such as indium gallium zinc oxide (IGZO).[16,17] In addition, amenability to low temperature processing allows the ZnO pressure sensor arrays to be seamlessly integrated into pressure display technologies.

When pressure is applied on top of a sputtered ZnO film, the net dipole moment in the *c*-direction is distorted, leading to accumulation or depletion of free charge carriers at the surface of the device.[18] The pressure-induced free charge carriers lead to a change in the drain current, with the magnitude of change being proportional to the applied pressure. In a field-effect transistor (FET) configuration, small pressures applied to the gate can lead to large drain current changes, especially when the transconductance of the ZnO FET is high. Vishniakou et al. reported the fabrication of 8×8 ZnO thin film transistor (TFT) arrays on rigid glass, with good pressure sensing characteristics.[12] However, their I_{on}/I_{off} ratio was lower than 10^3, and the piezoelectric properties of the films were not explored in detail. For good transistor performance, the unintentionally doped ZnO films, usually n-type due to O_2 vacancies and impurity donors, need to be compensated to achieve low leakage currents. Further, the film grains in the ZnO layers need to be

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/admt.201700279.

DOI: 10.1002/admt.201700279

aligned with their *c*-axis perpendicular to the surface of the substrate and to sustain a single surface polarity (O- or Zn-termination) in order to have a fixed net dipole moment and to achieve high pressure sensitivity. In this work, we report the optimization of ZnO TFT pressure sensors on thin flexible substrates for integrated low weight and flexible touchscreen displays. We systematically investigated a variety of ZnO thin film growth conditions including the introduction of a seed layer for better film uniformity, different sputtering gases during film growth, and higher temperature during the sputtering process. We utilized X-ray diffraction (XRD), transmission electron microscopy (TEM), scanning electron microscopy (SEM), piezoresponse force microscopy (PFM), and FET measurement techniques to optimize the growth conditions and utilized these conditions to fabricate pressure sensor arrays that were interfaced with a commercial touchscreen integrated circuit (IC) controllers.

2. Results and Discussion

In seeking the optimal ZnO film quality for FET pressure sensitivity, there are several constraints on the deposition that need to be considered. First, the ZnO film needs to be coalesced to maintain in-plane conductivity, yet still thin enough to maintain good electrostatic control of the channel. We determined that a 60 nm film meets these considerations (Figure S1, Supporting Information). Second, the deposited film needs to exhibit good crystalline quality with a *c*-axis growth direction normal to the substrate in order to exhibit acceptable piezoelectric response. Additionally, the deposition rate needs to be moderate to maintain good film quality and cost-effictiveness of the process and the deposition temperature should be compatible with display technologies on rigid and flexible substrates. We determined that the deposition of a 6 nm thick seed layer at room temperature followed by the deposition of 54 nm at 200 °C satisfies these constraints (Figures S2 and S3 and Table S1, Supporting Information). Third, the deposited ZnO layer needs to be moderately n-doped to enable excellent pinch-off characteristics and smaller power dissipation in the off-state. It is known that O_2 vacancies and unintentional dopants such as hydrogen exhibit donor characteristics and lead to elevated levels of free carriers. The flow of O_2 during sputtering can compensate these vacancies or prevent impurities from entering the lattice, as was suggested by Janotti and Van de Walle,[19] and result in semiconductive films that can have better pinch off characteristics. Recent studies of IGZO have reported similar effects.[20,21] We therefore conducted the sputtering of ZnO films in O_2 and N_2 environments and characterized their piezoelectric performance.

The morphologies of the ZnO thin films sputtered with either O_2 or N_2 gas with or without a seed layer are shown in **Figure 1**. The SEM images reveal larger, irregularly distributed grains on the ZnO film grown without a seed layer and with N_2 gas (Figure 1a). The two conditions for growth with the seed layer resulted in a more uniform film, where the best uniformity, albeit with smaller grain sizes, was achieved with O_2 with a seed layer (Figure 1c). The XRD scans of Figure S4 (Supporting Information) show the highest peak for the ZnO:N_2 with no seed layer. However, the O_2 film grown with a seed layer (Figure 1c) has higher *c*-axis peak compared to the N_2 film with seed layer (Figure 1b). The cross-sectional TEM images (Figure 1d–f) also confirm the better uniformity and film density of the O_2 with seed condition. The fast Fourier transform (FFT) for the three cross-sections are also in agreement with the morphological and XRD results. The FFT in Figure 1d illustrates that the no-seed condition resulted in a crystalline ZnO film. With a seed layer, the N_2 condition resulted in a polycrystalline ZnO film (FFT in Figure 1e) and the disorder in grain alignment seems to be lower with O_2 flow (FFT in Figure 1f). These results suggest a compromise in the deposition conditions for ZnO pressure sensing FETs. While N_2 flow with no seed layer resulted in single crystal aligned ZnO grain growth in the *c*-direction, the rough surface morphology can lead to degraded electron mobility, gate-leakage currents, and weaker gate control. In addition, the high conductivity in the ZnO films grown with N_2 flow lead to large source–drain leakage currents as will be discussed below. On the other hand, the compromised ZnO grain alignment in the *c*-axis for films grown with O_2 flow have smoother surfaces that are better fit for FET operation. The compensation for O_2 vacancies in ZnO with O_2 flow during the growth results in donor level compensation and lower n-type conductivity and a better gate modulation, leading to lower source–drain leakage.

To characterize the piezoelectric response of the ZnO films, we conducted PFM measurements and evaluated the piezoelectric coefficient, d_{33}, which quantifies the voltage build-up across a piezoelectric material under strain. The effective constant, d_{33}^{eff}, was calculated by measuring the vertical deflection of the AFM tip with applied voltage and characterizes the average piezoresponse normal to the surface.[22,23] The details of the measurement are provided in the Experimental Section and the results are summarized in **Figure 2** and **Table 1**. The ZnO:N_2 with no seed sample exhibited the largest d_{33}^{eff}, which is expected based on the fact that the largest grain alignment in *c*-orientation is observed in these films, using both TEM and XRD. This sample also exhibited the largest standard deviation because of the sharp height changes that are evident from the SEM images in Figure 1. The ZnO:N_2 with seed layer exhibited a lower d_{33}^{eff} constant compared to that with no seed layer due to misalignment of the vertical grains. The ZnO:O_2 with seed exhibited an acceptable d_{33}^{eff}, which is the lowest in the studied samples, and a relatively lower standard deviation. Earlier studies on ZnO reported a value of d_{33} for bulk films of 9.93 pm V^{-1}, and of 14.3–26.7 pm V^{-1} for nanostructures,[24] our results are close to the bulk value. Overall, the d_{33}^{eff} values obtained from ZnO deposited under all conditions are suitable for pressure sensing. The phase data of the PFM measurements additionally reveal that the films are predominantly single phase. Multiphase films are expected to have a bimodal distribution of phases in the piezoresponse phase image, however, Figure 2 shows a predominantly single-phase distribution of values in the films. For appropriate FET performance discussed below, we utilized the ZnO films deposited with O_2 flow and with a seed layer.

Although the highest measured d_{33}^{eff} value was observed for the ZnO film with N_2 and no seed layer, the final pressure sensitivity is proportional to the product of the transconductance g_m at the bias point, and the piezoelectric coefficient d_{33}. Therefore, a ZnO film with a higher piezoelectric response may

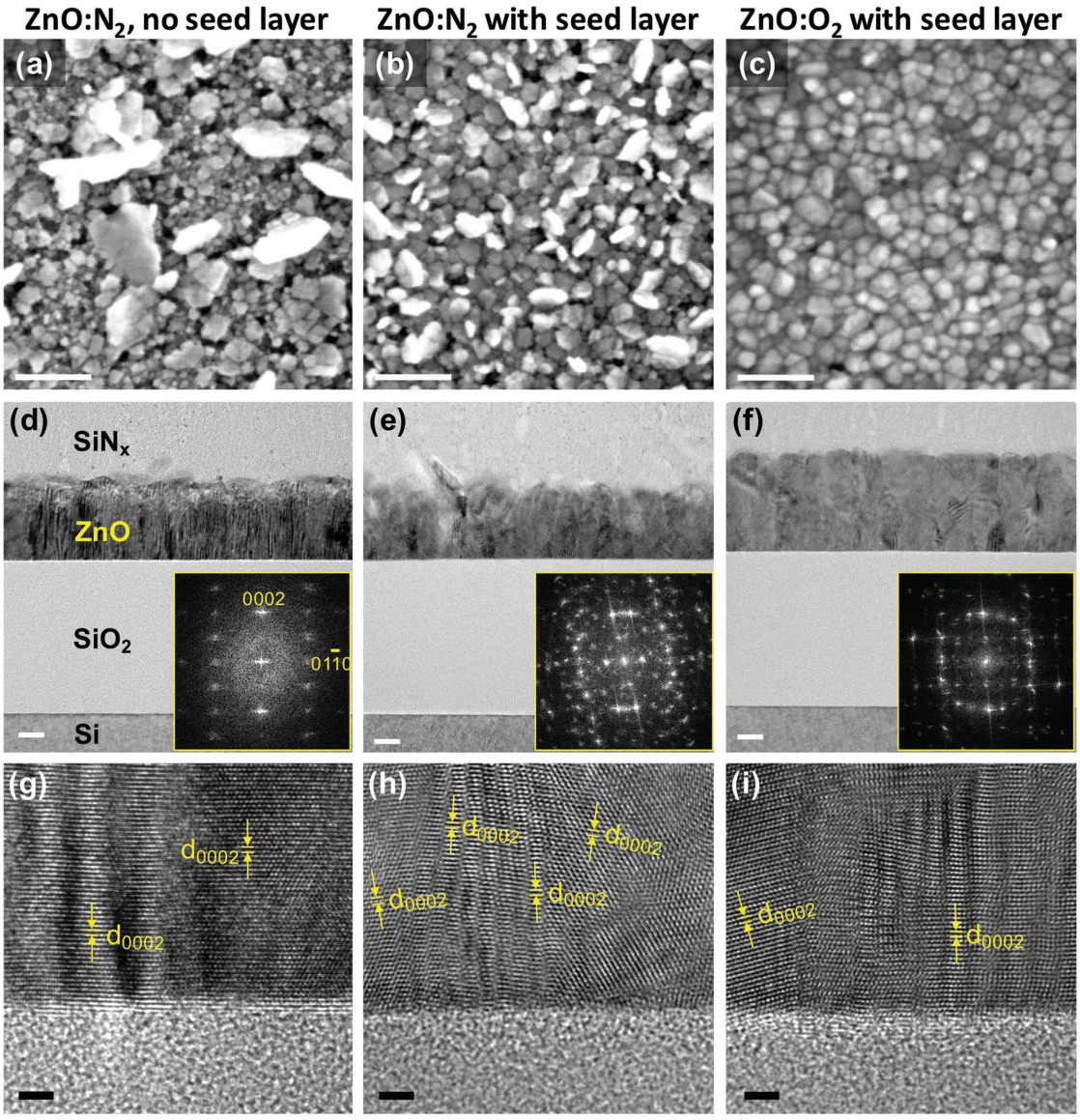

Figure 1. Morphology of ZnO films with different deposition conditions. a–c) Top view SEM images of the ZnO films. d–f) Cross-sectional TEM images and their corresponding FFT spectra of the ZnO thin films. g–i) HRTEM of the ZnO thin film. The various growth conditions are arranged in the respective columns. (a), (d), (g) ZnO:N_2 film grown without seed layer. (b), (e), (h) ZnO:N_2 film grown with a seed layer. (c), (f), (i) ZnO:O_2 film grown with a seed layer. Scale bars are 100 nm for (a)–(c), 20 nm for (d)–(f), and 2 nm for (g)–(i).

not necessarily exhibit superior performance when used as a channel material for a pressure-sensing thin-film transistor. Moreover, parameters such as the off-current, operating voltages, and ease of fabrication should also be taken into account when selecting the films for practical applications. We determined that the film grown with a seed layer at 200 °C using oxygen gas during sputtering produces the best pressure-sensing behavior.

The fabrication process of the ZnO TFTs accounted for a variety of layer interdependencies and the potential for sample degradation at each stage. The details of the fabrication process are reported in the Experimental Section and summarized in **Figure 3**. Two atomic layer depositions (ALDs) were incorporated, one (Figure 3b) for passivation of the ZnO surface directly after sputtering – which undergoes an etch for channel definition – and one (Figure 3d) for establishing a thick-enough gate dielectric that prevents gate-to-channel leakage and enables good electrical insulation of the gate-to-source and gate-to-drain overlap regions (Figure 3e). The active regions of the device are composed of ITO source/drain/gate electrodes with Ti/Au metal pads for probing.

ZnO TFTs were fabricated side by side for all ZnO films discussed in Figures 1 and 2. The ZnO TFTs made on samples sputtered with only N_2 gas were highly conductive and exhibited weak gate modulation (Figure S4, Supporting Information). The ZnO TFTs that were fabricated on films deposited with O_2 flow exhibited better pinch-off characteristics as shown in **Figure 4**. The transfer characteristics shown in Figure 4a

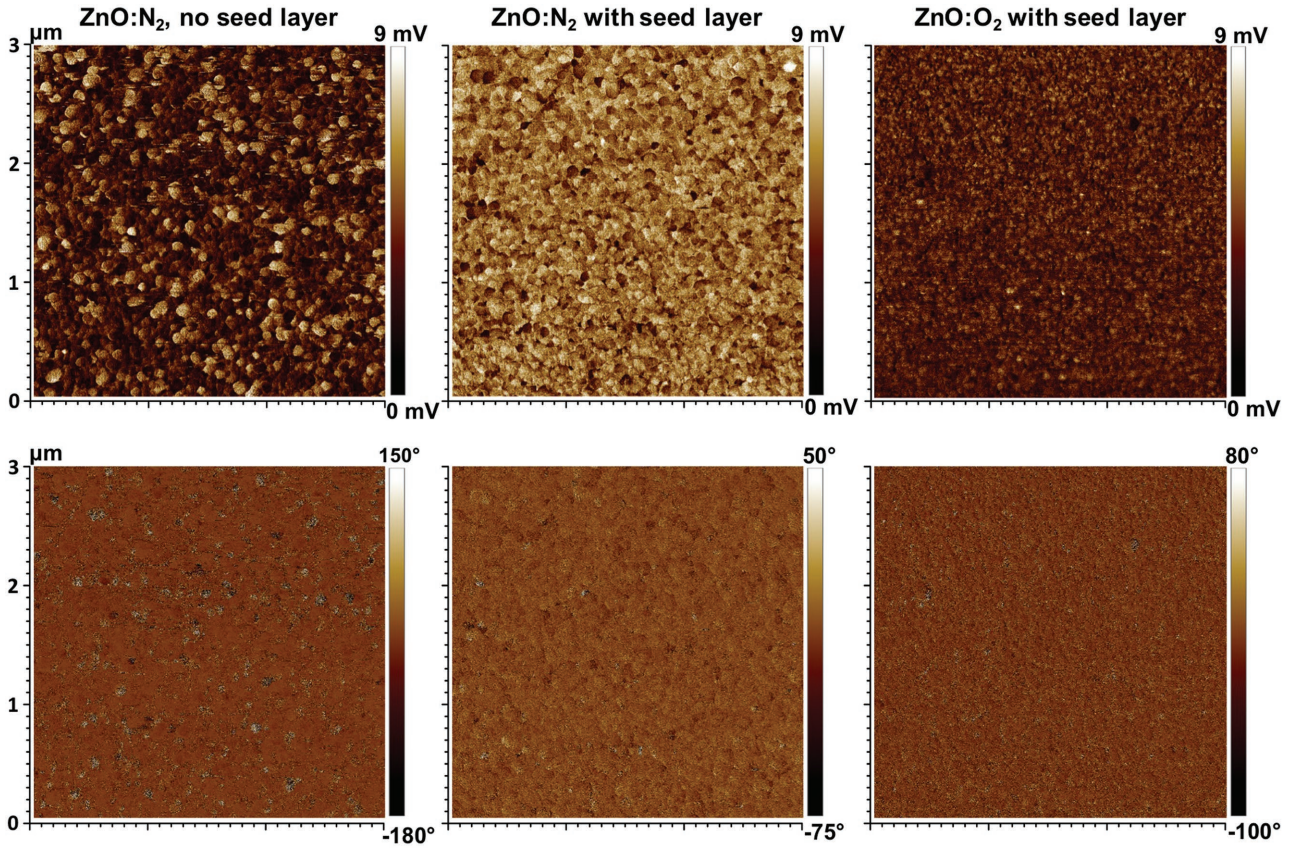

Figure 2. PFM scans of the ZnO thin films. Top images: Piezoresponse amplitude of the films. The units are arbitrary and are provided for comparison across samples. Bottom images: Piezoresponse phase of the films. Left column: ZnO:N_2 film grown without a seed layer. Middle column: ZnO:N_2 film grown with a seed layer. Right column: ZnO:O_2 film grown with a seed layer.

exhibit saturation with modest output conductance at high gate voltages due to the series contact resistance that becomes non-negligible with respect to the channel conductance at high V_{GS}. The transfer curves showed good modulation with $\approx 10^5$ I_{max}/I_{min} ratio over a V_{GS} range of 20 V. The Al_2O_3 dielectric thickness for these devices was 100 nm. A better gate transconductance and therefore a smaller gate voltage range can be achieved with a thinner gate dielectric.

With the optimized ZnO TFT performance, the pressure sensitivity of the single TFT devices was characterized using the experimental configuration shown in **Figure 5**a. These devices had additional processing condition differences than those of Figure S5 (Supporting Information), including ITO contacts and thermal ALD of Al_2O_3 at 200 °C as opposed to e-beam evaporated Al contacts and plasma ALD at 130 °C for devices of Figure S5 (Supporting Information). The highest pressure sensitivity can be obtained by biasing the transistors at the maximum transconductance point, which can vary from one element to the other in the TFT array. Here, we biased our ZnO TFTs in the saturation regime to preclude device sensitivity to noise. The pressure applied to the ZnO channel leads to the accumulation of electrons at the channel surface, thereby increasing the drain current. We can therefore quantify the sensitivity of the device in terms of either current increase with pressure (nA kPa^{-1}), or the apparent gate voltage that is needed to change the drain current by the same amount obtained with applying pressure, yielding an effective sensitivity in units of mV kPa^{-1}. We first measured the drain current as a function of time for different pressure values to extract the amount of current change. A stage is placed over the sample (Figure 5a), and weights are added on top of the stage sequentially. The applied pressure can be calculated using the contact area of the stage with the sample. We then extracted the change of drain current as a function of the added pressure onto the TFT and plotted it in Figure 5b (bottom gate) and Figure 5d (top gate). The I_{DS}–V_{GS} characteristics were then used to estimate the effective gate voltage required to induce an equivalent current change in the device as shown in Figure 5c,e. To conduct bottom gate and top gate measurements on the same device, we fabricated the devices on a Si/SiO_2 substrate with the same material structure and processing conditions as those fabricated on glass and used the Si substrate as the bottom gate electrode. The sensitivity of the ZnO TFT to pressure is nearly equivalent for both

Table 1. Measured effective piezoelectric coefficients for different ZnO deposition conditions.

Sample	d_{33}^{eff} [pm V^{-1}]	Std. Dev.	Std. Dev. [%]
ZnO:N_2 with no seed	10.46	7.72	73.8
ZnO:N_2 with seed	6.44	4.80	74.6
ZnO:O_2 with seed	5.43	3.84	70.6

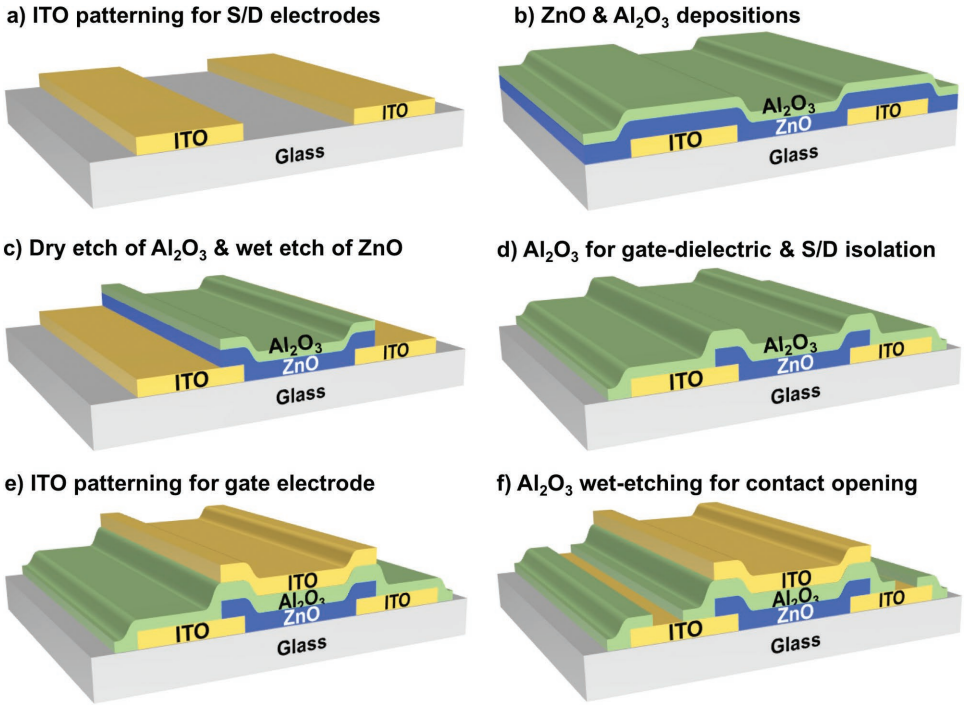

Figure 3. Fabrication process of the ZnO TFT pressure sensors. a) ITO source/drain electrode deposition on a glass or a SiO_2/Si substrate. b) ZnO sputter deposition, followed by ALD Al_2O_3 passivation. c) Al_2O_3 dry etching to create an etch mask for ZnO channel followed by ZnO wet etching. d) Al_2O_3 gate dielectric deposition by ALD. e) Gate electrode sputter deposition. f) Al_2O_3 etching to open drain and source contacts.

bottom and top gate bias and increases with V_{GS}. The equivalent voltage change due to applied force is a film property, not a device configuration property, because the voltage change is only dependent on film mobility and the d_{33}^{eff} constants. The overall device performance compared to the first generation devices reported elsewhere[12] is summarized in Table S2 (Supporting Information).

Besides sensitivity, the latency of a force sensor is a critical parameter, especially for touch applications. It is defined as the time of response for the sensor to detect the presence of pressure. Humans are very sensitive to touch delays and can even perceive a low latency of 10 ms.[25] To measure the latency of our devices, we positioned a stage on top of the pressure sensor, and added the current readout to an oscilloscope. The second channel of an oscilloscope was connected to a standard analog microphone. We characterized the latency by physically hitting the stage of the force sensor with the microphone. Upon impact, the microphone reports a change in voltage. The results are shown in Figure S6 (Supporting Information), where it can be seen that the two signals follow each other with less than 1 ms of delay. Therefore, the upper bound of the latency of the ZnO TFT pressure sensors is 1 ms.

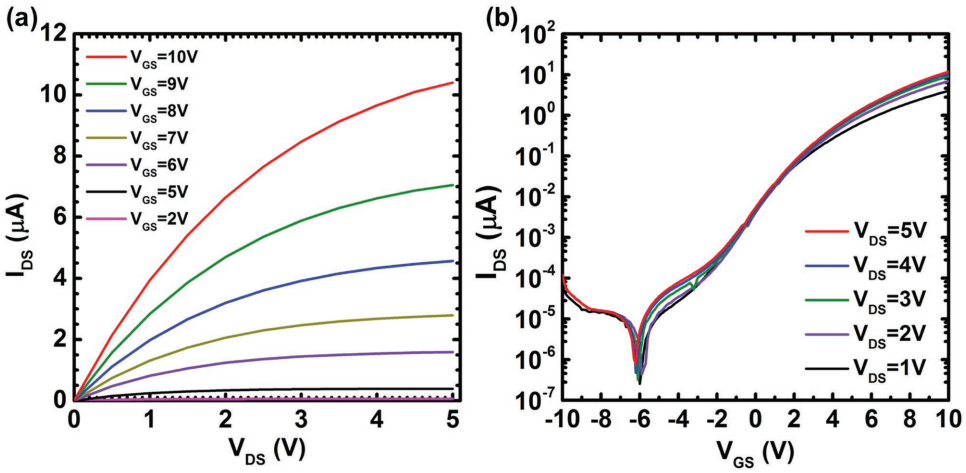

Figure 4. Field effect transistor characteristics of ZnO TFT. a) I_{DS}–V_{DS} curves under various gate voltages. b) I_{DS}–V_{GS} under different V_d biases.

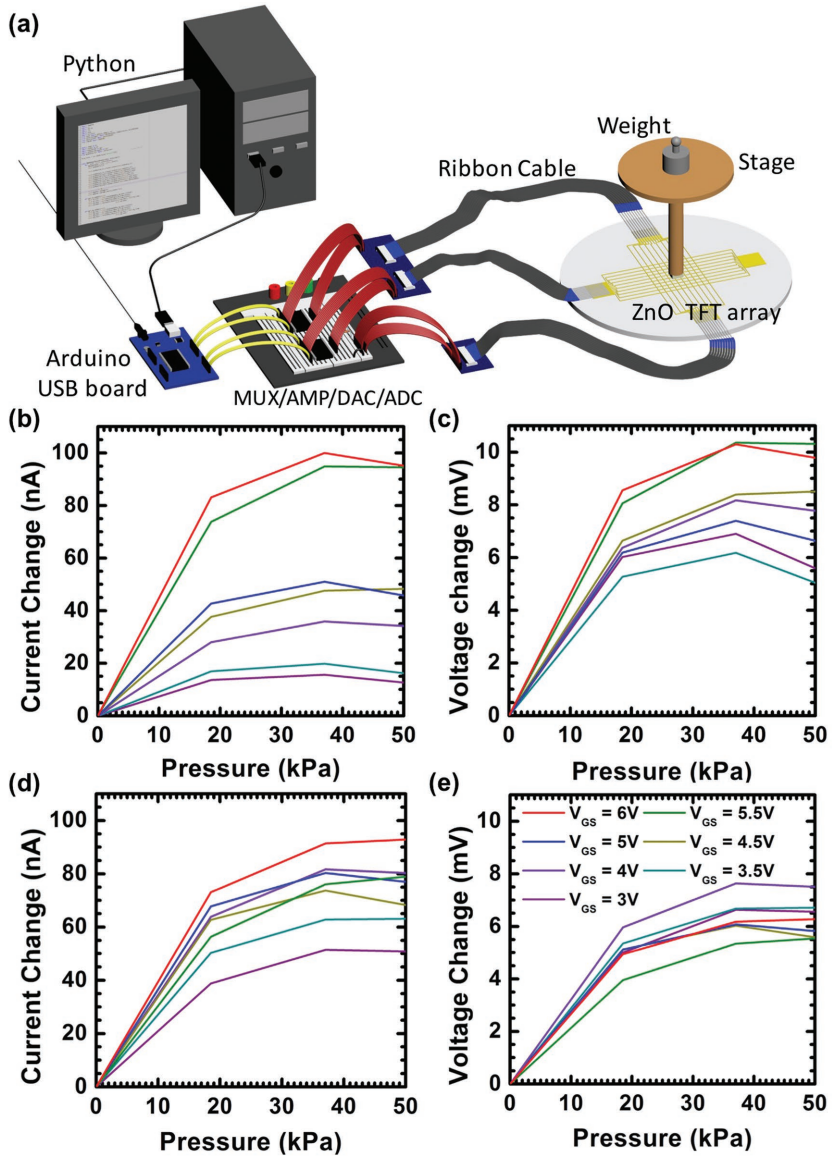

Figure 5. Drain current measurement. a) Illustration of ZnO:O_2 device pressure–current measurement setup. b) Drain current change measured as a function of pressure (bottom gate) for different gate voltages. Panels (b)–(e) share the same V_{GS} legend of panel (e). c) Extracted effective gate voltage change needed to cause the current (bottom gate). d) Drain current measured change as a function of pressure (top gate). e) Extracted effective gate voltage change needed to cause the current (top gate).

With these parametric characterizations, we designed and built a 16 × 16 pressure sensor array with a 1.5 mm sensor pitch on a 3 in. thin flexible Corning glass with 100 µm thickness, shown in **Figure 6**a,b. We built a custom array readout circuit to demonstrate the initial device operation. Figure 6c shows the 3D maps of drain current change at various times during the device operation. At $t = 0$, there is no pressure applied, and the current is in its initial distribution, as shown in Figure 6c. When an object is pressed in the center of the array (Figure 6b), current starts to increase in the area where the object is pressed, as shown in Figure 6d, and a full peak is developed soon after, as demonstrated in Figure 6e. This setup allows the measurement of 1 frame per about 1.5 s, due to the autoranging circuit function, serial communication delay, and bidirectional communication between microcontroller and host. Different approaches such as an FPGA used for current measurement and DAC/ADC communication together with a USB-based communication can allow for higher speeds.

Finally, our sensor arrays can be interfaced with a commercially available touchscreen IC driver that is currently being used in cell phones. The touch IC chip has been software reconfigured to be compatible with our sensors. The drive lines of the touch IC chip were used as the gate electrodes to select the active row of the array for measurement. The sense lines of the touch IC chip were connected to the drain electrodes. Our custom in-house built readout circuit had only one active component for current measurement. As a result, the entire array was multiplexed through a single measurement point, which significantly reduced the scanning frequency. Using a commercial chip, each drain/source electrode had a dedicated measurement circuit, which allowed to achieve a refresh rate of ≈13 Hz. The results for single and multiple point pressing are presented in **Figure 7**b,c, respectively. The scanning rate can be further increased to the typical 60 Hz in touchscreen operating frequency by reducing the input capacitances of gate-to-channel and source-to-drain. With the recent interest in integration of force sensing technologies into smartphone displays, the ZnO TFTs provide an excellent opportunity for embedding force sensors into the smartphone displays. The standard deposition techniques such as sputtering and photolithography used in our process are compatible with existing manufacturing equipment for displays, which could lower the barrier to adoption of this new technology.

3. Conclusion

In this paper, we have demonstrated an array of scalable, high-performance solid state force sensors fabricated on thin bendable glass wafers. The sensors are based on zinc oxide thin film transistors and can be easily scaled into large arrays due to the simultaneous operation of each sensor as a switch. We have optimized the film properties to achieve a high on–off ratio of the transistors, excellent pressure sensitivity, and a latency of less than 1 ms. The effective mobility of the ZnO film is 2.7 $cm^2\ V^{-1}\ s^{-1}$, which suggests that there remains significant potential to improve the device temporal performance and

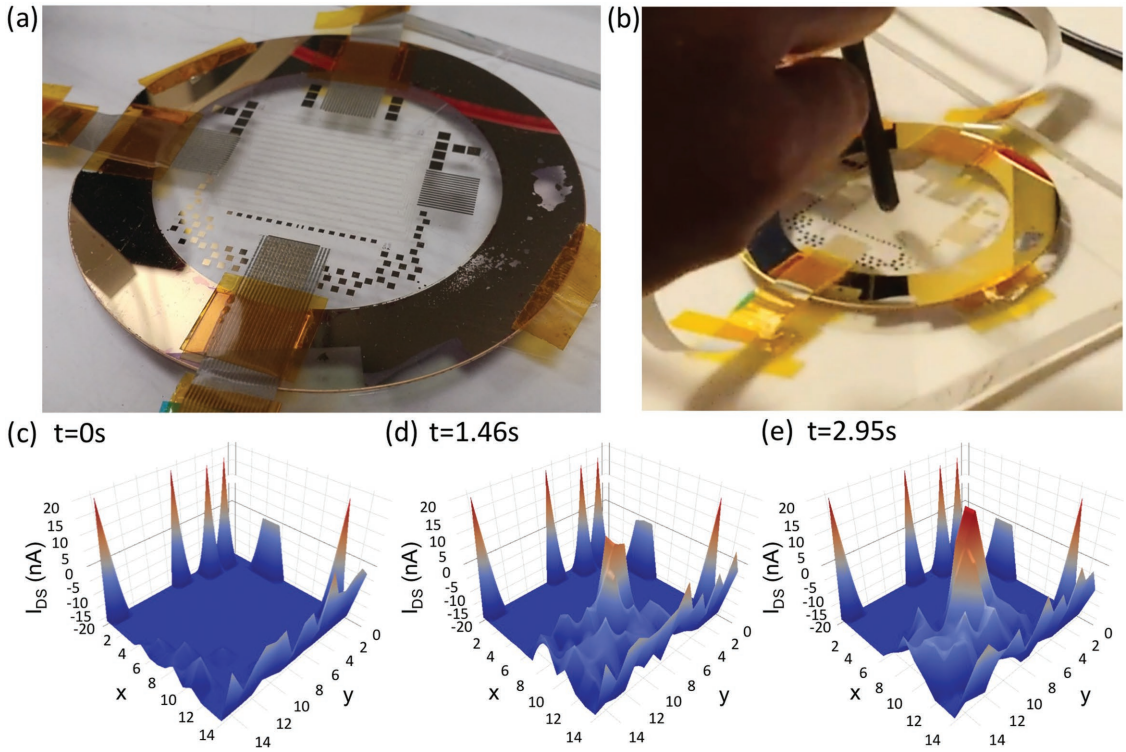

Figure 6. Pressure sensor array measurements. a) 16 × 16 pressure sensor array fabricated on a glass substrate with bonded electrodes. b) A nonconductive object pressing in the center of the array. c) 3D map of the drain current change prior to the pressure application. d,e) 3D maps of the drain current change during pressure application, at times 1.46 and 2.95 s, respectively.

sensitivity. To further demonstrate the commercial viability of the sensors, we have successfully interfaced our sensor array to an existing and shipping touchscreen driver IC.

4. Experimental Section

Device Fabrication and Characterization: For device fabrication, either thermally grown SiO_2 on highly doped Si wafers, or bendable 100 µm thick glass slides (Corning Inc.) were used. For the Si/SiO_2 wafers, highly doped n-type Si wafers were oxidized using dry oxidation in a furnace to a thickness of 100 nm. Next, source and drain layers were defined by first depositing ITO of ≈100 nm thickness using Denton Discovery 18 sputtering tool for 6 min, power of 300 W, Ar gas flow of 50 sccm, and a chamber pressure of 4.7 mT. The stage was rotating at 65 rpm. The pattern was etched using a positive photoresist (AZ1518) in a solution of 1:9 $HCl:H_2O$ for 1 min. After resist removal, the active ZnO layer was grown on top of the source/drain layer using AJA RF sputtering tool. ZnO was deposited in one or two stages, depending on the experiment. The first stage consisted of seed layer growth, which was done for 2 min at 100 W power at room temperature. The second stage layer was grown for 33 min at 100 W at 200 C. The sputtering gas varied based on the experiment. Next, a capping layer of Al_2O_3 was grown by ALD using Beneq TFS200. The machine was used in thermal mode at 200 °C, and the dielectric was grown in 100 cycles of TMA and H_2O pulses. Next, the Al_2O_3 layer was dry etched with a positive photoresist mask in Oxford Plasmalab 80+ reactive ion etching (RIE) system. The etching was done for 3 min with CF_4 and CHF_3 gases with the flows of 30 and 20 sccm, respectively, at 250 W power and 25 mT chamber pressure. Next, ZnO layer was etched in a dilute HCl solution of 1:1000 $HCl:H_2O$ for 30 s. After the channel was defined, gate dielectric of Al_2O_3 was grown to a thickness of 100 nm with an ALD as described above, with 1000 cycles of growth. Finally, a gate electrode was created by first growing 100 nm thick ITO layer by sputtering, then wet etching using the same process as for source/drain layer. To improve contacts to flex bonding or to the measurement probes, the electrodes were further metallized by first etching the openings to source/drain electrode pads using a 1:6 buffered oxide etch solution for 2 min. Ti/Au electrodes were deposited by sputtering on Discovery Denton 18 tool for 1.5 and 2.5 min, respectively, with a power of 200 W and Ar flow of 35 sccm, chamber pressure at 2.4 mT.

First, ITO thin film was sputtered onto glass substrates and the source/drain electrodes were defined by photolithography and wet etched in hydrochloric acid. Next, the ZnO thin film was deposited by sputtering by initially growing a thin ≈6 nm layer of ZnO at room temperature as a seed layer, and then growing the remainder at 200 °C up to 60 nm thickness. After sputter deposition, the devices were coated with Al_2O_3 film of 10 nm thickness for passivation using ALD. The same Al_2O_3 film was used as a mask to etch the ZnO channels. First, the Al_2O_3 was etched with a RIE process, followed by a wet etch of ZnO using a dilute hydrochloric acid solution. Next, the Al_2O_3 gate dielectric was grown using ALD to the thickness of 100 nm. Finally, the gate electrode was created by first depositing a thin film of ITO, and later etching the ITO with an HCl solution. The contacts may also be improved for measurement by defining Ti/Au pads on top of the ITO lines. This step was not shown here for simplicity.

PFM Measurements: A Bruker Dimension Icon AFM was used to perform the PFM experiments with conductive cobalt–chromium AFM tips (Bruker MESP). The background signal was removed from the measurement by using vector subtraction in reference to amplitude and phase measurements on a bare glass substrate. This was obtained by applying an AC voltage across the sample and measuring the time dependent deflection of the AFM tip. Here, the phase refers to whether

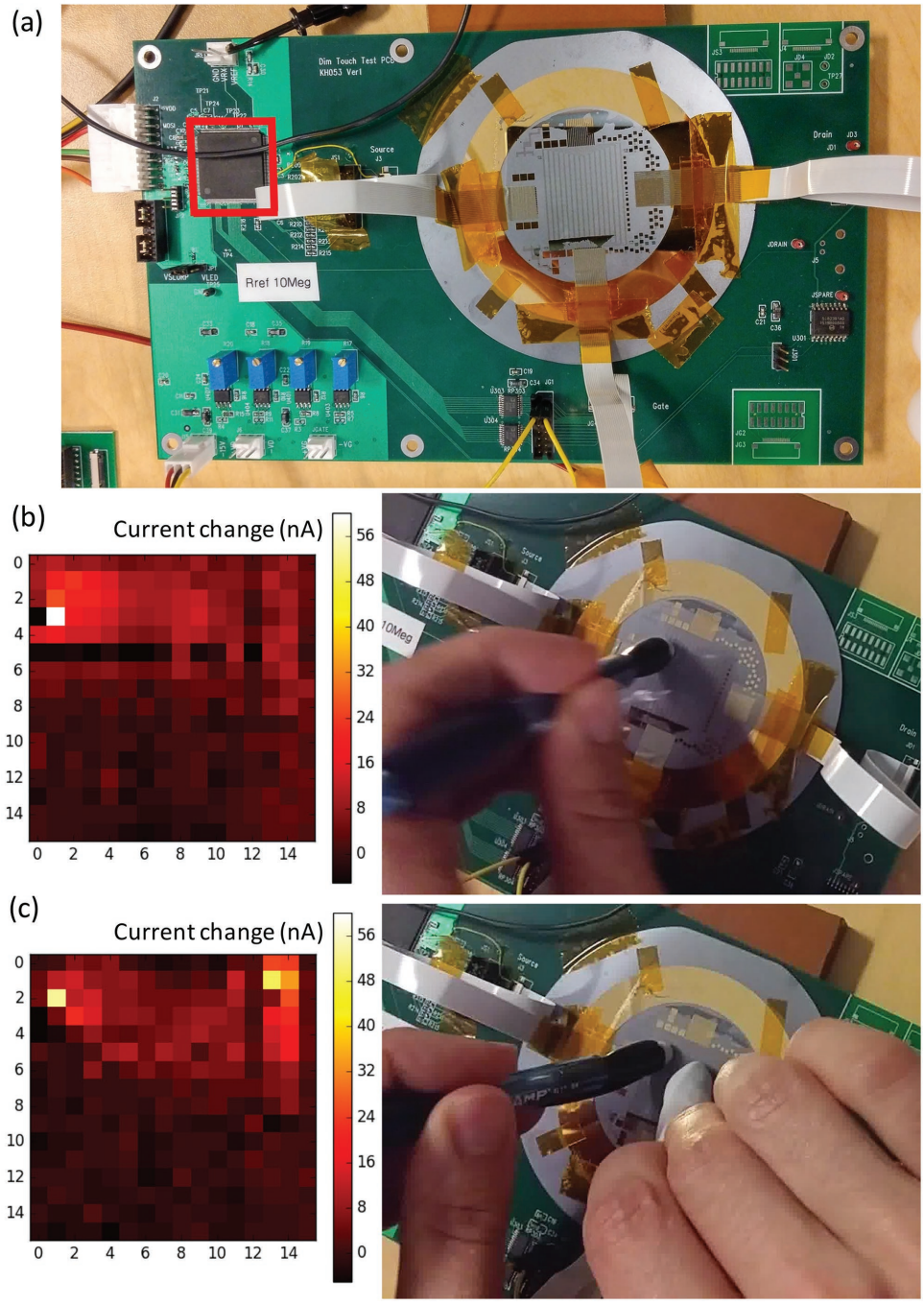

Figure 7. Reading out 16 × 16 pressure sensor array using a commercial touch driver IC. a) Custom designed PCB for interfacing a commercial chip to 16 × 16 sensor array. The actual chip is positioned on top left of the PCB, highlighted by a red box. b) A single object pressing on the array, and the corresponding 2D heat map of the drain current change. c) Two objects pressing on the array simultaneously and the corresponding heat map.

the sample is deflecting in-phase or out-of-phase with the applied voltage as measured by a lock-in amplifier. By creating a vector using the amplitude and phase of the glass signal and the ZnO signal, a vector subtraction was done to remove background signal which is not part of the real piezoresponse.

Electrical Characterization: The electrical measurements were performed using in-house developed tools, which included NI 6030E DAQ system, Keithley 6487 picoammeter/voltage source, Ithaco 1211 current preamplifier, as well as custom-developed breadboard and PCB circuits. The circuits were controlled by Arduino Mega 2560 microcontroller interfaced to a PC using Python.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by an NSF-IIP Award No. 1600329, partial support from the NSF No. ECCS-1351980, the NSF DMR-1311866, and the NSF-DMR-1503595, and by the department of Electrical and Computer Engineering at the UC San Diego. This work was performed in part at the UC San Diego's Nanotechnology Infrastructure, a member of the National Nanotechnology Coordinated Infrastructure, which is supported by the National Science Foundation. Part of this work was performed at the Center for Integrated Nanotechnologies (CINT), a U.S. Department of Energy Office of Basic Energy Sciences user facility at the Los Alamos National Laboratory (Contract DE-AC52-06NA25396) and the Sandia National Laboratories (Contract DE-AC04-94AL85000) through a CINT user proposal.

Conflict of Interest

The authors declare no conflict of interest.

Keywords

arrays, pressure sensors, thin film transistors (TFTs), touchscreens, ZnO

Received: October 6, 2017
Published online:

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