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# Crystalline SrZrO<sub>3</sub> deposition on Ge (001) by atomic layer deposition for high-*k* dielectric applications

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Heteroepitaxial growth of crystalline SrZrO<sub>3</sub> (SZO) on Ge (001) by atomic layer deposition is reported. Ge (001) surfaces are pretreated with 0.5-monolayers (ML) of Ba and an amorphous ~3-nm SZO layer is grown from strontium bis(triisopropylcyclopentadienyl), tetrakis (dimethylamido) zirconium, and water at 225 °C. This ~3-nm layer crystallizes at 590 °C and subsequent SZO growth at 225 °C leads to crystalline films that do not require further annealing. The film properties are investigated using X-ray photoelectron spectroscopy, x-ray diffraction, aberration-corrected electron microscopy, and capacitance-voltage measurements of metal-oxide semiconductor capacitor structures. Capacitance-voltage measurements of the SrZrO<sub>3</sub>/Ge heterojunctions reveal a dielectric constant of 30 for SrZrO<sub>3</sub> and a leakage current density of  $2.1 \times 10^{-8}$  A/cm<sup>2</sup> at 1 MV/cm with an equivalent oxide thickness of 0.8 nm. Oxygen plasma pretreatment of Ge (001), Zintl layer formation with 0.5 ML Ba, and atomic deuterium post-growth treatment were explored to lower interface trap density ( $D_{it}$ ) and achieved a  $D_{it}$  of  $8.56 \times 10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup>. Published by AIP Publishing.

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## I. INTRODUCTION

Crystalline perovskites have received increased attention due to the possibility of realizing a wide array of material functionalities including high-*k* dielectric, piezoelectricity, ferroelectricity, ferromagnetism, etc.<sup>1,2</sup> McKee first reported epitaxial growth of SrTiO<sub>3</sub> (STO) on silicon in 1998.<sup>3</sup> The study of crystalline perovskites on semiconductors has been widely expanded subsequently for device applications,<sup>4-13</sup> including the use of crystalline perovskites as a high-*k* gate oxide for field-effect transistor device applications.<sup>14</sup>

In the past several decades, the goals of faster computing speed and lower power consumption have led to ever-smaller transistor feature sizes and ever-thinner gate oxide. Unacceptable leakage current for SiO<sub>2</sub> on silicon<sup>15</sup> led to a search for alternative gate oxide materials. For high dielectric constant materials, the *k* value should be more than 12, preferably 25 to 35.<sup>16</sup> Previous work studied the deposition of crystalline SrHfO<sub>3</sub> (SHO), STO, and SrHf<sub>x</sub>Ti<sub>1-x</sub>O<sub>3</sub> (SHTO) on Ge (001) by atomic layer deposition (ALD).<sup>9,10,17</sup> The titanium-based perovskites display a large leakage current because of the negligible conduction band offset (CBO) between the Ti 3*d* states and Si or Ge.<sup>18-20</sup> While the STO/Ge heterojunction achieved *k* ~ 90 and an equivalent oxide thickness (EOT) of 0.7 nm, the leakage current density was around 10 A/cm<sup>2</sup> at 0.7 MV/cm.<sup>17</sup> Substituting Hf onto the Ti sites led to a lower dielectric constant, larger EOT, and lower

leakage current density, with values of *k* ~ 30, an EOT of 1.8 nm, and a leakage current density of 0.1 A/cm<sup>2</sup> at 1 MV/cm for SrHf<sub>0.55</sub>Ti<sub>0.45</sub>O<sub>3</sub>.<sup>9</sup> SHO displayed *k* ~ 17, an EOT of 1.0 nm, and a leakage current density of ~6.3 × 10<sup>-6</sup> A/cm<sup>2</sup> at 1.0 MV/cm.<sup>10</sup> While the leakage current density and EOT for SHO/Ge were comparable to those state-of-the-art Ge-based metal oxide semiconductor field effect transistors (MOSFETs), the interface trap density ( $D_{it}$ ) of ~4 × 10<sup>13</sup> cm<sup>-2</sup> eV<sup>-1</sup> of crystalline SrHfO<sub>3</sub> on Ge without a capping layer or treatment was too high.<sup>21</sup> Annealing temperatures above 650 °C were required to realize crystalline SHO films and this led to an amorphous interfacial layer of several Angstroms that may have contributed to the high  $D_{it}$  values. Zirconium, with an atomic mass half that of Hf, is expected to reduce the crystallization temperature of thin SrZrO<sub>3</sub> (SZO) when compared to SHO.<sup>9</sup>

Strontium zirconate has a conduction band offset (CBO) with Ge comparable to that of SHO, with values of 1.41–1.77 eV and 2.17 eV for SZO/Ge and SHO/Ge, respectively. SZO also has a large band gap of 5.7 eV and a dielectric constant *k* around 30.<sup>10,13,22,23</sup> Several groups have studied growth of crystalline SZO by molecular beam epitaxy (MBE) or pulsed laser deposition (PLD).<sup>13,22,24</sup> Herein, we report ALD growth of crystalline SZO and approaches to reduce the  $D_{it}$  through steps taken prior to ALD and by annealing SZO/Ge in a flux of atomic deuterium. Comparison of various Group 4 B-site cations in ALD-grown crystalline ABO<sub>3</sub> perovskites shows Zr to perform the best among Ti, Zr, and Hf in terms of leakage current density and  $D_{it}$ .

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The channel material plays a significant role in MOSFET performance. Silicon is the most common substrate and further transistor scaling requires that the channel material has higher mobility, which can lead to higher drive current.<sup>25–27</sup> Compared to Si, the electron mobility and hole mobility for Ge are 3900 vs 1400 cm<sup>2</sup>/V s and 1900 vs 500 cm<sup>2</sup>/V s, respectively, which makes Ge viable as a next generation channel material.<sup>27,28</sup> In addition, Ge has a more unstable oxide than Si, making it easier to remove the native oxide to achieve a clean surface.<sup>29–31</sup>

A high  $D_{it}$  can affect the channel mobility and negate the inherent mobility advantages of Ge.<sup>27</sup> Current state-of-the-art Ge-based MOSFETs have  $D_{it}$  less than  $1 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>.<sup>32–36</sup> Defects at the interface of Ge-based heterojunctions are mainly formed by dangling bonds.<sup>27,37</sup> Ge substrate roughness also increases  $D_{it}$ .<sup>9,38</sup> Several groups have employed different methods to lower the interface trap density,<sup>21,32–36,39–41</sup> one method uses GeO<sub>x</sub> as a passivation layer to yield  $D_{it}$  values in the low  $10^{11}$  cm<sup>-2</sup> eV<sup>-1</sup> range.<sup>32,34–36,42,43</sup> However, the presence of the passivation layer increases the EOT. The smoothness of a Ge surface can be improved with oxygen plasma treatment.<sup>30</sup> Zhang *et al.* used post-deposition annealing to treat Al<sub>2</sub>O<sub>3</sub>/GeO<sub>x</sub>/n-Ge in ambient atmosphere of N<sub>2</sub>, forming gas, H<sub>2</sub>, D<sub>2</sub>, atomic H, and atomic D to heal dangling bonds; the atomic D treatment led to the best effective electron mobility.<sup>44</sup> D desorption yields are 50 times lower than the H yields on Si,<sup>45</sup> and a lower yield should also be expected for D on Ge. Atomic D treatment is reported herein for crystalline SZO/Ge interfaces that do not feature an interfacial oxide.

## II. EXPERIMENT

### A. Ge substrate preparation

The growth facility has been previously described.<sup>46</sup> It includes an ALD chamber, a surface analysis chamber, a molecular beam epitaxy chamber, and a deuterium dosing chamber (described below) all connected to a common ultra-high vacuum transfer line, maintained at a base pressure  $<10^{-9}$  Torr, so the samples remain *in situ* between treatment, growth, and analysis. The 4-in. Ge wafers (n-type, Sb-doped, 0.1–0.5  $\Omega$  cm resistivity) were purchased from MTI Corp. and diced into  $18 \times 20$  mm<sup>2</sup> pieces. The Ge (100) wafers are  $(100) \pm 0.21^\circ$ – $0.25^\circ$  and with a polished roughness of  $<0.5$  nm. After degreasing the Ge substrate with acetone, isopropyl alcohol, and deionized water in an ultrasonic bath, two preparation methods were used to remove the residual carbon contamination and produce the  $2 \times 1$ -reconstructed Ge (001) surface that is the necessary template for perovskite growth by ALD.<sup>17</sup> Method A is the same procedure as previous work, in which a 30-min UV/ozone exposure was followed by 1 h thermal annealing at 700 °C in vacuum ( $<2 \times 10^{-9}$  Torr) to remove any native oxide. Method B used an oxygen plasma to remove the residual carbon contamination instead of UV/ozone exposure and to lower the surface roughness. In Method B, the sample was loaded into the vacuum system after degreasing and was transferred to the MBE chamber. An oxygen plasma with  $1.2 \times 10^{-5}$  Torr background

oxygen pressure and 300 W forward power is estimated to produce an atomic oxygen flux of  $\sim 5 \times 10^{13}$  cm<sup>-2</sup> s<sup>-1</sup>.<sup>30</sup> During the 30-min oxygen plasma exposure, the substrate temperature was 100 °C. Following plasma treatment, 1 h thermal annealing at 700 °C was applied to remove GeO<sub>2</sub>.

*In situ* reflection high-energy electron diffraction (RHEED) (Staib Instruments operating at 21 keV) was used to verify the reconstructed surface structure for Methods A and B. The clean Ge (001) sample was transferred *in situ* to the surface analysis chamber with an X-ray photoelectron spectrometer to verify the Ge surface composition. Following the thermal deoxidization process at 700 °C, some samples were heated to 600 °C for Zintl template preparation.<sup>47</sup> The Zintl template consisting of 0.5-monolayer (ML) of Ba was prepared by depositing atomic Ba in the MBE chamber on the deoxidized Ge (001) surface using a Ba flux rate that was calibrated to be 1 ML/min by a quartz crystal monitor in the MBE chamber.<sup>47</sup> *In situ* RHEED confirmed the  $2 \times 1$ -reconstructed surface structure for the Zintl template.

### B. Film growth

The bare Ge and Zintl-templated Ge substrate were transferred *in situ* to the ALD chamber for SZO seed layer growth at 225 °C. Argon carrier gas was at 1 Torr. Strontium bis(triisopropylcyclopentadienyl) from Air Liquide and tetrakis(dimethylamido) zirconium (IV) from Sigma-Aldrich were used as the Sr and Zr precursor and were heated to 130 and 60 °C, respectively. H<sub>2</sub>O, maintained at room temperature, was used as the oxygen source. Each unit cycle includes 2-s precursor dosing, 1-s H<sub>2</sub>O dosing, and 20-s Ar purging following each reactant exposure. When growing the slightly Sr-rich film, the cycle ratio was Sr:Zr = 3:2 on bare Ge (001). On Zintl-templated Ge (001), a cycle ratio of Sr:Zr = 2:1 was found to work best.

The first seed layer (20 ALD cycles and 2–3 nm thick) always grew as an amorphous film, so post-deposition annealing was required to obtain the single crystalline film. The sample was transferred back to the MBE chamber in vacuum and heated to the crystallization temperature with a  $10^\circ\text{C min}^{-1}$  heating rate. The onset of crystallization has been defined as the initial appearance of a diffraction spot in RHEED as described in previous work.<sup>9</sup> The sample temperature was then ramped up another 30 °C and maintained for 5 min to achieve better crystallinity. The temperature was established using a pyrometer. During the annealing process, RHEED was used to observe the transformation from an amorphous to crystalline film in real time. Obtaining single crystalline SZO films above 3-nm thickness required a two-step growth process. After annealing the 3-nm amorphous SZO film to achieve single crystalline SZO, the sample was transferred back to the ALD chamber for continuous film growth with a Sr:Zr = 3:2 cycle ratio. The second SZO layer was crystalline as deposited and the crystallinity was improved with post-deposition annealing to around 550 °C without pausing.

### C. Atomic deuterium treatment

Atomic D treatment was performed in a custom-built deuterium source chamber to explore the effect of deuterium



exposure on SZO/Ge heterojunctions, which previous studies have suggested can improve the trap density.<sup>44</sup> Atomic D was generated by a 400-W Osram Xenophot bulb, which had part of the glass enclosure removed to expose the tungsten filament. A current of 5.2 A was supplied by a DC power supply (KEPCO, MSK10-10M) to the tungsten filament and the filament temperature was  $\sim 1800$  K, as measured by a pyrometer. At this temperature, the tungsten filament can crack molecular deuterium to generate atomic deuterium.<sup>48</sup> The deuterium gas (99.999%; Matheson) pressure was controlled by a leak valve and maintained at  $5.0 \times 10^{-6}$  Torr in the chamber. The flux of atomic D was estimated around  $2 \times 10^{13}$  D/cm<sup>2</sup>·s based on previous work.<sup>49</sup> The sample was positioned approximately 4 cm above and faced toward the tungsten filament. A pyrolytic boron nitride heater from Momentive was 2 cm above the sample and maintained the sample temperature at 350 °C during treatment. The treatment time ranging from 1 to 3 h was adjusted for different SZO layer thicknesses.

### D. Characterization

In addition to RHEED that was used to monitor the Ge surface reconstruction and the film surface order that is used to track the crystallization process, *in situ* X-ray photoelectron spectroscopy (XPS) was performed to confirm the Ge surface composition and SZO film stoichiometry. The X-ray photoelectron spectrometer was equipped with a monochromatic Al K $\alpha$  source at 1486.6 eV and a VG Scienta R3000 electron energy analyzer, which is calibrated by a clean Ag foil. To obtain the spectra for the Sr 3d, Zr 3d, Ge 3d, and C 1s core levels, the basic settings were 100 eV pass energy with a 0.4 mm analyzer slit width and 50 meV steps with 157 ms/step dwell time. At this condition, the spectrometer yielded around 350 meV effective resolution. CasaXPS (Version 2.3.16 PR 1.6) was used to analyze the results. The atomic sensitivity factors for Sr 3d and Zr 3d were set as 1.843 and 2.576, respectively.<sup>50</sup>

For *ex situ* characterization, the film thickness was measured by X-ray reflectivity (XRR) and crystallinity was analyzed by X-ray diffraction (XRD) on a Rigaku Ultima IV system with a Cu K $\alpha$  source. High-angle annular-dark-field scanning transmission electron microscopy (HAADF-STEM) was employed here to investigate the grown film and interface. The samples were prepared via the standard cross-section method with Ar ion milling, and STEM images were taken with a probe-corrected JEOL ARM 200F operated at 200 kV.

Metal oxide semiconductor (MOS) capacitor structures were used to study the electrical properties, which include dielectric constant  $k$ , leakage current density  $J$ , and interface trap density  $D_{it}$ .<sup>25,27</sup> After patterning by optical lithography, 100  $\mu\text{m} \times 100 \mu\text{m}$  square top electrode contacts of Pt were fabricated by electron beam evaporation followed by lift-off. The backside of the substrate was scratched and silver paste was applied to form the bottom electrode. The capacitance-voltage (C-V) and current-voltage (I-V) measurements were performed on an Agilent B1500A semiconductor device parameter analyzer with a Cascade Microtech probe station.

A cryogenic probe station from Lakeshore Cryotronics was used for low temperature  $D_{it}$  measurement at 250 K.

## III. RESULTS AND DISCUSSION

### A. Ge substrate pretreatment

Figure 1 shows RHEED images indicating surface structure changes during the Ge substrate pretreatment process. The Ge surface is transformed from a  $1 \times 1$ - to a  $2 \times 1$ -reconstructed structure after thermal annealing to remove oxygen, which demonstrates Ge surface dimer formation. The  $2 \times 1$ -reconstructed Ge substrate was found to be necessary for ALD and MBE growth of crystalline perovskites.<sup>17,51</sup> The samples treated by UV/ozone and by the oxygen plasma show the same RHEED pattern after oxygen treatment [Fig. 1(b)] and after thermal annealing to remove oxygen [Fig. 1(c)] as illustrated for an oxygen plasma-treated sample in Fig. 1. The weaker  $1 \times 1$  pattern in Fig. 1(b) compared with Fig. 1(a) is a consequence of the thicker oxide layer that forms during oxygen plasma treatment. Any native carbon contamination of Ge (001) is removed by either the UV/ozone or oxygen plasma process<sup>17,30</sup> and the native oxide is removed after thermal annealing.<sup>9,17</sup> Oxygen plasma treatment was used to achieve a flatter reconstructed Ge (001) surface with fewer steps than are found using a UV/ozone treatment.<sup>30</sup> Fewer surface steps can help to reduce the number of defects at the interface and lower anti-phase boundary (APB) formation in films.<sup>9,52</sup> More details about the various methods of Ge surface cleaning are reviewed in the literature.<sup>53</sup>

Over time, the ALD chamber accumulates  $i\text{Pr}_3\text{Cp}$  ligands or  $i\text{Pr}_3\text{Cp}$ -derived molecules on the chamber surfaces that likely adsorb on bare Ge (001) and produce about 1 ML-equivalent of carbon contamination on the Ge (001) surface.<sup>47</sup> A recent study found that a Zintl template formed by adsorbing 0.5-ML Ba on Ge (001) by MBE could prevent the carbon adsorption in the ALD chamber.<sup>54</sup> The Zintl-templated surface formed with Ba retains the reconstructed

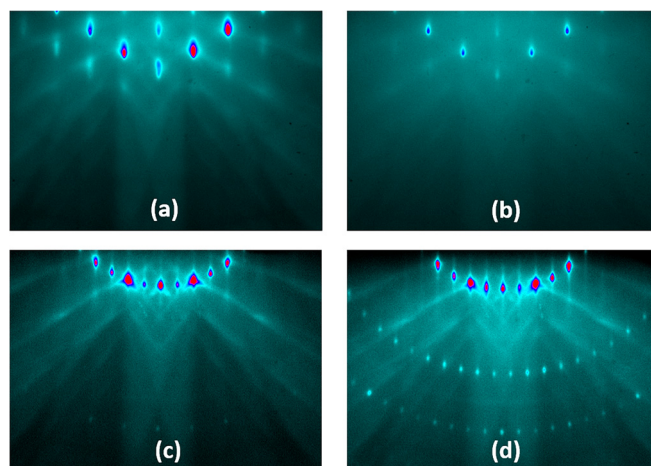


FIG. 1. Ge (001) surface observation by RHEED along the [110] zone axis (a) prior to oxygen plasma treatment; (b) after oxygen plasma treatment for 30 min; (c) after 1 h vacuum annealing at 700 °C. (d) Zintl template formation by 0.5-ML Ba deposition on Ge. All images taken at 200 °C substrate temperature with the same emission current.

surface structure as shown in Fig. 1(d). The sharper  $2 \times 1$  pattern following Zintl layer formation indicates the long-range order and cleanliness of the Ge surface. *In situ* XPS was used to check the surface composition for both Zintl-templated and clean bare Ge. XPS results also verify that the Zintl template is free of carbon and oxygen.<sup>47</sup>

## B. Deposition and crystallization of $\text{SrZrO}_3$

The SZO films above 3-nm thickness require a two-step growth procedure in which thicker films are deposited on a crystallized layer of SZO. As shown in Fig. 2(a), the first seed layer grows as an amorphous film on the Zintl template. With vacuum annealing at  $630^\circ\text{C}$  for 5 min, the first layer of SZO transforms from amorphous to crystalline. The second layer grows as a crystalline layer at  $225^\circ\text{C}$ . Sharper RHEED patterns can be realized by further annealing the second layer at  $550^\circ\text{C}$  [Fig. 2(b)]. Similar results were found with STO where a crystalline seed layer enabled subsequent STO growth as a crystalline film.<sup>55</sup> The SZO films grown on bare Ge (001) required the same two-step procedure in which the 2–3 nm amorphous films were annealed to crystallize the film (RHEED images not shown). The crystallization temperature for the seed layer on bare Ge is around  $590^\circ\text{C}$ , which is lower than that of  $\text{SrHfO}_3$  ( $\sim 650^\circ\text{C}$ ) but higher than that of  $\text{SrTiO}_3$  ( $\sim 510^\circ\text{C}$ ) on bare Ge (001).<sup>9</sup> This is consistent with the observation that the crystallization temperature in  $\text{SrBO}_3$  (B represents the column 4 elements, Ti, Zr, or Hf) amorphous thin films correlates with the atomic weight of the B-site atom.<sup>9</sup>

On bare Ge (001), the SZO seed layer is grown with a cycle ratio of  $\text{Sr}:\text{Zr} = 3:2$  and 20 unit cycles in total ( $\sim 3$  nm), which results in 49% Sr and 51% Zr (metals basis) by XPS. On Zintl-templated Ge, the same cycle ratio of  $\text{Sr}:\text{Zr} = 3:2$  will lead to SZO stoichiometry of 46% of Sr and 54% Zr. Films with this stoichiometry crystallize at  $640^\circ\text{C}$ . A higher Sr cycle is needed for Zintl-templated Ge. With a  $\text{Sr}:\text{Zr} = 2:1$  cycle ratio and a total of 20 unit cycles, the stoichiometry is 50% Sr and 50% Zr and the crystallization temperature is around  $600^\circ\text{C}$ .

The previous study showed that the bare  $2 \times 1$  Ge (001) surface could decompose the Sr precursor to form adsorbed Sr atoms that feature many of the same binding energy shifts as MBE-deposited Sr or Ba atoms.<sup>47</sup> However, higher-order reconstructions of Ge (001) were found with Sr compared to the  $2 \times 1$  reconstruction with 0.5-ML Ba that creates the

Zintl template. This Ba-based Zintl template protects the Ge (001) surface from C incorporation from the precursor ligands.<sup>54</sup> For reasons beyond the scope of this study, strontium bis(triisopropylcyclopentadienyl) appears less reactive on a Zintl-templated surface than on a bare Ge (001) surface necessitating the higher Sr cycle of  $\text{Sr}:\text{Zr} = 2:1$  to obtain stoichiometric films. The amorphous SZO on the Zintl-templated surface starts to crystallize at  $640^\circ\text{C}$ , while the amorphous SZO on the bare surface starts to crystallize at  $590^\circ\text{C}$ . The annealing temperature, which we adopt as  $30^\circ\text{C}$  higher than the crystallization temperature, is a significant factor in determining the interface quality. Higher annealing temperature will increase the possibility to form a non-abrupt interface.<sup>9,10</sup> As shown in Fig. 3(a), the SZO seed layer annealed at  $620^\circ\text{C}$  features a structurally abrupt interface in HAADF-STEM images with Sr atoms located between the dimer rows as expected of a Zintl layer.<sup>47,56</sup> In contrast, the SZO seed layer annealed at  $670^\circ\text{C}$  showed a thin layer ( $\sim 0.5$ – $1$  nm) of reduced intensity [Fig. 3(b)]. Moreover, the presence of some amorphous regions along the interface could indicate that the surface of the Ge film may have been partially oxidized at the higher annealing temperature. Since an interfacial reaction might lead to higher interface trap density, the annealing temperature is restricted to below  $640^\circ\text{C}$  in this work by using a 2:1  $\text{Sr}:\text{Zr}$  ALD cycle ratio on a Zintl template and a 3:2 ratio on bare Ge (001).

Regardless of bare Ge or a Ba-Zintl template, the second layer of SZO has the same growth cycle ratio of  $\text{Sr}:\text{Zr} = 3:2$  and crystallizes as it grows. Post-deposition annealing at  $550^\circ\text{C}$  is applied for all second-layer SZO films to improve the crystal quality. Based on XPS, the composition for the SZO films is 53% Sr and 47% Zr. This result is consistent

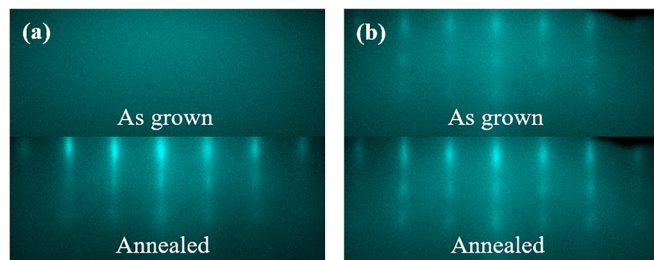


FIG. 2. RHEED images of two step growth for 6.2-nm  $\text{SrZrO}_3$  film on Zintl template Ge before and after annealing, (a) the first layer is around 2 nm; (b) the second layer is 4.2 nm. All images were taken with beam aligned along  $\langle 110 \rangle$  direction.

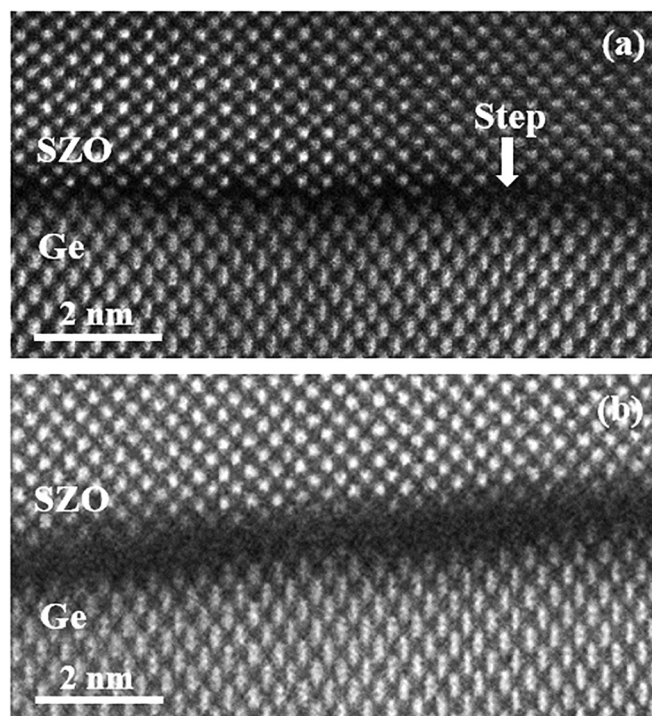


FIG. 3. Aberration-corrected HAADF-STEM images of: (a)  $\text{SrZrO}_3$  on bare Ge (001) annealed at  $620^\circ\text{C}$ ; (b)  $\text{SrZrO}_3$  on Zintl-templated Ge (001) annealed at  $670^\circ\text{C}$ .



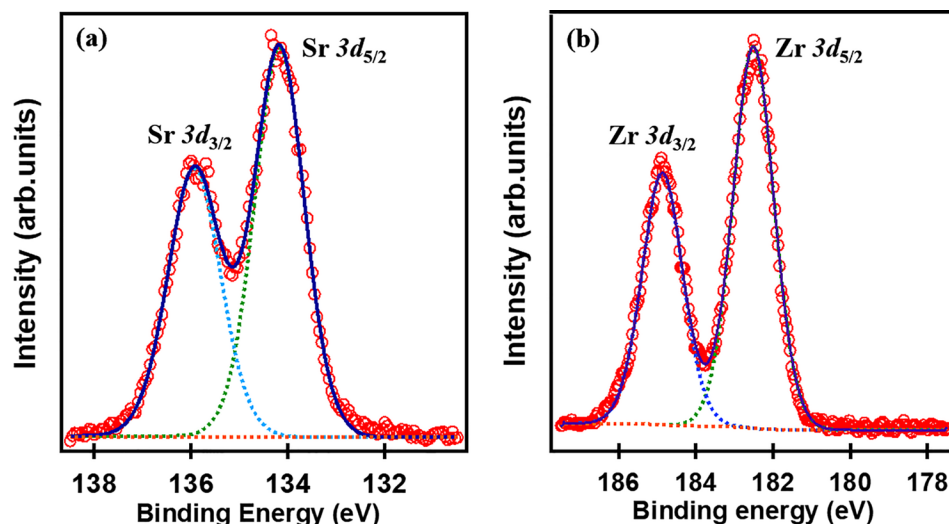


FIG. 4. X-ray photoelectron spectra for Sr 3d (a) and Zr 3d (b) in the 11.5-nm SrZrO<sub>3</sub> film after post-deposition annealing at 550 °C.

with previous work that showed Sr-rich composition helped the crystallization process.<sup>10,17</sup> Figure 4 presents the Sr 3d and Zr 3d X-ray photoelectron spectra. There are no obvious chemical shifts or low oxidation states for Sr<sup>2+</sup> and Zr<sup>4+</sup>, which indicates that the vacuum annealing does not lead to detectable oxygen vacancies in the SZO films.

The film thickness was confirmed by XRR and calculated by Bragg's law. The sample for X-ray measurement was grown with 80 total unit cycles on bare Ge and reached a thickness of 11.5 nm. The growth rate for SZO on Ge was around 1.4 Å per cycle. The out-of-plane scan XRD results in Fig. 5(a) reveal that the (002) peak is located at a  $2\theta$  value of  $43.83^\circ$ , which corresponds to an out-of-plane lattice constant for SZO of 4.13 Å. The in-plane scan of this film (supplementary material, Fig. S1) has a SZO (200) peak at  $2\theta$  of  $44.1^\circ$  corresponding to an in-plane lattice constant of 4.10 Å. The lattice constant for cubic SZO is 4.10 Å at room temperature.<sup>57</sup> The Ge-Ge distance in the [110] direction is 3.992 Å at the Ge (001) surface,<sup>58–60</sup> and a fully strained heteroepitaxial SZO film on Ge would lead to an in-plane compressive strain of  $-2.6\%$ . Relaxation from a strained to the bulk structure with the film thickness has been found in other perovskite systems.<sup>55,57,61–63</sup> Figure 5(b) shows the rocking curve for the (002) reflection of the 11.5-nm sample. The

full-width at half-maximum (FWHM) is  $1.4^\circ$  is somewhat high for such a thin film and, when combined with the in-plane and out-of-plane lattice constants, suggests that the film has mixed strain.<sup>63</sup>

**Supplementary material** Fig. S2(a) presents out-of-plane diffraction peaks for a 26.7-nm SrZrO<sub>3</sub> film grown on bare Ge by ALD; the SZO (002) reflection is at  $2\theta = 44.19 \pm 0.5^\circ$  corresponding to an out-of-plane lattice constant of 4.10 Å. The rocking curve of the (002) reflection associated with the 26.7-nm film [supplementary material Fig. S2(b)] has a full width at half maximum of  $0.9^\circ$ . The thicker film (Fig. S2, supplementary material) is likely relaxed to the bulk cubic structure.

One indication of surface quality can be found in the XRR scan of the 26.7-nm film [supplementary material Fig. S2(c)]. Atomic force microscopy (not shown) was also used to probe surface quality. The 11.5-nm film (used in Fig. 5) had a  $R_q$  roughness of 1.144 nm when measured over  $10 \mu\text{m} \times 10 \mu\text{m}$  areas and an  $R_q$  of 1.048 nm when measured over  $5 \mu\text{m} \times 5 \mu\text{m}$  areas.

### C. Electrical properties

Experiments were conducted to compare the effects of different starting surfaces and post-deposition exposure to

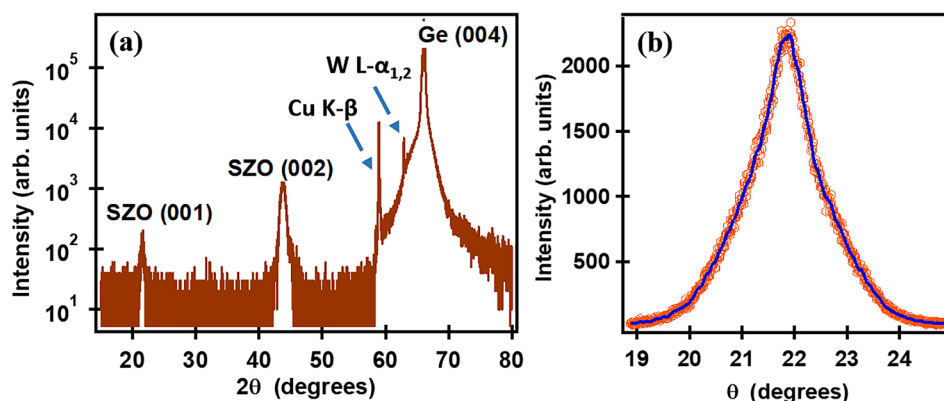


FIG. 5. X-ray diffraction pattern (a), and rocking curve (b), for the 11.5-nm SrZrO<sub>3</sub> film grown on bare Ge by ALD that was used to fabricate Device A. The 2-nm thick seed layer was post-deposition annealed at 620 °C in vacuum and the final film was annealed at 550 °C. The SZO (002) reflection peak is at  $2\theta = 43.83 \pm 0.5^\circ$  and the rocking curve for the (002) reflection has a full width at half maximum (FWHM) of  $1.4^\circ$ . The diffraction features labeled Cu K- $\beta$  and W L- $\alpha_{1,2}$  are associated with the Ge (004) reflections caused by X-ray source emissions for Cu K- $\beta$  and W L- $\alpha_{1,2}$ .

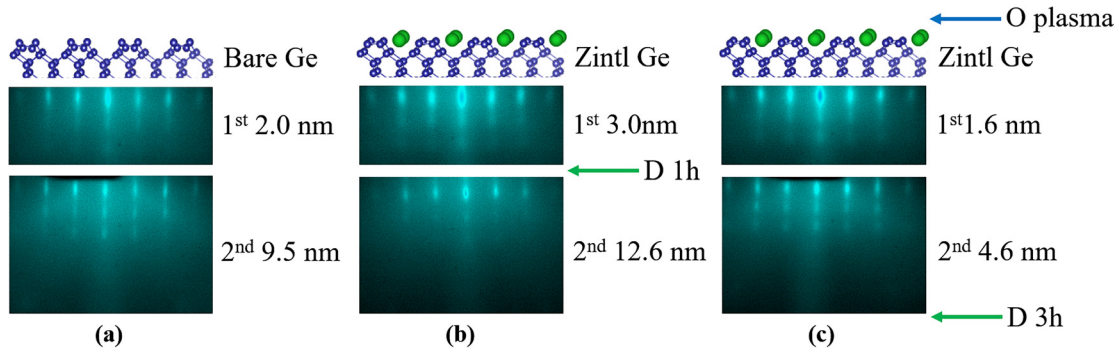


FIG. 6. Schematic of treatment procedures for Samples A, B, and C. (a) Sample A, two-step SZO deposition on bare Ge, (b) Sample B, two-step SZO deposition on Zintl-templated Ge with 1 h atomic D post treatment, and (c) Sample C, two-step SZO growth on Zintl-templated Ge with an oxygen plasma pretreatment and 3 h atomic D post treatment.

atomic D on  $D_{it}$ . Figure 6 presents a schematic and RHEED images from different treatment protocols discussed herein. Sample C used the thinnest first SZO layer to minimize the SZO film through which atomic D would need to diffuse to heal dangling bonds at the Ge-SZO interface. The comparison of a Zintl template with bare Ge is not shown here. Consistently more functional and stable devices are detected on the Zintl-templated samples than bare Ge samples, which indicates that the non-uniform carbon contamination at the interface might cause some device failure on bare Ge samples. Since the thicker SZO film would require longer gas diffusion time to reach the interface, the atomic D treatment was applied after obtaining the first crystalline 3-nm SZO layer instead of treating the 15-nm SZO film on Sample B. Sample A corresponds to an 11.5-nm film grown directly on bare Ge (001) that was treated with UV/ozone. Only Sample C was subjected to the oxygen plasma pretreatment protocol. Table I summarizes the sample preparation steps.

For Devices A, B, and C made from Samples A, B and C, respectively, C-V and I-V measurements were performed at room temperature, and  $D_{it}$  was measured at 250 K.<sup>64</sup> Figure 7 shows the C-V characteristics for Device C at frequencies from 1 kHz to 1000 kHz. The capacitance is normalized by the area of the top  $100\ \mu\text{m} \times 100\ \mu\text{m}$  square Pt electrode. The saturated  $C_{ox}$  at accumulation was  $3.92\ \mu\text{F}/\text{cm}^2$  with the 1 kHz C-V scan, which yields a dielectric constant of 27.6. A more accurate  $C_{ox}$  should be determined by C-V scans at a low frequency around 20 Hz but noisy signals were obtained. The flat band shift dispersion in Fig. 7 is likely related to the border traps, as studied by previous work.<sup>65</sup> A quasi-static method<sup>66</sup> was applied to correct the  $C_{ox}$  to estimate the dielectric constant. The final estimate for this device is around 30, which is consistent with reports in

the literature.<sup>24</sup> The same measurement and correction method were applied to Devices A and B. Both devices yield  $k$  of 30. Representative C-V scans are shown in the [supplementary material](#) for Devices A and B in Figs. S3 and S4, respectively.

As shown in Fig. 8, all devices are very insulating. The leakage current is normalized by the area of the top electrode to obtain the leakage current density. Nine, seven, and ten junctions were randomly tested across the whole wafer for Devices A, B, and C, respectively. The dielectric constant  $k$  for all three devices is nearly identical, with average  $k$  of 30 and standard deviation of 0.92. The apparent voltage shifts in the current-voltage characteristics arise due to small changes in parasitic current, at the level of  $\sim 10\ \text{fA}$ , from device to device. The asymmetry between positive and negative voltages is a consequence of the asymmetric structure of the junction and of carrier transport across the oxide between the metal and an inversion layer (for negative bias), and across the oxide plus a semiconductor depletion layer (for positive bias).

Table II lists the leakage current density ( $J$ ) at an applied electric field ( $E$ ) of 1 MV/cm along with the corresponding equivalent oxide thickness for the devices. Based on measurements for up to ten randomly tested junctions on each device, the average value of leakage current density is  $2.9 \times 10^{-8}$  with a standard deviation of  $1.6 \times 10^{-8}$  for Device A,  $2.3 \times 10^{-8}$  with a standard deviation of  $1.7 \times 10^{-8}$  for Device B, and  $3.4 \times 10^{-8}$  with a standard deviation of  $2.9 \times 10^{-8}$  for Device C. The electrical properties in previous studies on STO/Ge, SHO/Ge, and SHTO/Ge heterojunctions are also listed for comparison.

The leakage current density of SZO/Ge is about nine orders of magnitude less than that of STO/Ge, which is

TABLE I. Summary of the sample preparation protocol.

Film sample	Pretreatment steps prior to film growth	Sequence of growth and processing steps
A	UV/ozone	2-nm SZO ALD; anneal at 630 °C for 5 min + 9.5-nm SZO ALD; anneal 550 °C for 30 min
B	UV/ozone + 0.5 ML-Ba Zintl layer	3-nm SZO ALD; anneal at 630 °C for 5 min + 1 h exposure to D-atom source at 350 °C + 12.6-nm SZO ALD; anneal at 550 °C for 30 min
C	UV/ozone + oxygen plasma treatment and 700 °C anneal step + 0.5 ML-Ba Zintl layer	1.6-nm SZO ALD; anneal at 630 °C for 5 min + 4.6-nm SZO ALD; anneal at 550 °C for 30 min + 3 h exposure to D-atom source at 350 °C

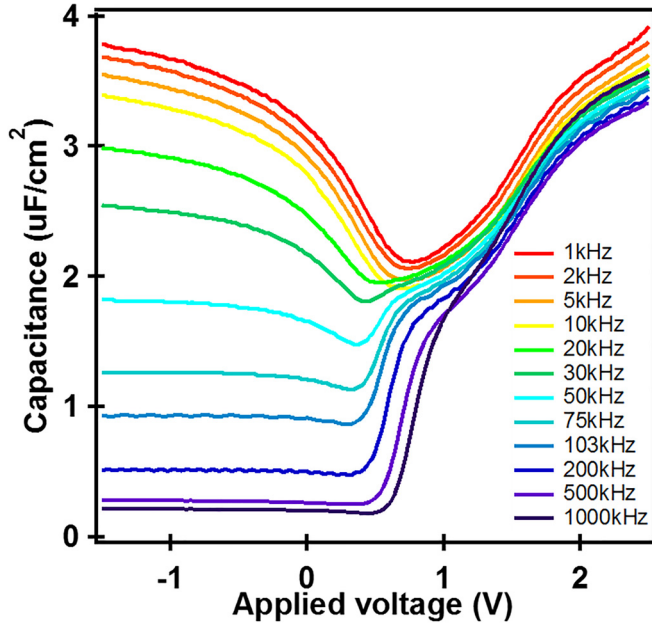


FIG. 7. Capacitance-voltage (C-V) characteristics of 6.2-nm SZO on the Zintl template (Device C) for frequencies from 1 kHz to 1000 kHz. The capacitance is normalized by the area of the top  $100 \mu\text{m} \times 100 \mu\text{m}$  square Pt electrode.

consistent with the CBO for these heterojunctions. The CBOs for STO/Ge, SZO/Ge, and SHO/Ge heterojunctions are 0.12, 1.77, and 2.17 eV, respectively.<sup>10,17,24</sup> The conduction band offset gets larger from Ti to Hf as the energy of the  $d$ -state goes up as  $3d$ ,  $4d$ , and  $5d$ , and these states control the conduction band of the  $\text{SrBO}_3$  oxide. Even though SHO/Ge has a higher CBO than SZO/Ge, the leakage current density for SZO/Ge is approximately two orders of magnitude less than that of SHO/Ge. The main reason may be that SZO is

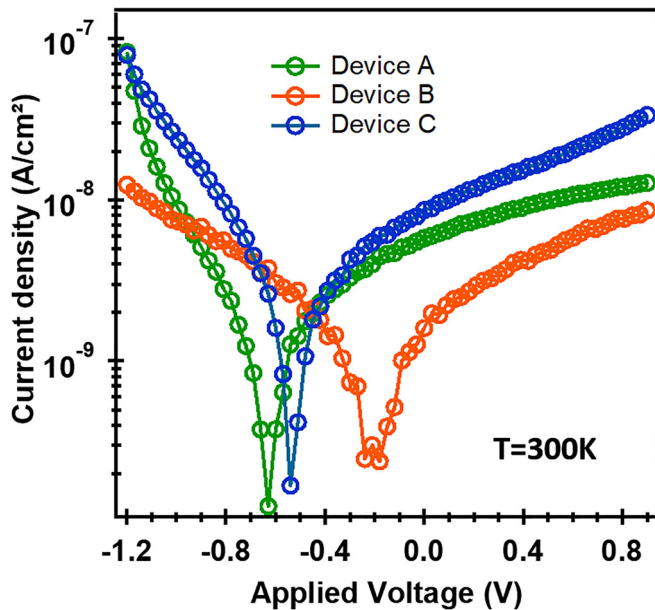


FIG. 8. Leakage current density-voltage (J-V) characteristics of 11.5-nm-SZO on Ge (Device A), 15.6 nm-SZO on the Zintl template (Device B), and 6.2 nm-SZO on the Zintl template (Device C). All devices exhibit low leakage current density. The leakage current density is normalized by the area of the top  $100 \mu\text{m} \times 100 \mu\text{m}$  square Pt electrode.

TABLE II. Electrical properties for  $\text{SrBO}_3/\text{Ge}^a$  heterojunctions.

Material		$J$ ( $\text{A}/\text{cm}^2$ )	EOT (nm)	$k$	E (MV/cm)
$\text{SrZrO}_3$	Device A	$2.9 \pm 1.6 \times 10^{-8}$	1.5	$30 \pm 0.92$	1.0
	Device B	$2.3 \pm 1.7 \times 10^{-8}$	2.0		
	Device C	$3.4 \pm 2.9 \times 10^{-8}$	0.8		
$\text{SrTiO}_3$ <sup>20</sup>		$\sim 10$	0.65	$\sim 90$	0.7
$\text{SrHfO}_3$ <sup>10</sup>		$6.3 \times 10^{-6}$	1.0	17	1.0
$\text{SrHf}_{0.55}\text{Ti}_{0.45}\text{O}_3$ <sup>9</sup>		0.1	1.8	30	1.0

<sup>a</sup>B represents the column 4 elements, Ti, Zr, or Hf.

easier to crystallize than SHO. The annealing temperature for SZO/Ge is about  $50^\circ\text{C}$  less than SHO/Ge. Higher temperature post-deposition annealing could cause more oxygen vacancies in the SHO films. Comparing the leakage current density performance and the EOT with other gate oxides on Ge that are reported in the literature<sup>21</sup> shows that crystalline SZO has a lower leakage current density without sacrificing the EOT. This suggests that crystalline SZO could be a competitive high- $k$  gate oxide material for field-effect transistor device applications.

The interface trap density is also an important consideration for high performance field-effect transistor applications. Our previous study of crystalline SHO on Ge (001) without treatment revealed that  $D_{it}$  was  $4 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ ,<sup>10</sup> generally too high for device applications. In this earlier work,  $D_{it}$  of SHO/Ge was measured at room temperature and estimated by the conductance method,<sup>10,21</sup> which assumes small intrinsic carrier concentration ( $1.45 \times 10^{10} \text{cm}^{-3}$  for Si at room temperature). Ge has a much higher intrinsic carrier concentration of  $2.4 \times 10^{13} \text{cm}^{-3}$  at room temperature, contributing strong conductance loss in weak inversion. In this work, we have therefore performed  $D_{it}$  measurements on oxide/Ge heterojunctions at 250 K.<sup>64,67</sup> In the conductance method for  $D_{it}$  measurement, the conductance  $G_p$  is measured as a function of frequency and plotted as  $G_p/\omega$  versus  $\omega$ . Figure 9 presents results for Devices B and C in the depletion region and the weak inversion region. The plot for Device A is shown in the [supplementary material](#), Fig. S5. Based on the conductance method, in the depletion and weak inversion regions, one takes the maximum peak value among the  $G_p/\omega$  versus  $\omega$  curves and substitutes it into the following equation to estimate the  $D_{it}$  value.<sup>66</sup>

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{\max}$$

The estimated  $D_{it}$  values for the three devices are listed in Table III. Device A is expected to have the roughest starting surface and to have carbon contamination at the interface, and it has the largest  $D_{it}$  value of the three devices. Crystalline SZO in Device A comes closest to crystalline SHO with respect to the starting interface and contamination levels, and SZO has a  $D_{it}$  value that is less than  $\sim 4 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$  for SHO.<sup>10</sup>  $D_{it}$ , improved with a Zintl-templated surface and some form of atomic D treatment (Device B). The lowest  $D_{it}$  value of  $8.56 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$  was observed when an oxygen plasma was used to generate a flatter Ge (001) surface and



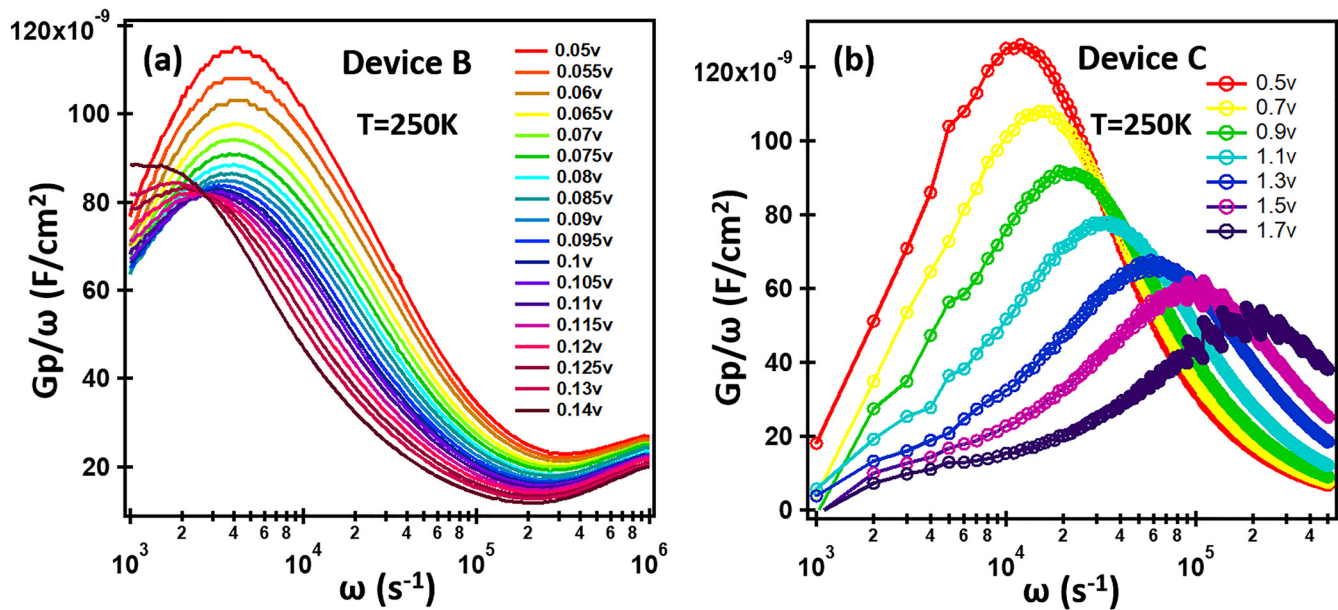


FIG. 9. The conductance  $G_p$  measured as a function of frequency and plotted as  $G_p/\omega$  versus  $\omega$ . (a) The  $G_p/\omega$  versus  $\omega$  plot for Device B. (b) The  $G_p/\omega$  versus  $\omega$  plot for Device C.  $G_p/\omega$  is normalized by the area of the top  $100\ \mu\text{m} \times 100\ \mu\text{m}$  square Pt electrode.

TABLE III.  $D_{it}$  values for the three devices.

Device	$D_{it}$ value ( $\text{cm}^{-2}\ \text{eV}^{-1}$ )
A	$4.07 \times 10^{12}$
B	$1.28 \times 10^{12}$
C	$8.56 \times 10^{11}$

suppress the Ge surface steps.<sup>30</sup> The steps could cause dangling bonds at the interface and APB formation within the epitaxial films.<sup>9</sup> The  $D_{it}$  investigation illustrates that steps can be taken to improve the electrical properties of crystalline perovskite-germanium interfaces, and additional studies may identify more optimal treatment conditions.

#### IV. CONCLUSION

Crystalline  $\text{SrZrO}_3$  (SZO) films have been deposited epitaxially on both bare Ge (001) and Ba Zintl-templated Ge (001) using ALD. Thick  $\text{SrZrO}_3$  films require two-step ALD growth. For SZO seed layer growth, bare Ge requires the cycle ratio of Sr:Zr = 3:2 and the Zintl template needs a heavier Sr cycle ratio of Sr:Zr = 2:1. Via this growth protocol, the annealing temperature of the SZO seed layer can be held to below  $640^\circ\text{C}$  to avoid interfacial reactions. The second layer of SZO can achieve crystallization during growth with a Sr:Zr = 3:2 cycle ratio and the crystal quality can be improved by post-deposition annealing at  $550^\circ\text{C}$ . Metal-oxide-semiconductor capacitor structures were used for electrical measurements. The SZO/Ge heterojunctions yield a dielectric constant of 30 and leakage current density of  $2.1 \times 10^{-8}\ \text{A}/\text{cm}^2$  at 1 MV/cm with an EOT = 0.8 nm, which gave the best electrical performance in the  $\text{SrBO}_3/\text{Ge}$  heterojunctions. In addition, this study also introduced oxygen plasma pretreatment to reduce the Ge surface roughness and

atomic D post treatment to heal the interface dangling bonds and achieve the lowest  $D_{it}$  value of  $8.56 \times 10^{11}\ \text{cm}^{-2}\ \text{eV}^{-1}$ .

#### SUPPLEMENTARY MATERIAL

See [supplementary material](#) for the in-plane XRD scan of a 11.5-nm SZO film, XRD, and XRR of a 27.7-nm SZO film, C-V characteristics of Devices A and B, and conductance as a function of frequency for Device A.

#### ACKNOWLEDGMENTS

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