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ABSTRACT

Analysis and mitigation of junction leakage currents are central to the engineering of vertical semiconductor diode structures. We have used scanning capacitance microscopy and conductive atomic force microscopy to characterize, with nanoscale spatial resolution, charge carrier distributions and local current distributions at the edges of mesa-etched and selective-area regrown vertical GaAs pn junction diodes grown by molecular-beam epitaxy. These studies indicate that wet etch-induced defect states are present on the etched surfaces of mesa structures, leading to increased local electrical conductivity that could contribute to sidewall leakage. For selective-area regrown structures, we observe an annular low-conductivity region in the vicinity of the GaAs–SiO_2 interface at the edge of regrown pn junction structures that could act to suppress current flow at the edges of pn junction diodes fabricated from selective-area regrown material. Together, these studies provide new insights into the origin of sidewall leakage currents in mesa-etched GaAs pn junction diodes and their suppression in selective-area regrown devices.

I. INTRODUCTION

Junction leakage currents play a critical role in semiconductor diodes and photodetectors. High leakage current can result in a shortened storage time in memory device applications,[1] introduce noise in imaging photodetectors,[2,3] and degrade the signal-to-noise ratio in charge-coupled devices.[4] Conversely, low-leakage devices can operate at elevated temperatures and have increased breakdown voltages and reduced power consumption.[5–9] For vertical p-n and p-i-n-type structures such as diodes or photodetectors, sidewall leakage current due to etch damage has been identified as one of the major sources of leakage current paths.[10–17] This damage includes defects from dislocation and impurities during fabrication processes. Dislocation defect density can range from 10^7 to 10^8 cm^{-2}.[18,19] Impurity density mainly varies by choice of the method of fabrication and choice of substrates. For example, impurities in the nucleation and growth process of the interface cause the formation of local traps. It is reported to range 10^{13}–10^{15} cm^{-3} in MBE grown GaAs on GaAs substrates.[20–22] To minimize leakage currents due to etch damage and enable more complex device designs, the selective-area growth technique has been extensively studied and applied.[23,24]

This study presents a detailed characterization of nanoscale charge carrier distributions and current flow in mesa-etched and selective-area regrown GaAs pn junction structures using scanning capacitance microscopy (SCM) and conductive atomic force microscopy (CAFM). For the mesa-etched structure, CAFM measurements reveal elevated current flow at the etched surface of the p-type layer compared to that for the unetched p-type surface and the underlying n-type layer. SCM measurements do not show evidence of a high density of surface or near-surface trap states, but reveal carrier spillover effects in the vicinity of the pn junction that influence the interpretation of SCM spectra in these regions. For the selective-area regrown structure, CAFM measurements reveal evidence of a highly resistive region near the perimeter of the selectively grown region. This highly resistive region may, effectively, passivate selective-area regrown devices from the effects of surface leakage at the perimeter of a device by suppressing current flow from the device interior to the perimeter, suggesting that selective-area regrowth holds promise for the

fabrication of diodes and photodetectors with very low-leakage currents.

II. EXPERIMENT

A. Sample structure

Two 300 nm-thick GaAs p-i-n junction diode structures were designed and fabricated for comparison of leakage currents in etched and selective-area regrown structures. For both, a 90 nm n-type GaAs layer was grown by molecular-beam epitaxy (MBE) with a dopant concentration of 1×10^{17} cm^{-3}, followed by a 90 nm unintentionally doped GaAs layer with a background dopant concentration of approximately 1×10^{16} cm^{-3}. Finally, a 120 nm p-type GaAs layer was grown with a dopant concentration of 1×10^{17} cm^{-3} ramped up in the last 30 nm to a concentration of 1×10^{18} cm^{-3}. For the mesa-etched structure, circular mesas of various diameters were created by wet etching to produce the structure as shown in Fig. 1(a), which we refer to as the "etched" structure. For the selective-area regrown structure, a 300 nm SiO_2 layer had been deposited and patterned with etched holes prior to MBE growth, to yield the structure shown in Fig. 1(b), which we refer to as the "regrown" structure. Both structures, thus, consisted of vertical p-i-n cylinders with diameters of 30, 50, and 100 μm.

B. Sample preparation

The GaAs pin diode was grown on an EPI Mod Gen II molecular-beam epitaxy system with a valved arsenic cracker. The material was grown at 615 °C with a growth rate of 0.25 μm/h and an As_4/Ga flux ratio of 20. Periodic supply epitaxy was used to ensure selective-area growth of GaAs by promoting the desorption of polycrystalline GaAs on SiO_2 during periodic interruptions in the Ga flux.[25,26] Periodic supply epitaxy cycles consisted of 30 s of GaAs growth followed by a 30 s pause in the Ga flux while maintaining the As flux. Silicon was used as the n-type dopant and beryllium was used as the p-type dopant. Dopant fluxes were supplied and interrupted concurrently with Ga to prevent the accumulation of dopants during growth pauses.

C. SPM measurements

SCM measurements were performed using a Bruker Dimension Icon atomic force microscopy system. DC bias voltages of −10 to +3 V with an AC bias voltage amplitude of 800 mV at 10 kHz were applied to determine the bias voltage dependence of carrier profiles. Conductive cobalt chromium tips (MESP-RC-V2, Bruker) were used for all SCM measurements. CAFM was performed using a Bruker Dimension Icon atomic force microscopy system in combination with a commercial current preamplifier (Ithaco 1211). Bias voltages of −4 to +3 V with 0.5 V step size were employed for the CAFM measurements. Conductive diamond coated tips (DDESP-V2, Bruker) were used for CAFM to minimize tip wear. Bias voltages were applied through the sample rather than through the tip to minimize degradation of the electric and physical quality of the tip.[27,28]

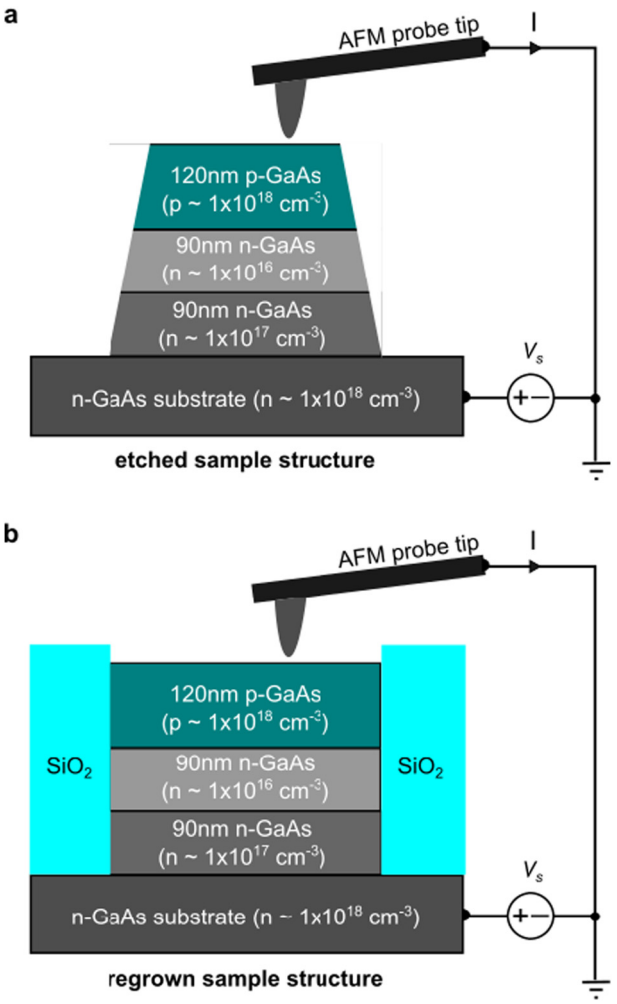

FIG. 1. Schematic diagrams of (a) etched and (b) selective-area regrown GaAs pin junction structures characterized by SCM and CAFM.

III. RESULT AND DISCUSSION

SCM measurements were used to investigate the carrier profiles of the etched sample and gain insights into the electronic structure of the etched sidewall surface. Figure 2(a) shows a schematic illustration of the sample and measurement geometry. Figure 2(b) shows a topographic line plot of the etched sample extracted from an atomic force microscope (AFM) topographic image (see Fig. S1 in the supplementary material). SCM images were obtained at DC bias voltages from −10 to +3 V (see Fig. S1 in the supplementary material). The SCM signal as a function of position and bias voltage, extracted from line cuts across each SCM image to provide a comprehensive representation of dC/dV as a function of bias voltage and sample location, is shown in Fig. 2(c). Note that there is an observation of line-to-line variation of the SCM signals in raster scans (see Fig. S1 in the supplementary material). Figure 2(d) shows line plots of the SCM signal as a

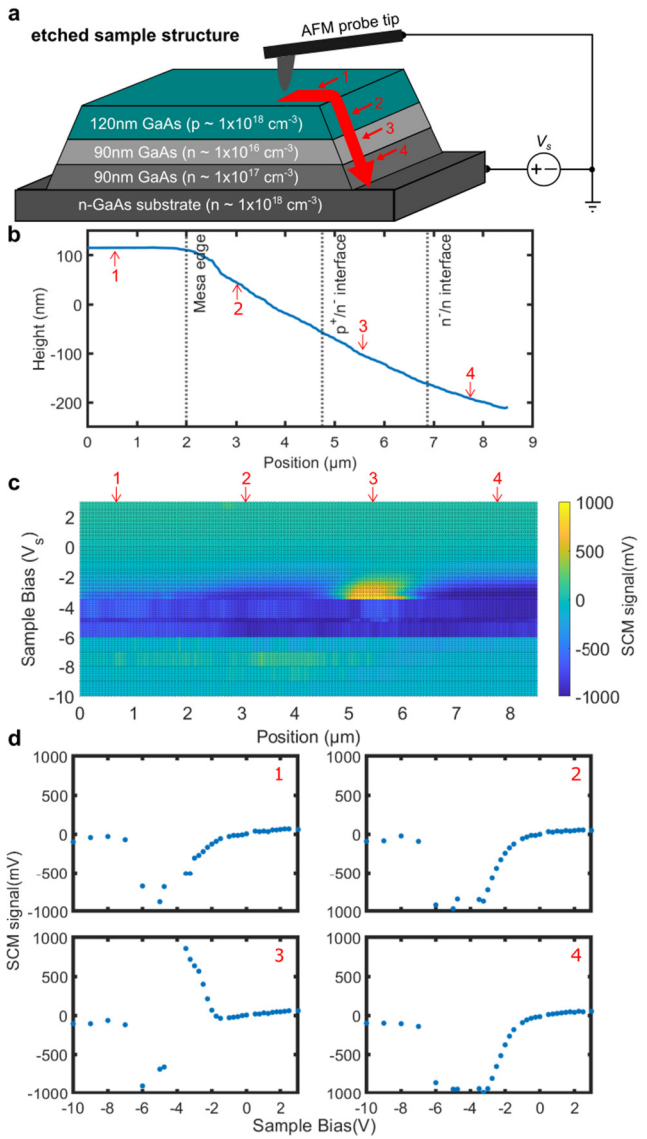

FIG. 2. (a) Schematic illustration of etched sample structure and SCM measurement geometry. (b) Surface topography measured by AFM with boundaries between p-type, unintentionally doped (n-), and n-type epitaxial layers indicated. (c) Scanning capacitance signal (in mV) measured as a function of sample bias voltage and sample position, referenced to horizontal positions in (a). (d) SCM signal spectra extracted from data in part (c) at locations indicated by numerical labels 1–4 in parts (a)–(c).

function of bias voltage, extracted from Fig. 2(c) at the four locations marked in Figs. 2(a)–2(c).

These four specific locations exhibit represent distinct electronic behaviors that are representative of the different regions of the etched structure as indicated in Fig. 2(a). The first location, marked as location 1, corresponds to the top of the mesa of the etched sample. Location 2 corresponds to the etched surface of the p-type layer, which has a graded dopant concentration resulting from the ramped acceptor incorporation. Location 3 corresponds to the unintentionally doped n^- region with the pn junction interface located at 4.7 μm along the horizontal axis. Location 4 corresponds to the etched surface of the n-type epitaxial layer.

To interpret the SCM measurements shown in Fig. 2, we note that the SCM signal is proportional to dC/dV_s, where V_s is the voltage applied to the sample relative to the grounded probe tip, averaged over the ac voltage modulation range. At zero sample bias ($V_s = 0$), pinning of the Fermi level at the GaAs surface for all locations leads to the formation of a depletion layer near the surface, resulting in a low value for both the capacitance and the corresponding SCM signal. Furthermore, the small size of the probe tip apex and the likely presence of surface states will increase the magnitudes of voltages required to modulate charges within the sample. Interpretation of the SCM signal spectrum is most straightforward for location 4, corresponding to the n-type GaAs layer. We observe that as Vs decreases, the capacitance gradually increases, resulting in negative values of dC/dV_s and of the SCM signal (see Fig. S1 in the supplementary material). For sufficiently negative values of V_s, electron accumulation occurs at the sample surface, resulting in a large, constant capacitance and small values for the SCM signal, as shown for location 4 in Fig. 2(d).

Very different SCM signal behavior is observed in location 3, which corresponds to the unintentionally doped GaAs region, but relatively close to the unetched or partially etched region of the p-type GaAs layer. At this location, proximity to the pn junction plays a key role in creating the observed SCM signal spectrum (see Fig. S2 in the supplementary material). At zero sample bias, the capacitance will be large due to the presence of holes that can spill over from nearby unetched p-type material. As Vs is decreased from zero, these holes are depleted, leading to a decrease in capacitance and a positive value for dC/dV_s. As V_s is further decreased, the depletion layer width in the sample decreases, leading to higher capacitance and a negative value for dC/dV_s. Finally, for sufficiently negative values of V_s, electrons accumulate at the sample surface, leading to a large, approximately constant capacitance and small values of dC/dV_s as shown for location 3 in Fig. 2(d).

Location 2 corresponds to the partially etched surface of the p-type GaAs layer with a relatively thin p-type region above the pn junction. At this location, the capacitance is small at zero sample bias due to Fermi level pinning at the GaAs surface. As V_s is decreased, we expect the thickness of the near-surface depletion layer to decrease and, simultaneously, the underlying pn junction to become forward-biased, both of which contribute to increasing capacitance and negative values for dC/dV_s (see Fig. S1 in the supplementary material). For sufficiently negative values of Vs, approximately constant capacitance and a correspondingly small value of dC/dV_s are observed, as shown for location 2 in Fig. 2(d). This could arise either from depletion extending through the p-type GaAs layer and past the pn junction or from electron accumulation at the etched surface due to carrier injection from the underlying n-type layer. Location 1 corresponds to the unetched surface of the p-type GaAs layer. The SCM signal spectrum observed in this location is similar to that observed for location 2, but with a smaller SCM signal amplitude, which we attribute to the higher p-type dopant concentration in this region of the sample structure.

The SCM measurements shown in Fig. 2 confirm the expected dopant distribution but do not show direct evidence of the presence of trap states that might influence sidewall leakage current. In contrast, CAFM measurements performed on the same structure suggest the presence of electrically conductive defect states on or near certain regions of the etched surface. We conjecture that the CAFM measurements are more sensitive, compared to SCM, to the presence of such defect states as their presence even in relatively low concentrations can have a substantial effect on local electrical conductivity. Figure 3(a) shows a schematic illustration of the sample and measurement geometry employed for CAFM measurements on the etched structure.

With a projected mesa length of 10 μm along the x-axis, the p-n- interface was situated at 5.1 μm, and the n^-–n interface at 7.6 μm as indicated in the topographic profile shown in Fig. 3(b). CAFM images were obtained at bias voltages from −4 to +5 V (see Fig. S3 in the supplementary material). Variations in CAFM signal from line to line have been observed. 500 nm in the y-axis at the center of the images has been selected to adequately represent each location (see Figs. S3 and S4 in the supplementary material). Figure 3(c) shows the measured local current as a function of position and bias voltage. Figure 3(d) shows current–voltage spectra extracted from the bias-dependent CAFM images at four selected locations, indicated in Figs. 3(a)–3(c). Location 1 corresponds to the top of the mesa of the etched sample. Location 2 corresponds to the etched surface of the p-type layer, which has a graded dopant concentration resulting from the ramped acceptor incorporation. Location 3 corresponds to the unintentionally doped n^- region with the pn junction interface located at 5.1 μm along the horizontal axis. Location 4 corresponds to the etched surface of the n-type epitaxial layer.

In location 4 (etched surface of n-type GaAs epitaxial layer), the current–voltage characteristic shown in Fig. 3(d) behaves as expected. For negative sample bias voltages, the tip–sample metal–semiconductor contact is forward-biased, and significant current begins to flow for V_s near −1 V. For positive sample bias voltages, we observe current flow at voltages of approximately 3 V and larger, corresponding to significant but not necessarily unexpected reverse-bias leakage current at the tip–sample contact. In location 3, corresponding to the etched surface of the unintentionally doped n^- region, we observe qualitatively similar current–voltage behavior as observed for location 4, but with lower overall electrical conductance arising from the reduced n-type dopant concentration in this region. Location 2 corresponds to the etched surface of the p-type GaAs layer. This region would be expected to exhibit a more negative turn-on voltage for current flow than location 3, as current flow would be associated with turn-on of the forward-biased pn junction below the surface, rather than the tip–sample metal-n-type semiconductor contact present at location 3. However, we observe turn-on of current flow at less negative sample bias voltages for location 2 compared to location 3, suggesting the presence of defects near the etched surface of region 2 that enable increased current flow. This behavior is observed across the entirety of the etched p-type surface region, suggesting that these defects are present on most or all of the etched surfaces of the p-type region. At location 1, corresponding to the unetched p-type surface, current flow is observed only for more negative sample bias voltages, as expected for p-type GaAs with an underlying pn junction. The increased magnitude of the turn-on voltage for the unetched p-type surface compared to that for the etched surface is also consistent with the presence of elevated electrical conductance associated with surface or near-surface etch damage in the p-type GaAs layer. The use of phosphoric acid (H_3PO_4) in the wet etching process may introduce morphologic enhancement, higher ideality factor, and higher dark current.[29–31]

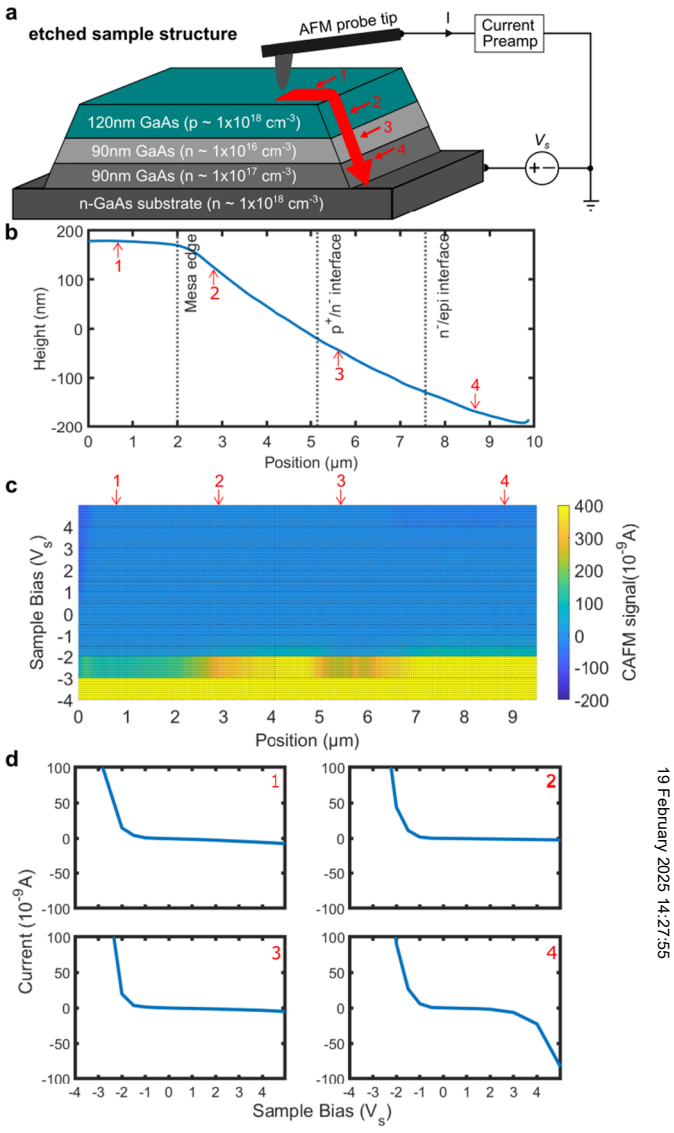

FIG. 3. (a) Schematic illustration of etched sample structure and CAFM measurement geometry. (b) Surface topography measured by AFM with boundaries between p-type, unintentionally doped (n-), and n-type epitaxial layers indicated. (c) Local electrical current measured as a function of sample bias voltage and sample position, referenced to horizontal positions in (a). (d) Local current–voltage characteristics extracted from data in part (c) at locations indicated by numerical labels 1–4 in parts (a)–(c).

Figure 4 shows a schematic illustration of the sample and measurement geometry employed for CAFM measurements on the regrown structure. AFM topographic and CAFM images were obtained for this structure at sample bias voltages ranging from −5 to 3 V (see Fig. S4 in the supplementary material), from which the topographic line profile shown in Fig. 4(b) was extracted. Some modulation of the surface height is observed near the GaAs–SiO_2 interface. This occurs because of the non-uniform diffusion of Ga adatoms and shadowing effects caused by the SiO_2 during growth.

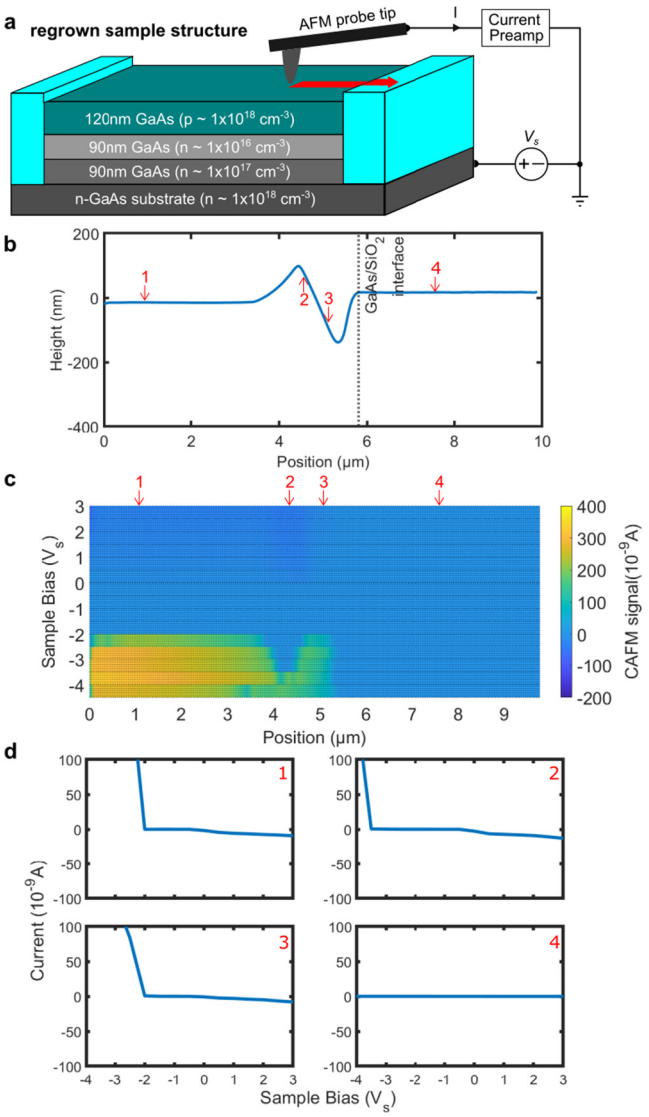

FIG. 4. (a) Schematic illustration of selective-area regrown sample structure and CAFM measurement geometry. (b) Surface topography measured by AFM with the boundary between GaAs and SiO_2 regions indicated. (c) Local electrical current measured as a function of sample bias voltage and sample position, referenced to horizontal positions in (a). (d) Local current–voltage characteristics extracted from data in part (c) at locations indicated by numerical labels 1–4 in parts (a)–(c).

However, cross-sectional SEM imaging of such samples (see Fig. S5 in the supplementary material) indicates that the full GaAs pn junction structure remains present in this region. Figure 4(c) shows the measured local current as a function of position and sample bias voltage, extracted from the CAFM images shown in Fig. S4 in the supplementary material. Figure 4(d) shows current–voltage characteristics extracted from the locations indicated in Figs. 4(a)–4(c). Location 1 corresponds to the regrown GaAs structure, away from the GaAs–SiO_2 interface. In this location, current–voltage behavior generally similar to that observed for the unetched top surface of the etched sample structure is observed. Turn-on of current flow at V_s of approximately −2 V occurs, corresponding to forward bias applied to the underlying pn junction. Very different behavior is observed at location 2. Here, much lower current flow and electrical conductance are observed at all sample bias voltages, with a turn-on of current flow at a negative sample bias voltage of approximately −4 V. Location 3 corresponds to the GaAs region adjacent to the GaAs–SiO_2 interface and exhibits current–voltage behavior similar to that observed in location 1, indicating that the region of decreased electrical conductance exemplified by location 2 is localized to an annulus near but not extending to the edge of the regrown GaAs region. Location 4 corresponds to the SiO_2 layer, for which, as expected, negligible current flow is observed. The observation at location 3 of increased turn-on voltage magnitude at negative sample bias with modest current flow for positive sample bias suggests the formation of a low-conductivity semiconductor region extending below the GaAs surface that would suppress current flow between the interior and edge of a diode device structure fabricated from the regrown GaAs region and correspondingly reduce the contribution of sidewall currents flowing at or near the GaAs–SiO_2 interface to the diode's reverse-bias leakage current.

IV. CONCLUSION

We have used SCM and CAFM to characterize local carrier distributions and electrical current flow in mesa-etched and selective-area regrown GaAs pn junction structures grown by MBE. These studies help to explain the origin of sidewall leakage currents observed in mesa-etched vertical pn junction diodes, and the absence of such currents in selective-area regrown devices. Specifically, CAFM characterization of the etched surface of the mesa-etched sample reveals that defect states are present on the etched surfaces of the mesa-etched structures and that these defects lead to increased local electrical conductivity that is expected to contribute to sidewall leakage currents that are frequently observed in etched mesa diode device structures. CAFM characterization of GaAs pn junction structures created by selective-area regrowth within SiO_2 cavities on GaAs substrates reveals the presence of an annular low-conductivity region in the vicinity of the vertical GaAs–SiO_2 interface at the edge of the pn junction diode that could act to suppress current flow at the edges of pn junction diode device structures fabricated from selective-area regrown material. Together, these studies provide insights into the origins of sidewall leakage currents in mesa-etched GaAs pn junction diodes, and their suppression in selective-area regrown devices by observation of low conductivity region near the periphery of the GaAs–SiO_2 interface. Finally, SCM measurements performed on pn junction

cross sections exposed by mesa etching reveal unique aspects of measurements on exposed cross sections of pn junction structures due to carrier motion within the sample in directions parallel to the tip axis. Specifically, tip bias-induced carrier spillover effects from p- or n-type electrode regions into the pn junction depletion region produce unusual SCM contrast and spectroscopic behavior near the exposed pn junction cross section. These observations are expected to help inform the interpretation of cross-sectional scanned probe measurements of a variety of electronic device structures at submicrometer to nanometer scales.

SUPPLEMENTARY MATERIAL

See the supplementary material for additional information about the SCM and KPFM images, SCM analysis method with energy band diagram, and the SEM image of regrown GaAs pn junction near the GaAs/SiO_2 interface.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Tae-Hyeon Kim: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Alec M. Skipper:** Conceptualization (supporting); Formal analysis (supporting); Investigation (equal); Methodology (supporting); Resources (lead). **Seth R. Bank:** Conceptualization (equal); Formal analysis (supporting); Funding acquisition (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – review & editing (supporting). **Edward T. Yu:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Project administration (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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