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Cross-sectional scanning thermal microscopy of ErAs/GaAs superlattices grown by molecular beam epitaxy

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Abstract

Scanning thermal microscopy has been implemented in a cross-sectional geometry, and its application for quantitative, nanoscale analysis of thermal conductivity is demonstrated in studies of an ErAs/GaAs nanocomposite superlattice. Spurious measurement effects, attributable to local thermal transport through air, were observed near large step edges, but could be eliminated by thermocompression bonding to an additional structure. Using this approach, bonding of an ErAs/GaAs superlattice grown on GaAs to a silicon-on-insulator wafer enabled thermal signals to be obtained simultaneously from Si, SiO_2, GaAs, and ErAs/GaAs superlattice. When combined with numerical modeling, the thermal conductivity of the ErAs/GaAs superlattice measured using this approach was $11 \pm 4\ \mathrm{W\,m^{-1}\,K^{-1}}$.

S Online supplementary data available from stacks.iop.org/NANO/26/265701/mmedia

Keywords: scanning thermal microscopy, ErAs/GaAs superlattice, thermal conductivity

(Some figures may appear in colour only in the online journal)

1. Introduction

Developments in the understanding and engineering of thermal properties of materials at the nanoscale [1–9] have led to increased interest in methods for quantitative characterization of thermal transport behavior with high spatial resolution [10–12]. Among the different types of nanostructures exhibiting altered thermal transport behavior compared to their bulk-like counterparts, crystalline semiconductors in which nanoparticles or other nanoscale structures are incorporated via epitaxial growth are of particular interest due to their potential for use in thermoelectric devices [6, 7, 13–15] or for integration of structures possessing particular thermal properties with high-performance electronic or optoelectronic devices. In addition, recent studies of $Si/Si_{1-x}Ge_x$ superlattices have suggested that layer design can dramatically alter thermal transport characteristics [5, 16], and there has been work suggesting that quantum-well and quantum-dot structures can produce large reductions in thermal conductivity that impact thermal transport and thermal management in semiconductor heterostructure devices [17–19].

In such structures, characterization of thermal conductivity in subsurface regions and of local variations in thermal conductivity presents a particular metrological challenge. For epitaxial semiconductor structures, scanning probe microscopy (SPM) is typically employed with the sample in an in-plane geometry that provides access only to the epitaxially grown surface [10, 11, 20, 21]. Here, we present studies in which nanoscale cross-sectional thermal measurements are demonstrated that enable direct measurement and comparison of thermal properties across multiple materials via the 3ω technique combined with SPM [10–12, 21]. By cleaving and, if needed, polishing to expose a smooth cross-sectional surface, properties of material beneath the final epitaxially grown surface can be characterized. In this measurement configuration, we can directly characterize thermal, electronic, and other material properties of interfaces and buried layers in heterostructures using scanned probe microscopy [22–24]. In this study, an ErAs/GaAs superlattice

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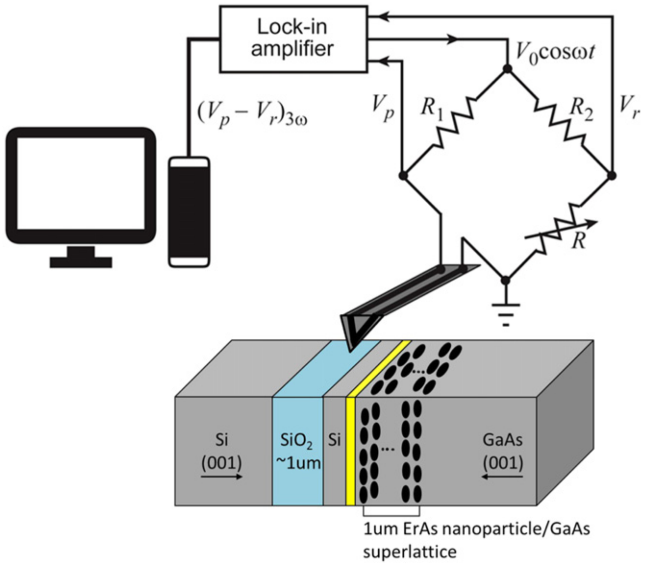

Figure 1. Schematic diagram of sample geometry, scanned thermal probe 3ω measurement apparatus, and associated electronic circuitry.

structure was employed in our analysis of thermal characteristics since the given structure is a highly promising candidate for thermoelectric devices application [25] because of the semimetallic properties of ErAs embedded in GaAs combined with decreasing thermal conductivity due to the phonon scattering from the ErAs/GaAs nanostructures [11, 15].

2. Experimental method

A schematic of the cross-sectional sample structure and scanning thermal measurement setup is shown in figure 1. The measurement apparatus and experimental geometry are analogous to those for the in-plane 3ω proximal probe method [11]. In brief, a functionalized thermal probe tip, VITA-DM-GLA-1 from Bruker, on which a thin patterned Pd film was fabricated on the Si_3N_4 substrate, was electrically excited at a frequency ω. The electrical excitation induced Joule heating of the thermal probe at frequency 2ω and a corresponding resistance variation in the thermal probe with frequency 2ω [10, 12, 26, 27]. To detect temperature variations, the thermal probe was connected to one arm of a Wheatstone bridge circuit, as shown in the schematic of figure 1, with two other resistors, R_1 and R_2, of known value and one variable resistor used to balance the bridge. Temperature changes of the thermal probe caused its resistance to change and the differential signal V_p–V_r at the 3rd harmonic frequency 3ω, which contains temperature information, was detected by a Sr-830 lock-in amplifier and used to monitor the thermal interaction between probe tip and sample.

The ErAs/GaAs superlattice structure employed in this work was grown by solid-source molecular beam epitaxy (MBE) in a Varian Gen II system. The sample structure consisted of a 150 nm undoped GaAs buffer layer grown at 580 °C on a semi-insulating GaAs (001) substrate, followed by a ~1000 nm ErAs/GaAs superlattice consisting of 200 repetitions of 0.25 monolayer (ML) ErAs and 5 nm GaAs grown at 530 °C. Under these growth conditions, the ErAs layers form 3–4 ML (~0.9–1.1 nm) high nanoparticles [28, 29], leading to an average fill factor of ~6% for each ErAs layer. The exposed GaAs layer remaining after each ErAs deposition seeds the GaAs overgrowth, allowing high-quality overgrowth of the ErAs nanoparticles [30]. The surface of the ErAs/GaAs superlattice structure is covered by a 15 nm GaAs capping layer to prevent oxidation.

Initial SThM measurements were performed with a cross-section of the ErAs/GaAs superlattice structure after cleaving the sample and rotating it to access the cross-section of the sample area of interest as shown in supplementary figure 1. Initial dc scanning thermal microscope data showed that a thermal signal response was observed near the edge region where the ErAs/GaAs superlattice is located. However, the thermal signal observed in this configuration is actually an artifact originating from heat transfer to air at the edge of the sample structure, and is not due to the ErAs/GaAs superlattice sample itself, as shown in supplementary figure 2. (See supplementary information for detailed discussion.)

To eliminate this undesirable edge effect, additional samples were prepared using thermocompression bonding to bond ErAs/GaAs superlattice epitaxial layer structures front-to-front with another solid-state structure; a silicon on insulator (SOI) wafer was employed for this purpose so that multiple materials with different thermal conductivities could be imaged simultaneously. This approach enabled the epitaxial layers of interest to be embedded within a sample region away from any edges, and eliminated the spurious edge-induced signal variation in the sample region of interest. For the thermocompression bonding process, 30 nm Ti followed by 250 nm Au was deposited on both the superlattice and SOI wafer surfaces, with the Ti acting as an adhesion and diffusion-blocking layer [31]. The wafers, approximately 1.3 × 1.3 cm in area each, were then held together with a force of 2 kN at 320 °C for 15 min in a vacuum chamber. The bonded structure was then cleaved, and the exposed cross-sectional surface polished with 3 μm, 1 μm, and then 300 nm grit size polishing paper. This process routinely yielded polished surfaces with ~6 nm rms surface roughness. It is important to have a very flat sample surface after the polishing process, since the thermal signal can be susceptible to crosstalk from topographic features.

3. Experimental results and discussion

Figure 2(a) shows a schematic diagram of the bonded cross-sectional sample structure, along with topographic and 3ω voltage signal ($V_{3\omega}$) images obtained at an excitation frequency $f = \omega/2\pi$ of 1.2 kHz and ac voltage amplitude of 0.75 V. Measured total electrical resistance of thermal probe was 364 Ω. NiCr limiter resistance is 200.34 Ω and Pd thermal probe tip resistance is 163.66 Ω, respectively. During the data collection, to maintain a same loading force, deflection

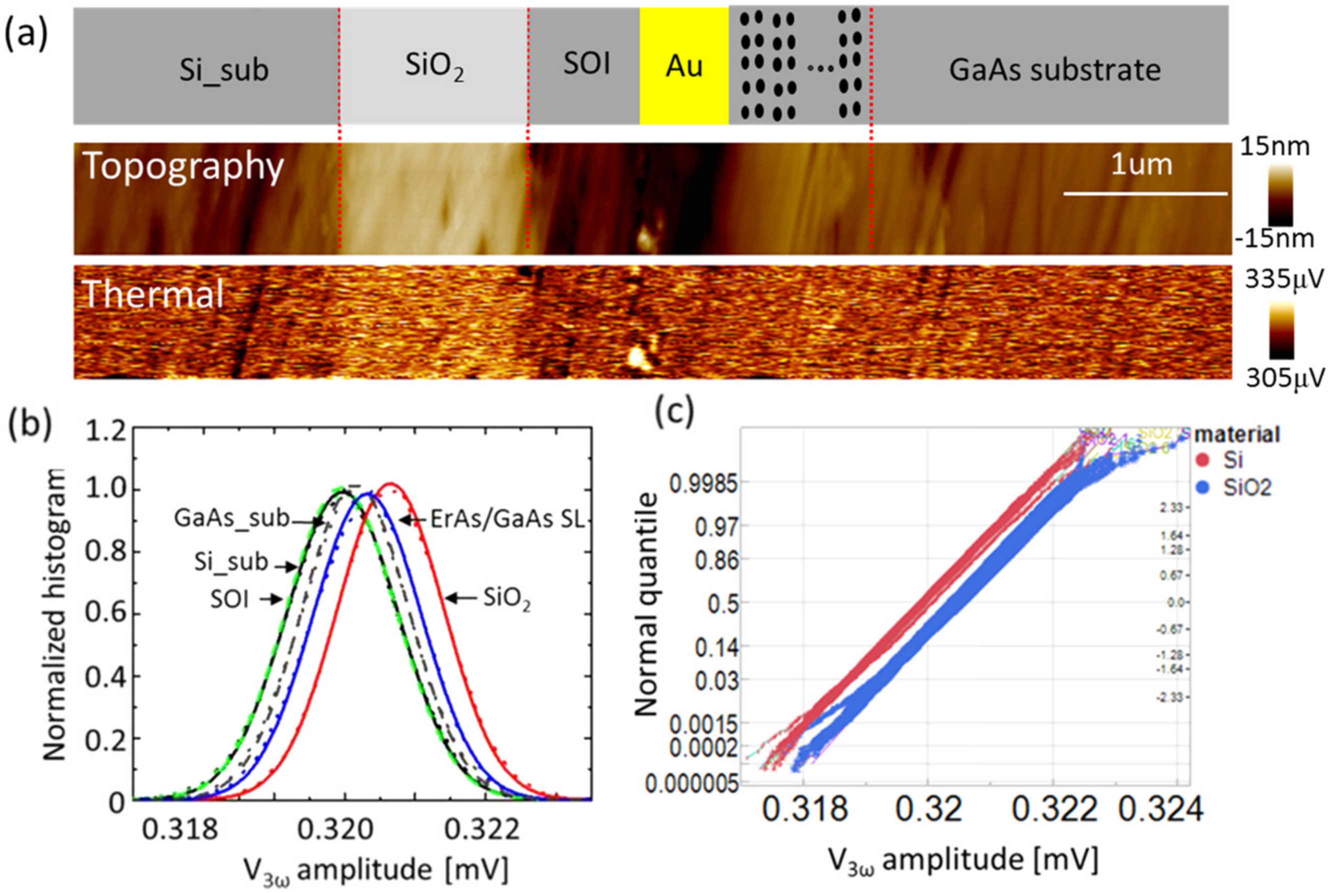

Figure 2. Cross-sectional scanning thermal microscopy of bonded SOI and ErAs/GaAs superlattice structure. (a) Schematic diagram of sample and measurement geometry, and topographic and thermal images of cross-sectional surface. (b) Normalized histograms (dots) for each designated region and fits to Gaussian distributions for each (lines and dashes). (c) Normal quantile plots for multiple measurements performed on 1000 × 1000 nm cross-sectional areas of the Si substrate (red) and SiO_2 layers (blue).

set point was set to 0.3. The cross-sectional area in the image encompasses, from left to right in the images, the Si substrate region of the SOI wafer, the buried oxide layer, thin Si layer, Au bonding layers, ErAs/GaAs superlattice, and GaAs buffer layer and substrate. Figure 2(b) shows normalized histograms of $V_{3\omega}$ signal amplitudes and Gaussian fits to these distributions for each designated region. From each material region, we take the peak position of the Gaussian distribution to be the signal level corresponding to that material. To assess the experimental uncertainty in determining this signal level for each material, we obtained multiple measurements for each material and compared the signal level distributions for each. Figure 2(c) shows a normal quantile plot of multiple measurement results for Si and SiO_2 sample regions [32, 33]. From the quantile plot, we can check that each material's thermal responses are normally distributed and they have clearly different distributions even though the width of each Gaussian distribution in figure 2(b) is quite large compared to their mean difference. T-tests for each material in figure 2(b) also confirm that their distributions are distinct.

Since each data point in thermal images such as those shown in figure 2(a) is influenced by a variety of factors including measurement duration, local surface roughness, and measurement noise, averaging a large number of points in an image for each material to obtain the average signal level, corresponding to the peaks of the Gaussian distributions shown in figure 2(b) and the 50th percentile values in figure 2(c), yields a characteristic signal level for that material. We then take the variation in this characteristic signal level across multiple measurements obtained in this manner to be the experimental uncertainty in determining this characteristic signal level for a given material.

Detailed modeling of thermal transport in the probe tip and sample structure, combined with model parameter calibration using $V_{3\omega}$ signals measured for materials of known thermal conductivity, enables quantitative, local determination of thermal conductivity in an unknown material [10–12]. We assumed a point contact of the thermal probe on the flat surface [11, 34]. Figure 3 shows the $V_{3\omega}$ amplitude calculated using such a model, following the approach of [11], along with the signal amplitudes for GaAs, SiO_2, Si substrate, thin Si layer, and ErAs/GaAs superlattice extracted from multiple measurements for each material in the manner described above. Au layer data fitting was intentionally excluded in the plot, since the thermal conductivity response is limited for high thermal conductivity materials [11, 35] as shown in figure 3. For GaAs, SiO_2, and the two Si layers, these values are plotted as a function of their known thermal conductivity.

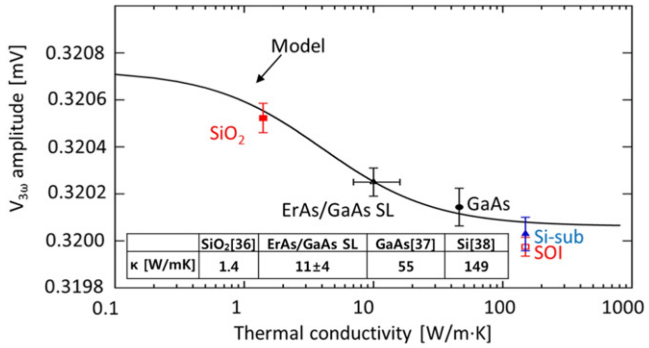

Figure 3. $V_{3\omega}$ amplitude predicted by numerical modeling and calibration to known thermal conductivities for Si, SiO$_2$, and GaAs (solid line), and measured mean values of $V_{3\omega}$ for SiO$_2$, ErAs/GaAs superlattice, GaAs, Si substrate, and thin Si layer. Horizontal positions of the measured signals were determined by using known thermal conductivities for GaAs, Si, and SiO$_2$, and by fitting to the numerical model for the ErAs/GaAs superlattice and corresponding thermal conductivity values are given in inset table.

As shown in figures 2(b) and (c), each material distribution is distinct and the mean value for each represents that material's thermal properties; multiple measurements for each material provided confidence intervals for each material's signal level. The vertical error bars in figure 3 correspond to the statistical distribution of mean values from multiple measurements for each material as described above. For SiO$_2$, GaAs, and Si, the material thermal conductivities were assumed to correspond to their established values which are given in the table in figure 3. The solid curve in figure 3 corresponds to the model for $V_{3\omega}$ signal response as a function of sample thermal conductivity, calibrated using the known thermal conductivities and measured signal values for GaAs, SiO$_2$, and Si. The thermal conductivity of the ErAs/GaAs superlattice is then taken to be that predicted by the calibrated model for the signal level measured experimentally for the superlattice. The resulting thermal conductivity of ErAs/GaAs, $11 \pm 4\ \mathrm{W\,m^{-1}\,K^{-1}}$ with confidence interval of 95%, agrees well with that determined from separate measurements reported elsewhere [11] and provides confirmation of the ability to obtain quantitative, local measurements of thermal conductivity in a cross-sectional geometry.

4. Conclusion

In conclusion, we have demonstrated the use of scanning thermal microscopy in a cross-sectional sample geometry to perform quantitative analysis of thermal conductivity in ErAs/GaAs superlattices grown by MBE. In doing so, we have elucidated the effects of thermal transport behavior near large topographic features such as abrupt edges or deep trenches in producing scanning thermal microscopy measurement artifacts, and shown that these effects can be eliminated by fabricating sample structures in which the epitaxial layers of interest are positioned away from the sample edge by bonding to an additional wafer followed by cleaving and polishing of the exposed cross-sectional surface. Furthermore, these measurements demonstrate an approach that allows thermal conductivity to be characterized for buried layers in semiconductor heterostructures, opening up the possibility of performing such measurements for a broad range of heterostructures, nanostructures, and semiconductor devices. We have obtained a room-temperature thermal conductivity for the ErAs/GaAs superlattice structure studied here of $11 \pm 4\ \mathrm{W\,m^{-1}\,K^{-1}}$, which confirms that ErAs/GaAs superlattice structures are able to reduce the thermal conductivity of the host material, GaAs, due to phonon scattering from ErAs nanoparticles.

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