Trap characterization by gate-drain conductance and capacitance dispersion studies of an AlGaN/GaN heterostructure field-effect transistor

E. J. Miller, X. Z. Dang, H. H. Wieder, P. M. Asbeck, and E. T. Yu[a)]
Department of Electrical and Computer Engineering, University of California San Diego, La Jolla, California 92093-0407

G. J. Sullivan
Rockwell International Science Center, Thousand Oaks, California 91358

J. M. Redwing
Epitronics/ATMI, Phoenix, Arizona 85027

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Gate-drain capacitance and conductance measurements were performed on an $Al_{0.15}Ga_{0.85}N/GaN$ heterostructure field-effect transistor to study the effects of trap states on frequency-dependent device characteristics. By varying the measurement frequency in addition to the bias applied to the gate, the density and time constants of the trap states have been determined as functions of gate bias. Detailed analysis of the frequency-dependent capacitance and conductance data was performed assuming models in which traps are present at the heterojunction (interface traps), in the AlGaN barrier layer (bulk traps), and at the gate contact (metal–semiconductor traps). Bias-dependent measurements were performed at voltages in the vicinity of the transistor threshold voltage, yielding time constants on the order of 1 μs and trap densities of approximately $10^{12}\,cm^{-2}\,eV^{-1}$. © *2000 American Institute of Physics.* [S0021-8979(00)01711-4]

I. INTRODUCTION

Devices based on nitride semiconductor compounds are very desirable for high-power applications because the relatively high thermal conductivity, high breakdown field, and large energy band gap of GaN and AlGaN lead to the possibility of device operation at high-power levels and elevated temperatures and at microwave frequencies.[1] Outstanding dc and rf characteristics have been reported for nitride-based heterostructure field-effect transistors (HFETs),[2–6] but at high frequencies, power compression can occur and the rf characteristics that are predicted based on dc operation are often not realized.[7] A possible factor contributing to this decrease in power output is the presence of traps in the heterostructure, which can introduce a voltage delay in the transistor's response and prevent the voltage from being modulated along the full extent of the dc load line. The decreased voltage swing leads to a smaller variation in current and, therefore, less power output from the device. Detailed studies of the traps in nitride-based HFETs are therefore necessary to understand the impact of trap states on device performance at high frequencies.

Frequency-dependent measurements of the capacitance and conductance of semiconductor structures have been successfully employed to investigate trap states in GaAs and GaSb,[8,9] and studies of the conductance dispersion in an HFET gate-drain diode have been useful in understanding traps in the InAlAs/InP system.[10] Capacitance and conductance studies are particularly appropriate for determining the effects of traps. The filling and emptying of trap states produces an energy loss which causes a measurable change in the conductance of the structure. This loss is caused by electrons in the conduction band filling trap states in the band gap which are at a lower energy or by electrons in trap states being emitted into lower energy valence band states.[11] As traps are filled and emptied, the measured capacitance is also affected by the charge stored in these states. By performing investigations at different modulation frequencies, it is possible to extract explicitly the density of traps and the characteristic times for trap charging and discharging processes.

There are four main possibilities to consider for the spatial location of traps in the HFET structure: the metal–semiconductor interface of the gate contact, the bulk of the barrier layer, the interface between the barrier layer and the channel, and the bulk of the channel layer. Since it is impossible to know where the traps are located *a priori*, all four locations must be considered. By selecting a range of voltages which did not significantly deplete the GaN layer, the effects of trap states in the channel layer could be eliminated in our studies. Interface traps at the oxide–semiconductor interface in metal–oxide–semiconductor (MOS) structures have been extensively studied using the conductance method, and the model describing them is well understood.[11] Adapting the model to HFETs with traps located at the heterojunction (referred to as interface traps herein) is straightforward, and thus this model has been used as a starting point for these investigations and altered as necessary to account for traps in other locations.

Section II describes the measurement technique and the method used to extract trap parameters from the data. In Sec. III, information about the trap states is presented and interpreted. Section IV concludes the article.

[a)]Electronic mail: ety@ece.ucsd.edu

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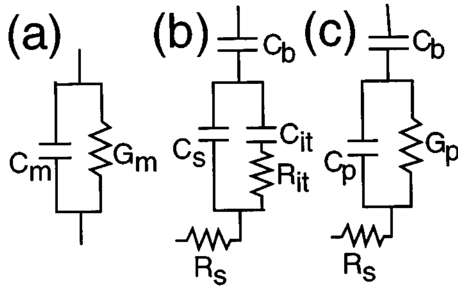

FIG. 1. Models of the HFET structure used to extract trap parameters from the experimental measurements. To make parameter extraction from the measurement circuit (a) more straightforward, the assumed model with the trap states (b) is converted to a simplified circuit (c).

II. EXPERIMENTAL PROCEDURE

The epitaxial layer structure employed in these studies was grown using metalorganic chemical vapor deposition and consisted of a 300 Å $Al_{0.15}Ga_{0.85}N$ barrier layer doped with Si at a concentration of $2\times10^{18}\,cm^{-3}$, an undoped, 100 Å $Al_{0.15}Ga_{0.85}N$ spacer layer, and a 3 μm, undoped GaN channel layer on a sapphire substrate. Details concerning the initial buffer layer and growth conditions are described elsewhere.[12] Transistor structures were fabricated with Pt/Au as the gate metal and Ti/Al/Pt/Au annealed at 800 °C for 60 s for the ohmic source and drain contacts. Measurements were performed on the gate-drain diode of large-area transistors, with gate lengths of 50 μm and gate widths ranging from 50 to 150 μm. Measurements of the gate-drain conductance G and the gate-drain capacitance C as functions of frequency were performed using HP 4284A and HP 4285 A precision LCR meters, which provided a range of measurement frequencies extending from 20 Hz to 30 MHz. Results are shown for measurements at frequencies ranging from 25 kHz to 1 MHz. To account for the stray capacitance of the cables, an open and short circuit correction were done for each measurement frequency.

The capacitance and conductance of the gate-drain diode were measured simultaneously assuming a parallel combination of C and G as shown in Fig. 1(a). The method described by Schroder for MOS capacitor analysis[13] has been adapted for these studies to the analysis of HFET structures with interface traps in the manner outlined below. The full circuit model of the HFET structure employed in our analysis is shown in Fig. 1(b), where C_b is the barrier capacitance, C_s is the capacitance of the spacer layer near the heterojunction, R_s is the series resistance of the drain contact, and $C_{\rm it}$ and $R_{\rm it}$ are the interface trap capacitance and associated loss term for the traps. It is useful to represent the full circuit of Fig. 1(b) by the simplified circuit of Fig. 1(c) because, as described below, C_p and G_p can be extracted directly from the measurement circuit shown in Fig. 1(a). By plotting these quantities as functions of frequency and fitting the resulting curves to equations derived by ac analysis for the circuit in Fig. 1(b), the interface trap density $D_{\rm it}$ and trap state time constant τ may be extracted. The analysis may be performed assuming the trap states comprise a single energy level or a continuum of levels. For the case of trap states at only a single energy level, C_p and G_p/ω are given by

$$C_p=C_s+\frac{C_{\rm it}}{1+(\omega\tau)^2}, \tag{1a}$$

$$\frac{G_p}{\omega}=\frac{q\omega\tau D_{\rm it}}{1+(\omega\tau)^2}, \tag{1b}$$

whereas, for a continuum of levels, they are given by

$$C_p=C_s+\frac{C_{\rm it}}{\omega\tau\tan(\omega\tau)}, \tag{2a}$$

$$\frac{G_p}{\omega}=\frac{qD_{\rm it}}{2\omega\tau}\ln[1+(\omega\tau)^2]. \tag{2b}$$

Equations (2a) and (2b), derived for a continuum of levels, provided a better fit to the values of C_p and G_p/ω we obtained, and are therefore used for the analysis.

The influence of series resistance on capacitance measurements in gate-drain diodes has been studied and shown under certain circumstances to be quite significant; it is possible, however, to account for series resistance effects using either a simple lumped-element equivalent circuit or a more elaborate distributed RC network.[14] The lumped-element model may be used for contacts and measurement frequencies for which $\omega RC\ll1$. In these studies, measurement and analysis were performed for $\omega<10^7\,s^{-1}$. Further, we take $\epsilon\approx9\times10^{-13}$ F/cm for the AlGaN barrier and assume a depletion layer width $d\geq10^{-7}$ cm under the drain contact. Using these values combined with a very conservative estimate for the contact resistance ($R_c<10^{-4}\,\Omega\,cm^2$), we obtain $\omega RC=\omega R\epsilon A/d=\omega R_c\epsilon/d<0.01$ for the drain contact. Therefore, even if we assume a relatively poor contact resistance and large capacitance for the contacts, over the measured range of frequencies a lumped-element equivalent circuit can be used to extract the values of C_p and G_p directly from our measurements. This is accomplished by including a resistor R_s in the circuit model in series with the rest of the circuit as shown in Figs. 1(b) and 1(c). In extracting C_p and G_p from our measurements using the assumed measurement circuit configuration of Fig. 1(a), it is necessary to account for both the series resistance and the barrier capacitance. A comparison between the equivalent circuits shown in Figs. 1(c) and 1(a) yields explicit expressions for C_p and G_p/ω, which are given in terms of C_m, G_m, R_s, and C_b by

$$C_p=\frac{-C_b[(C_m^2-C_mC_b)\omega^2+G_m^2]}{\omega^4C_m^2C_b^2R_s^2+\omega^2(C_b^2R_s^2G_m^2+C_m^2+C_b^2-2C_b^2R_sG_m-2C_mC_b)+G_m^2}, \tag{3a}$$

$$\frac{G_p}{\omega}=\frac{-\omega C_b^2(R_sC_m^2\omega^2+R_sG_m^2-G_m)}{\omega^4C_m^2C_b^2R_s^2+\omega^2(C_b^2R_s^2G_m^2+C_m^2+C_b^2-2C_b^2R_sG_m-2C_mC_b)+G_m^2}. \tag{3b}$$

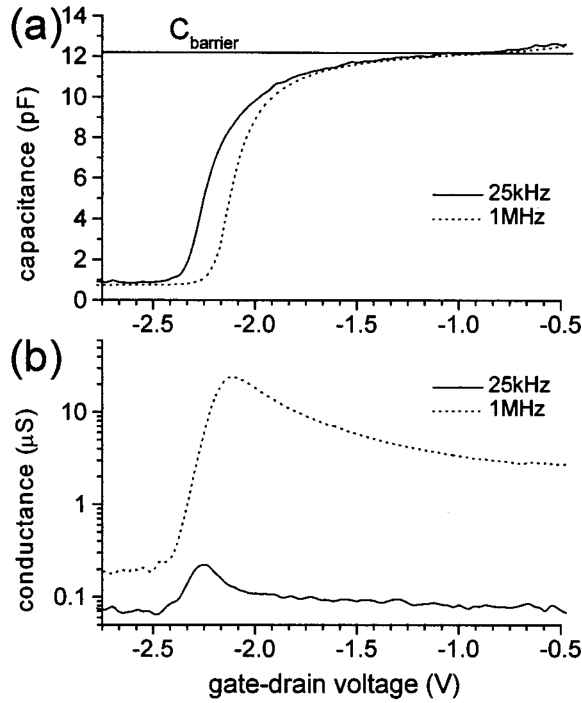

FIG. 2. Typical (a) capacitance and (b) conductance data for high frequency (dashed line) and low frequency (solid line) showing the dispersion that occurs over the measured frequency range.

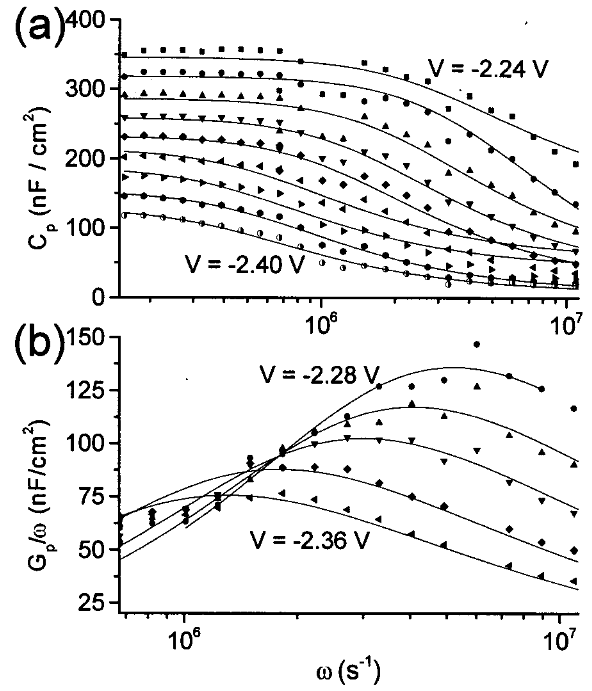

FIG. 3. Data for (a) the capacitance C_p and (b) conductance G_p/ω elements of the circuit shown in Fig. 1(c), extracted from measured data and adjusted to account for the presence of the barrier capacitance and series resistance. Fitted curves are also shown for each voltage series.

Thus, by measuring R_s and C_b in addition to C_m and G_m, the quantities C_p and G_p/ω can be extracted. The series resistance was calculated as a function of gate bias by taking $I-V$ measurements and determining the resistance from the slope of the curves near the origin. The value of the barrier capacitance was determined from the plateau in the gate-drain $C-V$ curve associated with accumulation of electrons in the two-dimensional electron gas channel.

III. RESULTS AND DISCUSSION

Typical $C-V$ and $G-V$ curves are plotted in Fig. 2 for frequencies of 25 kHz and 1 MHz. The dispersion is clearly apparent for the range of frequencies shown. The values of C_p and G_p/ω calculated from the measured capacitance, conductance, series resistance, and barrier capacitance are plotted in Fig. 3 for selected voltages near the threshold voltage. The curves that were fitted to these data using Eqs. (2a) and (2b) are also shown in Fig. 3. Fitting C_p vs ω yields values for C_s, C_{it}, and τ. The trap density D_{it} can be calculated using the relation $D_{\mathrm{it}}=C_{\mathrm{it}}/q$. Alternatively, D_{it} can be obtained from measured low- and high-frequency capacitance curves using the relation[13]

$$D_{\mathrm{it}}=\frac{C_b}{q}\left(\frac{C_{\mathrm{lf}}/C_b}{1-C_{\mathrm{lf}}/C_b}-\frac{C_{\mathrm{hf}}/C_b}{1-C_{\mathrm{hf}}/C_b}\right). \quad (4)$$

The time constant and trap density may also be obtained from the conductance data by fitting the measured values for G_p/ω versus ω using the expression given in Eq. 2(b). The results obtained using both the capacitance and conductance methods are in reasonable agreement, yielding values for the time constant of $\sim 1\ \mu$s and for the interface trap density D_{it} of $\sim 10^{12}\ \mathrm{cm}^{-2}\,\mathrm{eV}^{-2}$.

Further analysis was performed to address the possibility that the traps may be located in the bulk of the barrier layer or at the metal–semiconductor interface. Specifically, the branch of the circuit diagram in Fig. 1(b) containing the trap capacitance and loss element was placed first in parallel with the entire barrier capacitance, and second in parallel with a small part of the barrier capacitance near the metal–semiconductor interface, corresponding to the two other possible spatial locations for the traps. Analysis of these circuit models was more complicated because the parameters C_p and G_p of Fig. 1(c) could not be extracted due to the unknown capacitance C_s taking the place of the previously measurable element C_b. Thus, instead of extracting C_p and G_p as an intermediate step, the measured values of capacitance and conductance were fitted directly to expressions involving the trap parameters.

The expressions

$$C_m=\frac{C_s[C_b(C_b+C_s)(1+(\omega\tau)^2)+C_{\mathrm{bt}}(C_{\mathrm{bt}}+2C_b+C_s)]}{(C_b+C_s)^2(1+(\omega\tau)^2)+C_{\mathrm{bt}}(C_{\mathrm{bt}}+C_b+2C_s)}, \quad (5a)$$

$$\frac{G_m}{\omega}=\frac{C_{\mathrm{bt}}C_s^2\omega\tau}{(C_b+C_s)^2[1+(\omega\tau)^2]+C_{\mathrm{bt}}(C_{\mathrm{bt}}+C_b+2C_s)} \quad (5b)$$

were used for the analysis based on the bulk trap model where C_{bt} is the bulk trap capacitance. Similar expressions were used for the analysis based on the metal–semiconductor interface trap model. The trap density and time constant could then be extracted directly from the fits.

The expressions were derived in two steps. First, we found C_p and G_p/ω in terms C_s, C_m, G_m, and ω by a comparison of the new circuit model with the circuit in Fig. 1(c) with C_s replacing C_b and neglecting R_s. The expressions for C_p and G_p/ω were then equated to Eqs. 1(a) and 1(b) and solved for C_m and G_m/ω. Series resistance effects were accounted for in C_m and G_m with the basic correction[13]

$$C_m=\frac{C_m'}{(1+R_sG_m')^2+(\omega R_sC_m')^2}, \tag{6a}$$

$$G_m=\frac{G_m'(1+R_sG_m')+R_s(\omega C_m')^2}{(1+R_sG_m')^2+(\omega R_sC_m')^2}, \tag{6b}$$

where C_m' and G_m' are the actual measured values. This analysis yielded values for the bulk trap density and metal–semiconductor interface trap density that were very consistent with the values obtained using the interface trap model. The time constants that were obtained with the bulk trap and metal–semiconductor interface trap models were also approximately the same as the time constants from the interface trap model.

To determine the plausibility of our measured values for the trap density and time constant, we note first that the dispersion in the capacitance and conductance occurred primarily for measurement frequencies ranging from 50 kHz to 1 MHz. The effects of trap states with a time constant of $\sim$1 μs would be expected to be exhibited in this frequency range, so the time constants obtained with the three models were reasonable. Also, trap densities of $10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ are not surprising considering the high concentration of defects in nitride materials.[15]

These studies suggest that trap states could be a significant contributing factor to the power compression typically observed in AlGaN/GaN HFETs. The decrease in modulation of channel charge as frequency is increased, which could arise from the presence of interface or bulk traps, is consistent with reduced power output at high frequencies. An additional mechanism that has been proposed[7] as a major contributing factor in nitride HFET power compression is the behavior of the AlGaN barrier layer as a lossy dielectric, giving rise to the frequency dispersion observed in transistor $I-V$ characteristics. However, a calculation of the dielectric relaxation time $\tau=\rho\epsilon$ for depleted AlGaN yields a value of $\sim$1 ns. This value is too small to account for the dispersion observed in our measurements, for which time constants of $\sim$1 μs were derived.

The dispersion observed in our studies of an $Al_{0.15}Ga_{0.85}N$/GaN HFET structure occurs over a higher range of frequencies than that reported for studies of $Al_xGa_{1-x}N$/GaN HFET structures with higher Al content such as Ref. 7 ($x_{Al}\approx 30\%$) and Ref. 16 ($x_{Al}=100\%$). This could also be consistent with dispersion arising from trapping associated with deep levels in the AlGaN layer or near the AlGaN/GaN interface. A number of studies have suggested that certain deep levels in semiconductor alloys can remain at a fixed energy relative to the vacuum level, and that the trap activation energy can therefore change as the band-gap and band-edge energies vary with alloy composition.[17,18] On this basis, it might be expected that the trap activation energies and therefore trap time constants would increase with increasing Al concentration, leading to the observation of conductance and capacitance dispersion at lower frequencies in $Al_xGa_{1-x}N$/GaN HFETs with higher Al concentration.

IV. SUMMARY

In summary, extensive electrical characterization of the gate-drain diode of an AlGaN/GaN HFET structure has been performed by measuring the capacitance and conductance as a function of frequency for gate voltages near the threshold voltage. Detailed and systematic analysis of these measurements allows information about trap states to be extracted. Various models were employed to account for the presence of traps located at the heterojunction, in the bulk of the barrier layer, and at the metal–semiconductor interface. A trap density of approximately $10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ and a time constant on the order of 1 μs were obtained with all three models, but the location of the traps could not be determined unambiguously. These results are consistent with other studies of the frequency dispersion of electrical characteristics in AlGaN/GaN HFETs and shed light on what is likely to be a significant factor contributing to rf power compression in these devices.

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