ACS APPLIED MATERIALS & INTERFACES

Research Article

Cite This: ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

www.acsami.org

Large Reduction of Hot Spot Temperature in Graphene Electronic Devices with Heat-Spreading Hexagonal Boron Nitride

David Choi,[†] Nirakar Poudel,[‡] Saungeun Park,[§] Deji Akinwande,[§,∥] Stephen B. Cronin,[‡] Kenji Watanabe,[⊥] Takashi Taniguchi,[⊥] Zhen Yao,[#] and Li Shi*[,†,∥]

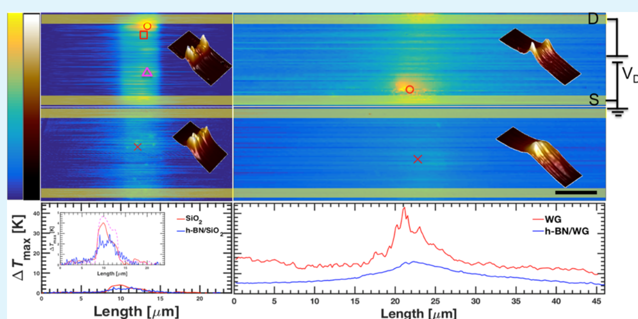
[†]Department of Mechanical Engineering, [§]Microelectronics Research Center, Department of Electrical and Computer Engineering, [∥]Texas Materials Institute, and [#]Department of Physics, The University of Texas at Austin, Austin, Texas 78712, United States

[‡]Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089, United States

[⊥]National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan

Supporting Information

ABSTRACT: Scanning thermal microscopy measurements reveal a significant thermal benefit of including a high thermal conductivity hexagonal boron nitride (h-BN) heat-spreading layer between graphene and either a SiO_2/Si substrate or a 100 μm thick Corning flexible Willow glass (WG) substrate. At the same power density, an 80 nm thick h-BN layer on the silicon substrate can yield a factor of 2.2 reduction of the hot spot temperature, whereas a 35 nm thick h-BN layer on the WG substrate is sufficient to obtain a factor of 4.1 reduction. The larger effect of the h-BN heat spreader on WG than on SiO_2/Si is attributed to a smaller effective heat transfer coefficient per unit area for three-dimensional heat conduction into the thick, low-thermal conductivity WG substrate than for one-dimensional heat conduction through the thin oxide layer on silicon. Consequently, the h-BN lateral heat-spreading length is much larger on WG than on SiO_2/Si, resulting in a larger degree of temperature reduction.



KEYWORDS: *graphene, hexagonal boron nitride, two-dimensional materials, thermal management, scanning thermal microscopy*

1. INTRODUCTION

The high intrinsic electron mobility,[1−3] thermal conductivity,[4−6] and mechanical strength of graphene have motivated the exploration of not only this zero-band gap two-dimensional (2D) material but also other 2D semiconducting materials for next-generation electronic devices.[7−12] These atomically thin 2D materials are as optically transparent and flexible as many plastics, which can potentially allow for the realization of transformative, flexible electronic technologies.[12] However, as the size of electronic components continues to shrink, the increased power densities result in localized hot spots that compromise the reliability and performance of the device. While thermal dissipation has already become a bottleneck in devices fabricated on high-thermal conductivity silicon substrates, the low thermal conductivity and low glass-transition temperatures of most polymer or glass substrates mandate even stricter thermal management requirements on flexible platforms.[13,14] Furthermore, because of the large exposed surface area of 2D materials, both their electron mobility and thermal conductivity can be drastically reduced when they are supported on an amorphous SiO_2 or polymeric substrate.[15−17]

The reduced mobility, in turn, leads to an increased power density at the same current, which cannot be dissipated effectively because of the reduced thermal conductivity. These issues have been found to result in high hot spot temperatures on graphene devices fabricated on both rigid and flexible substrates.[18,19]

Because of its atomic flatness, high-energy surface optical phonons, chemical inertness, and absence of dangling bonds, hexagonal boron nitride (h-BN) has recently been identified as a superior dielectric support for graphene and other 2D electronic materials. When h-BN was used as a support for graphene as compared to SiO_2, the electron mobility of the graphene layer was seen to increase by nearly an order of magnitude[20] because of the reduction of electron−hole puddles and inhomogeneity in the charge carrier concentration.[15,21] Besides enhancing the electron mobility of graphene, h-BN possesses a room-temperature in-plane thermal conductivity as high as 390 W m^{-1} K^{-1},[22] which is more than 2 orders of magnitude larger than most common dielectrics including SiO_2. However, the cross-plane thermal conductivity of h-BN is only about 2 W m^{-1} K^{-1}.[23] Therefore, the thermal benefit of an h-BN support for 2D electronic devices has remained elusive.

Received: November 1, 2017
Accepted: March 12, 2018
Published: March 12, 2018

Downloaded via UNIV OF TEXAS AT AUSTIN on May 23, 2020 at 21:08:28 (UTC).
See https://pubs.acs.org/sharingguidelines for options on how to legitimately share published articles.

ACS Publications © 2018 American Chemical Society

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

In this paper, we report high-spatial resolution, quantitative scanning thermal microscopy (SThM) measurements of the effect of an h-BN heat spreader for lowering the hot spot temperature of 2D electronic devices. The representative 2D devices used in this study are graphene channels fabricated on a silicon substrate and on a flexible Corning Willow glass (WG) substrate. Similar to silicon electronic devices where the local power density can be much higher than the average value for an entire chip, which is on the order of 100 W cm^{-2},[24] the local power density at the individual micron-scale graphene device is as high as 16 000 W cm^{-2} during the experiments. The measurement and analysis results show that for equivalent power densities, an h-BN layer can yield a reduction of the local hot spot temperature by as much as a factor of about 2.2 and 4.1 for the devices fabricated on the silicon substrate and on the glass substrate, respectively, mainly because of the heat-spreading capability of the h-BN layer. This observed reduction is more than 1 order of magnitude higher than an earlier measurement that showed lower average temperatures of a large heater when it was covered by an h-BN/graphene composite heat-spreading layer.[25] The results shown here clearly demonstrate that an h-BN heat spreader can significantly reduce the temperature of micron and submicron scale hot spots.

2. EXPERIMENTAL METHODS

SThM was employed in this work to study the effect of h-BN as a lateral heat-spreading layer between graphene and a 300 nm SiO_2/Si substrate as well as between graphene and a flexible Corning WG substrate, as shown in Figure 1a,b, respectively. The h-BN flakes were exfoliated from high-purity h-BN powders, which were synthesized under high-temperature and high-pressure conditions using barium boron nitride as a solvent.[26] The graphene sample was grown with low-pressure chemical vapor deposition on an acetic acid pretreated copper foil at 1035 °C for 10 min with flow rates of 5 SCCM for CH_4 and 5 SCCM for H_2. The pressure during the growth was held constant at 100 mTorr. A poly(methyl methacrylate) (PMMA)-assisted wet-transfer technique was used to transfer the graphene to the target substrate, where the final rectangular graphene strip was patterned by electron-beam lithography (EBL) and etched by an O_2 plasma. Electrodes were defined by a second EBL step and deposited by evaporation of 5 nm Cr and 50 nm Pd. After liftoff in acetone, the final device was annealed at 350 °C in air for 10 min in an attempt to burn off residual PMMA. The Joule-heated graphene channels under study measured 5 μm across and 10 μm long. For the h-BN/SiO_2/Si sample shown in Figure 1a, Joule heating was applied to the graphene section between the fourth and fifth electrodes from the top only, such that the underlying h-BN was of uniform thickness. Thermal scans performed perpendicular to the electrodes showed similar temperature profiles above the fourth electrode and below the fifth electrode, which can be attributed to a greater amount of heat flowing into the Pd electrode heat sinks rather than beyond them into other sections of the h-BN with variable thickness.

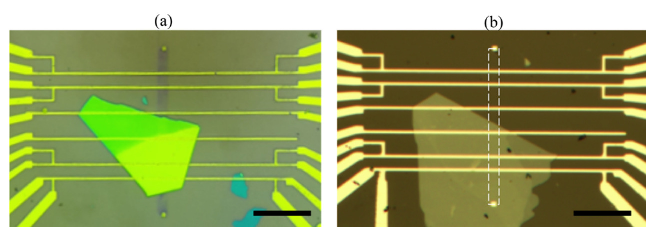


Figure 1. Optical images of the measured devices on the SiO_2/Si substrate (a) and the Corning WG substrate (b). The white dashed line in (b) shows the location of the full graphene strip. The scale bars are 25 μm.

Thermal maps of the graphene channels were obtained using an SThM probe (TSP Nanoscopy) with a Cr/Au thermocouple junction fabricated on the SiO_2 tip of a SiO_2 cantilever. Under ambient measurement conditions, the local thermal signal due to heat transfer through the tip-sample solid−solid contact and the surrounding liquid meniscus is masked by a nonlocal signal from conduction through the air. Similar to several recent experiments,[27−29] a triple-scan procedure was used in this work to eliminate the nonlocal signal measured in the lift mode from the signal obtained in the contact mode, so that the corrected signal is due to local heat transfer through the sub-100 nm tip-sample contact. In this method, the thermovoltage of the tip is recorded three times for each scan line, once while the tip is in direct contact with the sample and again with the tip lifted to 300 and 100 nm above it. Because the temperature rise in the tip due to conduction through the air increases approximately linearly with decreasing lift height,[29] the two lift profiles can be extrapolated to obtain the thermal signal at a theoretical lift height of 0 nm where the tip is lifted just enough to be out of contact from the sample. At this position, the thermocouple junction reading would contain only the contribution through the air. The local temperature rise at the tip can then be found according to a prior study as[28]

$$\Delta T_S = \Delta T_C + \varphi(\Delta T_C - \Delta T_L) \quad (1)$$

where ΔT_C and ΔT_L are the thermocouple junction temperature rise when the tip is in contact with the sample and with the tip lifted just enough to be out of contact, respectively, ΔT_S is the sample temperature rise, and the parameter φ depends on the thermal resistance for local heat transfer across the tip-sample solid−solid contact and the surrounding liquid meniscus.

The φ parameter was obtained from a calibration experiment for the same SThM tip used in the thermal imaging. A 1 μm wide, 100 μm long Pd line similar to the second line in Figure 1a was used as a resistance thermometer to calibrate the SThM probe. During this calibration, the measured four-probe current−voltage ($I-V$) curve of the Pd line was used to calculate its electrical resistance increase due to Joule heating. The resistance increase is converted to the temperature rise with the use of the separately measured temperature coefficient of resistance of the Pd line. Because of the high aspect ratio of the heated line on the thinly oxidized Si, the sample temperature rise (ΔT_S) at the center of the Pd line is closely approximated by the average temperature of the line.[30] The thermovoltages of the tip immediately before and after contact with the center of the line were then recorded and converted to the corresponding temperature rises ΔT_L and ΔT_C using the specified 20.5 μV K^{-1} thermopower of the thermocouple tip. Equation 1 was then used to obtain φ = 40.6 ± 8.3 based on the measured ΔT_S, ΔT_L, and ΔT_C. Finally, the variation in φ due to variable sample surfaces was found to be within the calculated uncertainty and can be attributed to similar surface conditions caused by polymer residue left from the lithography process on the sample surface.[29] The variation between surfaces has been included in the overall uncertainty of φ. The calibration procedures are discussed in detail in the Supporting Information.

3. RESULTS AND DISCUSSION

Figure 2a−c shows the SThM results for graphene channels fabricated on a SiO_2/Si substrate. The images in Figure 2a,b are the thermal maps of graphene supported by SiO_2/Si and by h-BN/SiO_2/Si, respectively, and are plotted on the same 0−7 K scale. Both channels are subjected to a 2000 W cm^{-2} Joule-heat power density. The location of the maximum temperature in each section is indicated by the red "o" and "x". The yellow, horizontal bars indicate the location of the Cr/Pd electrodes and the insets show three-dimensional (3D) representations of each map. The temperature of a second spot several microns away from the contact and indicated by the red square in Figure 2a was chosen as the characteristic hot spot temperature for

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

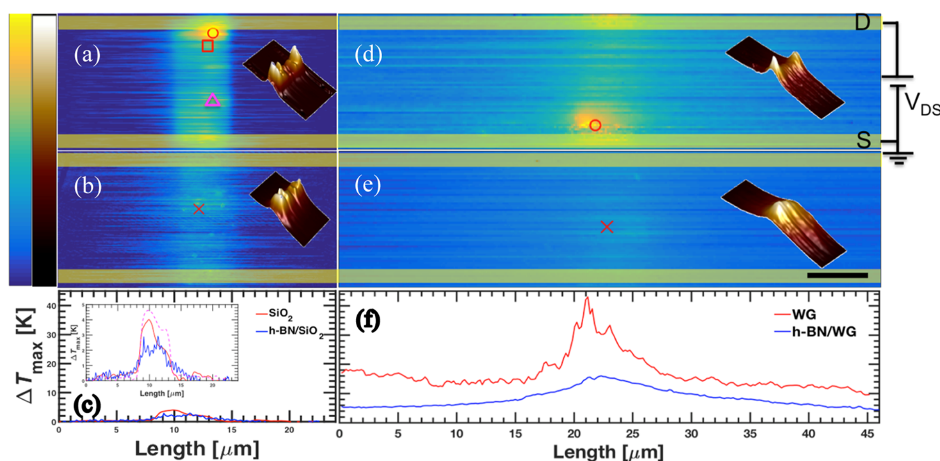


Figure 2. Thermal images of graphene supported on SiO_2/Si (a), h-BN/SiO_2/Si (b), WG (d), and h-BN/WG (e) substrates. The insets in the thermal images are 3D temperature contours of the graphene channels. Each graphene channel was subjected to 2000 W cm^{-2} of Joule heating except for (d), where the power density is 1600 W cm^{-2}. The open circles "o" and "x" mark the locations of the hottest temperature in each image. The horizontal scan lines through each hot spot in (b,d,e) are shown by the solid lines in figures (c,f). An expanded view of the main figure in (c) is shown in the inset for clarity. The open square in (a) is a different hot spot removed from the contact, whose horizontal scan line is plotted in the inset of (c) as the solid red line alongside a third scan line (dashed pink line) whose location toward the center of the channel is indicated by the pink triangle. The scale bar is 5 μm. The blue to yellow color bars range from 0 to 7 K for figures (a,b) and from 0 to 45 K for figures (d,e). The black to white color bars for the 3D insets range from 0 to 3 K, 0 to 7 K, 5 to 20 K, and 10 to 45 K for (a), (b), (d), and (e), respectively.

that device to avoid any possible effect of contact heating. Although it is difficult to see this hot spot at the 2 kW/cm^2 power density, this spot was clearly visible in the SThM image obtained at the 16 kW/cm^2 dissipation density, as shown in Figure S6 of the Supporting Information. Figure 2c shows the thermal line scan through each respective characteristic hot spot indicated in Figure 2a,b. An expanded view is shown in the inset for clarity, where a third scan through the spot indicated by a pink triangle in Figure 2a near the center of the channel has also been shown. Similarly, Figure 2d,e shows the thermal images for graphene on WG under 1600 W cm^{-2} power density and graphene on h-BN/WG under 2000 W cm^{-2}. The temperature rise scale in these figures is 0−45 K. Figure 2f displays the line scans through the hot spots in these two devices. Figure 2c,f is plotted on the same scale to clearly illustrate the difference in thermal magnitude and distribution between the two substrates.

A comparison between the two substrate types reveals fundamental differences in both the magnitude of the temperature rise and the heat distribution. Figure 2c,f shows that the maximum temperature rise of graphene on the thick, flexible WG substrate is an order of magnitude larger than that on the silicon substrate. For power densities of 1600 and 2000 W cm^{-2}, the maximum temperature rise of graphene on WG is 43.0 ± 6.1 K and the temperature rise at the characteristic hot spot on SiO_2/Si is 4.0 ± 1.4 K. Similarly, the maximum temperature rises for graphene/h-BN/WG and graphene/h-BN/SiO_2/Si at 2000 W cm^{-2} are 16.0 ± 1.8 and 2.9 ± 0.3 K, respectively. The much lower temperatures on silicon are attributed to the high thermal conductivity of the silicon substrate and relatively small thickness of the oxide layer compared to the channel width.[31] Consequently, heat is dissipated almost vertically through the SiO_2 and into the Si heat sink, as shown in Figure 2a−c, where the temperature quickly drops to ambient within a couple microns laterally from the graphene edge. In contrast, Figure 2d,e shows elevated temperatures extending beyond 20 μm from the graphene edge on WG. Vertical heat transfer is therefore no longer dominant in the 100 μm thick WG, leading to a greater degree of lateral heat spreading and much hotter temperatures.

Because breakdown of graphene on WG was observed beyond the relatively low power density of 1600 W cm^{-2}, a direct comparison at an equal 2000 W cm^{-2} density for all devices was prohibitive. Moreover, the small temperature rise of graphene on h-BN/SiO_2/Si when dissipating less than 2000 W cm^{-2} was difficult to measure accurately. The study was therefore extended over multiple power densities. Figure 3 shows that the hot spot temperatures increase linearly with the increasing power density and reveals that inclusion of an h-BN layer reduces the hottest spot temperature by a factor of about 2.2 and 4.1 for the devices fabricated on the silicon and WG substrates, respectively.

It is necessary to discuss whether the observed reduction by the h-BN layer can be caused by the elimination of localized Joule heating, the heat-spreading capability of the h-BN layer, or a combination of both factors. It is reported that an h-BN support can suppress electron−hole puddles[13,20] and change the Dirac point and carrier type in the graphene channel.[32] The four-probe resistance of the h-BN-supported graphene channel on SiO_2 was 3320 Ω compared to the 970 Ω resistance of the graphene on bare SiO_2. Similarly, the four-probe resistance of the h-BN-supported graphene channel on WG was 4250 Ω compared to the 1150 Ω resistance of the graphene on bare WG. The resistance increase with the h-BN layer is indicative of reduced electron−hole puddles and carrier concentration, as well as a shifting of the Dirac point toward 0 V. However, it is unclear whether electron−hole puddle suppression can potentially lead to increased uniformity of the Joule heat generation and thus reduced localized Joule heating.

The concentrated hot spots observed in the devices without the h-BN can, in principle, be caused by localized Joule heating because of contact heating, nonuniform charge carrier density, or nonuniform defect concentration along the graphene channel,[29,30,33−35] as well as Peltier cooling and heating at the contacts. On the basis of the measured two-probe and four-probe resistances of the graphene channel and the two-probe

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

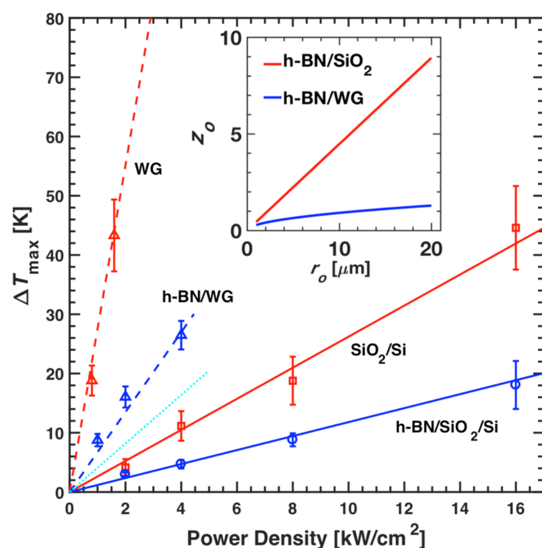


Figure 3. Maximum hot spot temperatures as a function power density. The light blue dotted line indicates the analytical solution of a graphene device on h-BN/WG with the same 80 nm h-BN thickness as for the h-BN/SiO_2 case, while the h-BN thickness used to calculate the dark blue dashed line is the 35 nm of the actual sample. Values of 2.8, 4.0, 4.0, and 5.3 μm for r_o, the characteristic hot spot radius, were used to fit the data for SiO_2/Si, h-BN/SiO_2/Si, WG, and h-BN/WG, respectively and are comparable in magnitude to the experimental r_o values of 2.43, 3.69, 3.75, and 7.8 μm, respectively. The inset shows the dimensionless parameter z_o as a function of r_o.

resistance of the electrical leads to the contacts, the contact resistance for the graphene/SiO_2 device of Figure 2a is only about 60 Ω, which is much smaller than the four-probe resistance of 970 Ω for the graphene channel and typical for such devices. Thus, the small contact resistance is not expected to be sufficient to generate the hottest spot near the drain contact for this device. However, to eliminate any ambiguity of the origin of the hot spot, only the temperature of the spot several microns away from the contact and indicated by the red square in Figure 2a is reported in Figure 3. For the graphene/WG device shown in Figure 2d, the hottest spot centers at a distance of about 2 μm away from the actual contact, suggesting that the hot spot cannot be attributed to contact heating either in this device.

In addition, the electron concentration of an n-type graphene channel is higher near the grounded source contact than near the drain contact where a positive drain-source voltage is applied, so that the resistivity and local Joule heating would be higher near the drain than near the source. The situation is reversed for a p-type graphene channel. Gate field-dependent current−voltage (I−V) measurements of the graphene channel on h-BN/SiO_2/Si showed that the channel is p-type (Supporting Information). Despite being p-type, Figure 2b does not reveal the presence of a hot spot near the source electrode where the hole concentration is expected to be the lowest in this device. However, current leakage between a bonding pad and the silicon back gate through the 300 nm SiO_2 layer of the device without h-BN occurred after several ramping cycles of the gate voltage. The gate leakage was caused mainly by the damage of the thin oxide layer by a combination of a large mechanical force of the wire bonding tool and the large gate field. The leakage prevented determination of the majority carrier type of the graphene/SiO_2 channel (Supporting Information). Hence, it is unclear whether the hottest spot found near the drain electrode for this device is caused by nonuniform carrier concentration, nonuniform defect concentration, or Peltier effect.

In spite of this uncertainty, it is apparent from the two thermal images in Figure 2a,b that most areas of the graphene channel without the h-BN layer are considerably hotter than the hottest point of the graphene channel with the h-BN layer at the same average power density. The dashed line in the inset of Figure 2c shows that the temperatures even at locations far away from the concentrated hottest spot in the graphene/SiO_2 device are in general higher than the hottest point in the h-BN channel. This comparison clearly suggests that the temperature reduction is mainly caused by the heat-spreading effect of the h-BN layer instead of the presence of localized Joule dissipation only in the device without the h-BN layer but not in the device with the h-BN layer. A similar comparison can be made between the two devices on the WG substrate with and without the h-BN layer to reveal the heat-spreading effect of the h-BN layer.

To better understand the main cause for the hot spot temperature reduction, an analytical model is established to gain physical insight into the heat-spreading capability of the h-BN layer on the two different substrates. The cross-plane thermal conductivity of h-BN is in the range of 1.5 to 2.5 W m^{-1} K^{-1} at room temperature. Thus, the cross plane thermal conductance of the h-BN layer is approximately 5×10^7 W m^{-2} K^{-1}, which is close to the interface thermal conductance between h-BN and graphene in a recent work.[23,36] In comparison, the cross-plane thermal conductance through the 300 nm SiO_2 is about 4×10^6 W m^{-2} K^{-1}, which is already much larger than the spreading thermal conductance of the 100 μm thick WG. Therefore, the temperature drop across the thickness of the graphene/h-BN stack is expected to be small compared to the temperature drops across the SiO_2 layer and the WG substrate. Consequently, both the graphene and the graphene/h-BN stack are assumed to act as a heat transfer fin with a uniform temperature across the thickness, such that the governing equation is

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{dT}{dr}\right) - \frac{h}{\kappa_g t_g + \kappa_{\text{h-BN}} t_{\text{h-BN}}}(T - T_o) + \frac{\dot{q}''' t_g}{\kappa_g t_g + \kappa_{\text{h-BN}} t_{\text{h-BN}}} = 0 \tag{2}$$

where T_o is the ambient temperature, h is the effective heat transfer coefficient between the ambient and the sample, t_g and κ_g are the thickness and in-plane thermal conductivity of the monolayer graphene, respectively, $t_{\text{h-BN}}$ and $\kappa_{\text{h-BN}}$ are the thickness and in-plane thermal conductivity of the h-BN layer, respectively, and $\dot{q}'''$ is the volumetric Joule heating in the graphene. The volumetric heating is assumed to take a Gaussian shape such that

$$\dot{q}''' \equiv A\cdot\exp\left(-\frac{r^2}{r_o^2}\right) \tag{3}$$

where r_o is the Gaussian radius of the hot spot and is used as a fitting parameter. The coefficient A is calculated such that the total amount of heat generated within the hot spot is equal to the experimentally applied power. Assuming a vanishing

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

gradient at the center of the hot spot and $\lim_{r\to\infty} T(r) = T_o$, the solution for the maximum temperature rise in eq 2 has been derived as[4,37]

$$\Delta T_{max} = -\lim_{z\to\infty}\left(\frac{\Delta T_p(z)}{I_0(z)}\right) \quad (4)$$

where

$$\Delta T_p(z) = I_0(z)\int_0^z \frac{K_0(z)\frac{A\cdot t_{gr}}{h}\exp\left(-\frac{z^2}{z_o^2}\right)}{-I_0(z)K_1(z) - K_0(z)I_1(z)}dz - K_0(z)\int_0^z \frac{I_0(z)\frac{A\cdot t_{gr}}{h}\exp\left(-\frac{z^2}{z_o^2}\right)}{-I_0(z)K_1(z) - K_0(z)I_1(z)}dz \quad (5)$$

$z \equiv r/L_s$, $L_s \equiv \left(\frac{\kappa_g t_g + \kappa_{h\text{-BN}} t_{h\text{-BN}}}{h}\right)^{0.5}$ is defined as the heat-spreading length, I_0 and I_1 are the zeroth- and first-order modified Bessel function of the first kind, respectively, and K_0 and K_1 are the zeroth- and first-order modified Bessel functions of the second kind, respectively.

The surface heat transfer coefficient, h, consists of a series combination of heat diffusion into the substrate and the interfacial thermal conductance between the sample and the substrate. Heat diffusion into the substrate is calculated differently for each case and is reflective of the physical structure of the underlying support. With respect to the silicon substrate, vertical heat dissipation through the oxide is assumed based on the thermal scans shown in Figure 2a–c. The surface heat transfer coefficient per unit area is therefore calculated as

$$h_{SiO_2} = \left[\frac{t_{ox}}{\kappa_{ox}} + \frac{1}{G}\right]^{-1} \quad (6)$$

where t_{ox} is the SiO_2 thickness, κ_{ox} is the SiO_2 thermal conductivity, and G is the interface thermal conductance at the interface with SiO_2 per unit area. In contrast to the thin oxide layer, the isotropic, 100 μm thick WG substrate is much thicker than the width of the graphene channel. Therefore, the first term in eq 6 is replaced with a 3D thermal spreading resistance term for a circular hot spot above a semi-infinite medium, $R_{sp} = \frac{1}{4\kappa_{WG} r_o}$,[38] which is normalized by the area of the hot spot to yield

$$h_{WG} = \left[\frac{\pi r_o}{4\kappa_{WG}} + \frac{1}{G}\right]^{-1} \quad (7)$$

where κ_{WG} is the WG thermal conductivity. In these models, a typical value of $G = 5 \times 10^7$ W m^{-2} K^{-1} reported in the literature was assumed.[39,40] Values for r_o of 2.8, 4.0, 4.0, and 5.3 μm were used to fit the data for SiO_2/Si, h-BN/SiO_2/Si, WG, and h-BN/WG, respectively, and are comparable in magnitude to the experimental r_o values of 2.43, 3.69, 3.75, and 7.8 μm, respectively. The corresponding calculated values of ΔT_{max} are plotted in Figure 3 as dashed and solid lines and are in good agreement with the experimental data. Equivalent to the effective hot spot thermal resistances per unit area, the slopes of these lines are 2.76×10^{-6}, 0.67×10^{-6}, 0.26×10^{-6}, and 0.12×10^{-6} m^2 K W^{-1} for WG, h-BN/WG, SiO_2/Si, and h-BN/SiO_2/Si, respectively.

According to these calculation results, the heat-spreading capability of the h-BN layer alone is able to yield a reduction in the hot spot temperature by a factor of 4.1 and 2.2 on the WG and SiO_2/Si substrates, respectively. Hence, the observed hot spot temperature reduction can be mainly attributed to the heat-spreading effect of the h-BN layer, instead of the suppression of the localized Joule heating by the h-BN layer.

In addition, it is necessary to note that the experimental h-BN thickness on WG was 35 nm compared to 80 nm on SiO_2/Si. An additional analytical model for an 80 nm h-BN layer on WG is therefore included in Figure 3 as the dotted light-blue line. The thermal resistance per unit area for this curve is 0.39×10^{-6} m^2 K W^{-1}, which predicts hot spot temperature reduction by a factor of 7.1 as compared to bare WG. The larger benefit of h-BN on WG compared to SiO_2/Si can be understood from the effect of the substrate-dependent heat transfer coefficient on the heat-spreading lengths. The generated heat needs to be conducted through the substrate to the heat sink.[37,41] As a result, it had been suggested that increasing the interface conductance, G, should be a key focus in improving thermal performance. However, for devices fabricated on a flexible substrate or a silicon substrate with an oxide layer thicker than ~100 nm where the substrate conductance is much smaller than the interface conductance, increasing G has a negligible effect on reducing hot spot temperatures.[37] In the experiments performed here, the first terms in eqs 6 and 7, which represent the substrate through-thickness thermal resistances, are both more than 1 order of magnitude greater than the second term, $1/G$, which is associated with thermal resistance of the interface. As a result, the analytical results found that even varying G to be as low as 1×10^7 W m^{-2} K^{-1} or as high as 10×10^7 W m^{-2} K^{-1} did not significantly affect the overall findings. Through-thickness dissipation is therefore dominated by the diffusive resistance of the substrate instead of the interface resistance.

Increasing the lateral footprint of the hot spot, however, can have a significant impact by enabling through-thickness dissipation over a larger area. In particular, increasing the heat-spreading length relative to the hot spot size such that $z_o = r_o/L_s$ is less than about 10 is an effective method to reduce hot spot temperatures.[37] This approach remains effective as long as the heat-spreading length is not much larger than the distance between adjacent hot spots such that thermal cross talk is prevented. The inset of Figure 3 plots z_o as a function of the hot spot size for both substrates. This figure shows that inclusion of an assumed 50 nm h-BN heat-spreading layer can reduce the hot spot temperature effectively when the hot spot size on SiO_2/Si is less than 10 μm. Because of a lower h value for 3D heat conduction through the WG layer compared to vertical heat conduction through the thin SiO_2 layer on the Si substrate, the z_o value is much lower for WG than for SiO_2/Si. Consequently, the z_o value for the h-BN/WG case is still below 1 when the hot spot size is as large as 20 μm, such that the h-BN heat spreader is still expected to be effective if the separation between hot spots is larger than this length. The relatively large benefit of h-BN heat spreading on WG for larger hot spots follows naturally from eqs 6 and 7, where it can be seen that the heat transfer coefficient per unit area (h) decreases even further with the increasing hot spot size on the WG substrate but not on the silicon substrate. As a result, the

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101–11107

heat-spreading length scales with the hot spot size on the WG substrate but not on the SiO_2/Si substrate.

4. CONCLUSIONS

The experimental and analytical results show that for equivalent power densities, inclusion of an h-BN layer between a graphene channel and its underlying substrate can result in a large drop in localized hot spot temperatures. Besides increasing the electron mobility, reducing electron−hole puddles, and shifting the Dirac point, an h-BN dielectric layer below graphene serves as a highly effective lateral heat spreader and leads to a reduction of hot spot temperatures. The effective heat transfer coefficient per unit area is lower for 3D heat conduction through a low-thermal conductivity glass substrate than for one-dimensional vertical heat conduction through SiO_2 and decreases with the hot spot size for the WG substrate but not for the SiO_2/Si substrate. As a result, the effect of the h-BN heat spreader is more pronounced for devices fabricated on a flexible glass substrate than on a SiO_2/silicon substrate because of a much larger heat-spreading length. While localized heating inside individual 2D devices has been observed because of the presence of local defects or inhomogeneity in the charge carrier concentration, h-BN dielectric supports can reduce peak device temperatures by spreading hot spots laterally over the area between them.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b16634.

SThM calibration and triple scan technique (PDF)

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: lishi@mail.utexas.edu.

ORCID

David Choi: 0000-0002-2666-4003
Stephen B. Cronin: 0000-0001-7089-6672
Kenji Watanabe: 0000-0003-3701-8119
Li Shi: 0000-0002-5401-6839

Author Contributions

D.C. carried out the device fabrication, measurements, and analysis. N.P., S.P., S.B.C., and D.A. contributed to device fabrication. K.W. and T.T. synthesized the h-BN source materials. Z.Y. assisted in the scanning probe measurement. L.S. designed the experiment and contributed to the thermal measurements and data analysis. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Funding

The experiments with on devices on silicon substrates were supported by Department of Energy Basic Energy Science Office award numbers DE-FG02-07ER46376 (N.P. and S.C.) and DE-FG02-07ER46377 (D.C. and L.S.). The experiments with devices on the flexible substrate were supported by the National Science Foundation award number EEC-1160494 (D.C., S.P., D.A., and L.S.). Growth of hexagonal boron nitride crystals was supported by the Elemental Strategy Initiative conducted by the MEXT, Japan, and JSPS KAKENHI grant number JP15K21722 (K.W. and T.T.).

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The lead extends his deepest gratitude to Dr. Mir Mohammad Sadeghi for the insightful discussions and advice he has provided.

■ REFERENCES

(1) Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh Electron Mobility in Suspended Graphene. *Solid State Commun.* **2008**, *146*, 351−355.

(2) Morozov, S. V.; Novoselov, K. S.; Katsnelson, M. I.; Schedin, F.; Elias, D. C.; Jaszczak, J. A.; Geim, A. K. Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer. *Phys. Rev. Lett.* **2008**, *100*, 16602.

(3) Wang, J.; Ma, F.; Liang, W.; Sun, M. Electrical Properties and Applications of Graphene, Hexagonal Boron Nitride (H-BN), and Graphene/h-BN Heterostructures. *Mater. Today Phys.* **2017**, *2*, 6−34.

(4) Cai, W.; Moore, A. L.; Zhu, Y.; Li, X.; Chen, S.; Shi, L.; Ruoff, R. S. Thermal Transport in Suspended and Supported Monolayer Graphene Grown by Chemical Vapor Deposition. *Nano Lett.* **2010**, *10*, 1645−1651.

(5) Seol, J. H.; Jo, I.; Moore, A.; Lindsay, L.; Aitken, Z. H.; Pettes, M. T.; Li, X.; Yao, Z.; Huang, R.; Broido, D.; Mingo, N.; Ruoff, R. S.; Shi, L. Two-Dimensional Phonon Transport in Supported Graphene. *Science* **2010**, *328*, 213−216.

(6) Chen, S.; Moore, A. L.; Cai, W.; Suk, J. W.; An, J. H.; Mishra, C.; Amos, C.; Magnuson, C. W.; Kang, J.; Shi, L.; Ruoff, R. S. Raman Measurements of Thermal Transport in Suspended Monolayer Graphene of Variable Sizes in Vacuum and Gaseous Environments. *ACS Nano* **2011**, *5*, 321−328.

(7) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666−669.

(8) Novoselov, K. S.; Fal'ko, V. I.; Colombo, L.; Gellert, P. R.; Schwab, M. G.; Kim, K. A Roadmap for Graphene. *Nature* **2012**, *490*, 192−200.

(9) Butler, S. Z.; Hollen, S. M.; Cao, L.; Cui, Y.; Gupta, J. A.; Gutiérrez, H. R.; Heinz, T. F.; Hong, S. S.; Huang, J.; Ismach, A. F.; Johnston-Halperin, E.; Kuno, M.; Plashnitsa, V. V.; Robinson, R. D.; Ruoff, R. S.; Salahuddin, S.; Shan, J.; Shi, L.; Spencer, M. G.; Terrones, M.; Windl, W.; Goldberger, J. E. Progress, Challenges, and Opportunities in Two-Dimensional Materials beyond Graphene. *ACS Nano* **2013**, *7*, 2898−2926.

(10) Sun, D.-M.; Liu, C.; Ren, W.-C.; Cheng, H.-M. A Review of Carbon Nanotube- and Graphene-Based Flexible Thin-Film Transistors. *Small* **2013**, *9*, 1188−1205.

(11) Akinwande, D.; Petrone, N.; Hone, J. Two-Dimensional Flexible Nanoelectronics. *Nat. Commun.* **2014**, *5*, 5678.

(12) Ferrari, A. C.; Bonaccorso, F.; Falko, V.; Novoselov, K. S. Science and Technology Roadmap for Graphene, Related Two-Dimensional Crystals, and Hybrid Systems. *Nanoscale* **2015**, *7*, 4598−4810.

(13) Lee, J.; Ha, T.-J.; Parrish, K. N.; Chowdhury, S. F.; Tao, L.; Dodabalapur, A.; Akinwande, D. High-Performance Current Saturating Graphene Field-Effect Transistor with Hexagonal Boron Nitride Dielectric on Flexible Polymeric Substrates. *IEEE Electron Device Lett.* **2013**, *34*, 172−174.

(14) Cahill, D. G.; Braun, P. V.; Chen, G.; Clarke, D. R.; Fan, S.; Goodson, K. E.; Keblinski, P.; King, W. P.; Mahan, G. D.; Majumdar, A.; Maris, H. J.; Phillpot, S. R.; Pop, E.; Shi, L. Nanoscale Thermal Transport. II. 2003-2012. *Appl. Phys. Rev.* **2014**, *1*, 011305.

(15) Fratini, S.; Guinea, F. Substrate-Limited Electron Dynamics in Graphene. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2008**, *77*, 195415.

(16) Chen, J.-H.; Jang, C.; Xiao, S.; Ishigami, M.; Fuhrer, M. S. Intrinsic and Extrinsic Performance Limits of Graphene Devices on SiO2. *Nat. Nanotechnol.* **2008**, *3*, 206−209.

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107

(17) Katsnelson, M. I.; Geim, A. K. Electron Scattering on Microscopic Corrugations in Graphene. *Philos. Trans. R. Soc., A* **2008**, *366*, 195−204.
(18) Bae, M.-H.; Islam, S.; Dorgan, V. E.; Pop, E. Scaling of High-Field Transport and Localized Heating in Graphene. *ACS Nano* **2011**, *5*, 7936−7944.
(19) Lee, J.; Chang, H.-Y.; Ha, T.-J.; Li, H.; Ruoff, R. S.; Dodabalapur, A.; Akinwande, D. High-Performance Flexible Nano-electronics: 2D Atomic Channel Materials for Low-Power Digital and High-Frequency Analog Devices. *International Electron Devices Meeting*, 2013; pp 491−494.
(20) Dean, C. R.; Young, a F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J. Boron Nitride Substrates for High-Quality Graphene Electronics. *Nat. Nanotechnol.* **2010**, *5*, 722−726.
(21) Meric, I.; Han, M. Y.; Young, A. F.; Ozyilmaz, B.; Kim, P.; Shepard, K. L. Current Saturation in Zero-Bandgap, Top-Gated Graphene Field-Effect Transistors. *Nat. Nanotechnol.* **2008**, *3*, 654−659.
(22) Jo, I.; Pettes, M. T.; Kim, J.; Watanabe, K.; Taniguchi, T.; Yao, Z.; Shi, L. Thermal Conductivity and Phonon Transport in Suspended Few-Layer Hexagonal Boron Nitride. *Nano Lett.* **2013**, *13*, 550−554.
(23) Simpson, A.; Stuckes, A. D. The Thermal Conductivity of Highly Oriented Pyrolytic Boron Nitride. *J. Phys. C: Solid State Phys.* **1971**, *4*, 1710−1718.
(24) Pop, E. Energy Dissipation and Transport in Nanoscale Devices. *Nano Res.* **2010**, *3*, 147−169.
(25) Bao, J.; Edwards, M.; Huang, S.; Zhang, Y.; Fu, Y.; Lu, X.; Yuan, Z.; Jeppson, K.; Liu, J. Two-Dimensional Hexagonal Boron Nitride as Lateral Heat Spreader in Electrically Insulating Packaging. *J. Phys. D: Appl. Phys.* **2016**, *49*, 265501.
(26) Taniguchi, T.; Watanabe, K. Synthesis of High-Purity Boron Nitride Single Crystals under High Pressure by Using Ba-BN Solvent. *J. Cryst. Growth* **2007**, *303*, 525−529.
(27) Kim, K.; Chung, J.; Won, J.; Kwon, O.; Lee, J. S.; Park, S. H.; Choi, Y. K. Quantitative Scanning Thermal Microscopy Using Double Scan Technique. *Appl. Phys. Lett.* **2008**, *93*, 203115.
(28) Kim, K.; Chung, J.; Hwang, G.; Kwon, O.; Lee, J. S. Quantitative Measurement with Scanning Thermal Microscope by Preventing the Distortion due to the Heat Transfer through the Air. *ACS Nano* **2011**, *5*, 8700−8709.
(29) Sadeghi, M. M.; Park, S.; Huang, Y.; Akinwande, D.; Yao, Z.; Murthy, J.; Shi, L. Quantitative Scanning Thermal Microscopy of Graphene Devices on Flexible Polyimide Substrates. *J. Appl. Phys.* **2016**, *119*, 235101.
(30) Jo, I.; Hsu, I. K.; Lee, Y. J.; Sadeghi, M. M.; Kim, S.; Cronin, S.; Tutuc, E.; Banerjee, S. K.; Yao, Z.; Shi, L. Low-Frequency Acoustic Phonon Temperature Distribution in Electrically Biased Graphene. *Nano Lett.* **2011**, *11*, 85−90.
(31) Liao, A. D.; Wu, J. Z.; Wang, X.; Tahy, K.; Jena, D.; Dai, H.; Pop, E. Thermally-Limited Current Carrying Ability of Graphene Nanoribbons. *Phys. Rev. Lett.* **2011**, *106*, 256801.
(32) Dean, C.; Young, A. F.; Wang, L.; Meric, I.; Lee, G.-H.; Watanabe, K.; Taniguchi, T.; Shepard, K.; Kim, P.; Hone, J. Graphene Based Heterostructures. *Solid State Commun.* **2012**, *152*, 1275−1282.
(33) Freitag, M.; Chiu, H.-Y.; Steiner, M.; Perebeinos, V.; Avouris, P. Thermal Infrared Emission Reveals the Dirac Point Movement in Biased Graphene. *Nat. Nanotechnol.* **2010**, *5*, 497−501.
(34) Bae, M.-H.; Ong, Z.-Y.; Estrada, D.; Pop, E. Imaging, Simulation, and Electrostatic Control of Power Dissipation in Graphene Devices. *Nano Lett.* **2010**, *10*, 4787−4793.
(35) Grosse, K. L.; Bae, M.-H.; Lian, F.; Pop, E.; King, W. P. Nanoscale Joule Heating, Peltier Cooling and Current Crowding at Graphene-Metal Contacts. *Nat. Nanotechnol.* **2011**, *6*, 287−290.
(36) Liu, Y.; Ong, Z.-Y.; Wu, J.; Zhao, Y.; Watanabe, K.; Taniguchi, T.; Chi, D.; Zhang, G.; Thong, J. T. L.; Qiu, C.-W.; Hippalgaonkar, K. Thermal Conductance of the 2D MoS2/h-BN and Graphene/h-BN Interfaces. *Sci. Rep.* **2017**, *7*, 43886.
(37) Choi, D.; Poudel, N.; Cronin, S. B.; Shi, L. Effects of Basal-Plane Thermal Conductivity and Interface Thermal Conductance on the Hot Spot Temperature in Graphene Electronic Devices. *Appl. Phys. Lett.* **2017**, *110*, 073104.
(38) Bergman, T. L.; Lavine, A. S.; Incropera, F. P.; Dewitt, D. P. *Fundamentals of Heat and Mass Transfer*; John Wiley & Sons, 2011.
(39) Chen, Z.; Jang, W.; Bao, W.; Lau, C. N.; Dames, C. Thermal Contact Resistance between Graphene and Silicon Dioxide. *Appl. Phys. Lett.* **2009**, *95*, 16190.
(40) Mak, K. F.; Lui, C. H.; Heinz, T. F. Measurement of the Thermal Conductance of the Graphene/SiO 2 Interface. *Appl. Phys. Lett.* **2010**, *97*, 221904.
(41) Pop, E. The Role of Electrical and Thermal Contact Resistance for Joule Breakdown of Single-Wall Carbon Nanotubes. *Nanotechnology* **2008**, *19*, 295202.

DOI: 10.1021/acsami.7b16634
ACS Appl. Mater. Interfaces 2018, 10, 11101−11107