REVIEW

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# Graphene and two-dimensional materials for silicon technology

Deji Akinwande[1]*, Cedric Huyghebaert[2], Ching-Hua Wang[3], Martha I. Serna[1], Stijn Goossens[4], Lain-Jong Li[5], H.-S. Philip Wong[3,5] & Frank H. L. Koppens[4,6]

**The development of silicon semiconductor technology has produced breakthroughs in electronics—from the microprocessor in the late 1960s to early 1970s, to automation, computers and smartphones—by downscaling the physical size of devices and wires to the nanometre regime. Now, graphene and related two-dimensional (2D) materials offer prospects of unprecedented advances in device performance at the atomic limit, and a synergistic combination of 2D materials with silicon chips promises a heterogeneous platform to deliver massively enhanced potential based on silicon technology. Integration is achieved via three-dimensional monolithic construction of multifunctional high-rise 2D silicon chips, enabling enhanced performance by exploiting the vertical direction and the functional diversification of the silicon platform for applications in opto-electronics and sensing. Here we review the opportunities, progress and challenges of integrating atomically thin materials with silicon-based nanosystems, and also consider the prospects for computational and non-computational applications.**

Advances in semiconductor technology have manifested in the doubling of the number of components (for example, transistors) per die at a regular interval (for example, every two years), which is loosely called Moore's law. In 2018, the semiconductor industry crossed the 10-nm threshold to offer silicon logic technologies at the 7-nm technology node, with the 5-nm and 3-nm nodes expected in the foreseeable future. (A technology node is a generation of semiconductor manufacturing processes associated with a particular size.) Meanwhile, memory technologies have already changed course and departed from the traditional scaling of geometry. Dynamic random access memory (DRAM) has virtually stopped dimensional downscaling, and has transitioned into the stacking of DRAM chips with logic chips to provide the memory capacity, reduced latency and increased bandwidth required of today's computing systems. Flash memory (in particular, NAND flash), which has become the dominant non-volatile data storage device, has also stopped dimensional downscaling in the 2D plane of the chip. Current and future generations of flash memory are providing increasingly larger storage capacity by building up multiple layers of memory cells in the third dimension, in a way akin to a high-rise building. Flash memories with 64 layers were already in production in 2018, with further opportunities for taller, high-rise memory chips.

## Silicon wonderland

Will future logic technologies continue to provide the energy efficiency required of computing systems? Will emerging applications (for example, in optoelectronics and sensors) and future computation workloads (such as neuromorphic and quantum computing) demand new materials and device concepts compatible with Si CMOS integration? How will technology progression be assessed now that the linear dimensions of devices have ceased to serve as a meaningful metric? In the same sense, how will the added value of integrating 2D materials (2DMs) and new materials be evaluated? These are some of the most pressing questions facing the semiconductor industry today. They are in particular put in a special context by considering the many advantages and diverse functions that are afforded by 2DMs, which can have a massive economic impact in leveraging ubiquitous Si technology (see Fig. 1a).

### Smaller is better

The advances of key metrics such as power–performance–area (and cost reduction) of semiconductor technology in the past five decades have mostly been achieved through dimensional scaling[1]. The principle of device scaling introduced by Dennard provides a guideline to scale down a field-effect transistor (FET) to a small size by proportionally scaling down all physical dimensions simultaneously while scaling up the doping concentration of the transistor channel[2]. By the late 1990s, it was becoming increasingly clear that this constant-field scaling had reached its limits owing to the increasing difficulty in achieving complex doping profiles and the excessive leakage current through the thin silicon dioxide gate insulator[3]. Thus began the 'equivalent scaling' era of the past two decades, which saw the introduction of strained silicon to enhance current drive[4], and high dielectric constant (high-$k$) gate dielectrics and metal gate electrodes[5] as a way to continue the performance and cost benefits expected of Moore's law.

Nevertheless, controlling short-channel effects for sustained dimensional scaling remains a critical challenge. Towards the end of the last millennium, emerging research began to explore a new concept, named the Scale Length Theory[6–8], which relates the transistor's electrostatic integrity to a natural scale length ($\lambda$) that is a function of the gate/channel geometry, thicknesses and dielectric constants. A FET would not suffer from short-channel effects if the gate length maintained a certain aspect ratio to the scale length, even for a channel without doping. The state-of-the-art FinFET transistors (Fig. 1b) guided by this theory have been in volume production since the 22-nm node (about 2012)[9]. For the 10- and 7-nm technology nodes, the gate lengths of FinFETs are about 20 nm, and the fin thickness is about 7–8 nm. Multiple-stacked nanowires and nanosheets with wrap-around gates are being developed to provide even better electrostatic control. As transistor width

[1]Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX, USA. [2]IMEC, Leuven, Belgium. [3]Department of Electrical Engineering, Stanford University, Stanford, CA, USA. [4]ICFO–Institut de Ciencies Fotoniques, The Barcelona Institute of Science and Technology, Castelldefels (Barcelona), Barcelona, Spain. [5]Corporate Research, Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan. [6]ICREA–Institució Catalana de Recerça i Estudis Avancats, Barcelona, Spain. *e-mail: deji@ece.utexas.edu

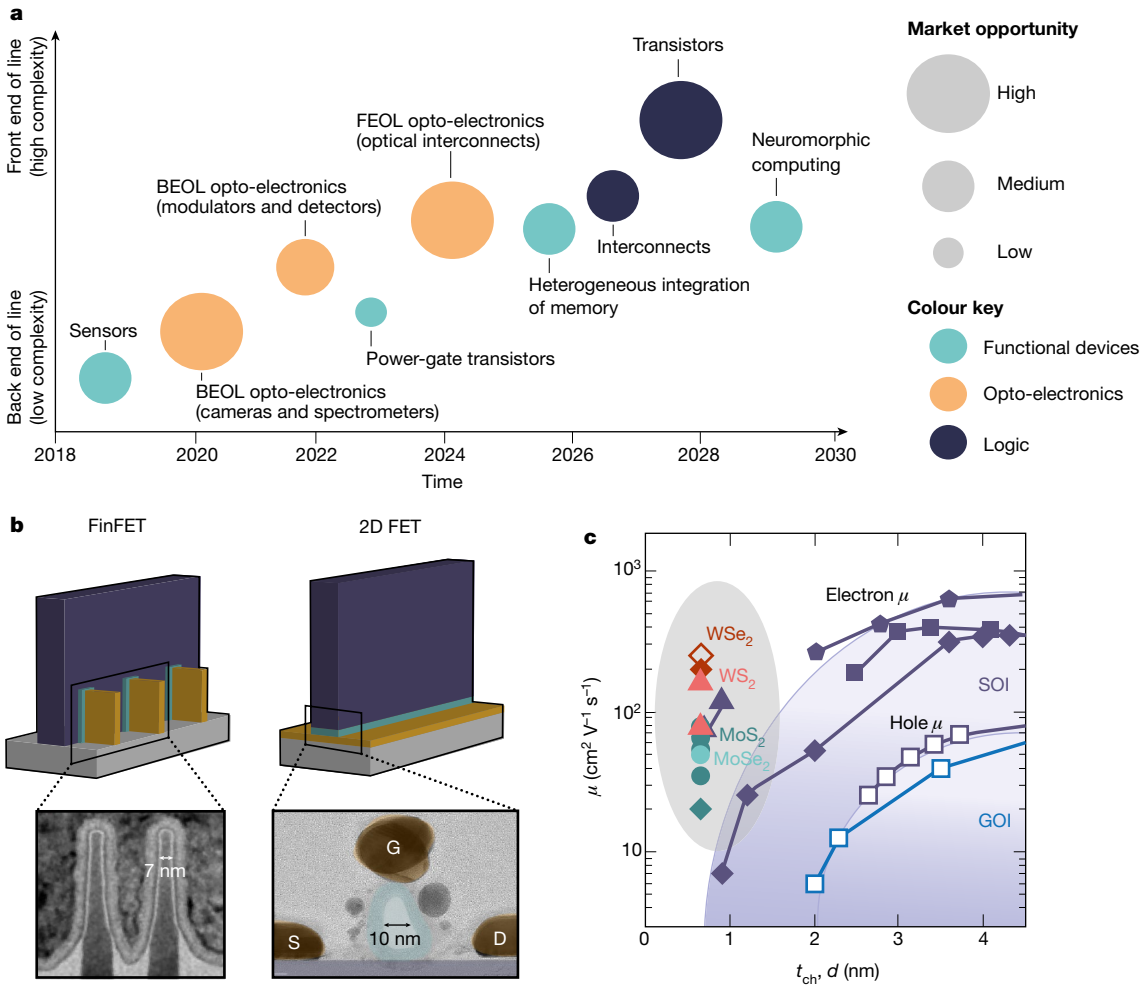


**Fig. 1 | Potential applications of 2DMs and modern transistor devices.** **a**, Applications of 2DM–Si technology mapped in time and integration complexity. The area of the circles is a rough qualitative estimate of addressable market opportunity (from refs [34,117]). The position of a circle indicates the time when the first products with the 2DM-based technology could potentially be introduced. Complexity increases when moving from back end of line (BEOL) to front end of line (FEOL) integration. **b**, Left, state-of-the-art FinFET transistor in production (adapted with permission from ref. [118], IEEE). Right, an example of a planar 2D FET being considered for future technology generation (adapted with permission from ref. [12], IEEE). The upper panels show structural diagrams (dark blue, gate; brown, channel; light blue, gate dielectric; grey, substrate) and the lower panels show images of parts of an actual device, originating from the positions shown boxed above. **c**, Mobility ($\mu$) versus channel thickness ($t_{ch}$) for semiconducting channels of TMDs[12] (within the ellipse) and for ultrathin silicon-on-insulator (SOI) and germanium-on-insulator (GOI) devices[110] (blue shaded areas). Filled (open) symbols represent electron (hole) mobilities. Adapted from ref. [11], American Chemical Society.

can only increase by adding a discrete number of fins or nanowires, multiple-stacked nanosheet FETs offer the additional benefit of continuous transistor widths[10]. To provide for higher device density and the associated cost reduction, one must continue to shrink the gate length and thus a thinner channel is required. Because the carrier mobility and transport along the thin-body channel of three-dimensional (3D) bulk semiconductors degrades substantially for thicknesses below 3 nm (Fig. 1c)[11], a new channel material that is thin and yet maintains good carrier transport is required.

### The rise of 2DMs

2D layered semiconductors have emerged as plausible candidates for FETs that require extremely thin channels because many 2DMs maintain good carrier transport even for atomically thin layers below 1 nm. For instance, the scale length for planar 2D FETs is approximately[6]:

$$\lambda \approx t_{ch} + \frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ox}$$

where $t_{ch}$ and $\varepsilon_{ch}$ are the channel thickness and channel $k$, respectively, and $t_{ox}$ and $\varepsilon_{ox}$ are, respectively, the thickness and $k$ of the gate oxide. Notably, $\lambda$ approaches 1 nm for monolayer transition-metal dichalcogenides (TMDs) using high-$k$ dielectrics ($k > 10$) with thickness below 2 nm, revealing the promising scalability of 2D FETs. Indeed, high-bandgap $MoS_2$ FETs with 10-nm gate length have been successfully demonstrated (Fig. 1b) with good subthreshold slope (80 mV per decade) and high 'on' currents (>400 μA μm$^{-1}$)[12]. Moreover, using a nanotube as the gate electrode, a $MoS_2$ FET with 1-nm gate length has been reported[13]. With lower-bandgap, higher-mobility materials such as black phosphorus, larger 'on' current (of about 1 mA μm$^{-1}$) is achievable[14]. It is also important to recognize that the use of 2D channel materials is compatible with other performance-enhancing technologies, such as (but not limited to) the use of negative capacitance to boost gate-to-channel coupling[15,16] and the use of stacked layers of channel materials to boost current drive per area. In addition, 2D FETs can be fabricated at low temperatures, a key requirement for attaining the next level of computing performance and energy efficiency using monolithic 3D integration of logic and memory[17].

## Non-computational systems

Beyond the endless interest in advancing modern Si electronics by exploiting the intrinsic scalability and low-power benefits of 2DMs for computational systems as mentioned above, there exists also an ever-widening opportunity to employ these atomic materials for

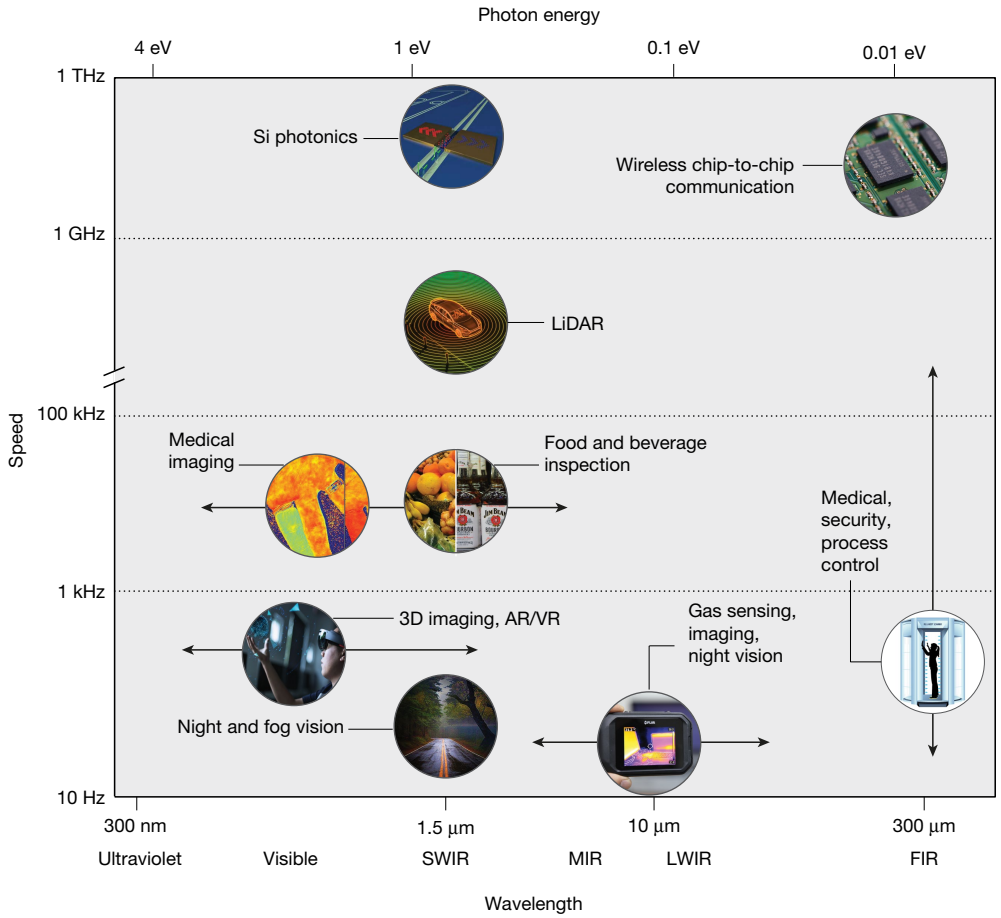


**Fig. 2 | Optoelectronic applications.** Technology areas of 2DM-based integrated opto-electronics, mapped in terms of required speed and operational wavelength range (lower *x* axis; the upper *x* axis gives the corresponding photon energy). AR, augmented reality; VR, virtual reality; SWIR, short-wave infrared; MIR, mid-infrared; LWIR, long-wave infrared; FIR, far infrared. Image credits: top row, left, adapted with permission from ref. [119]; second row, Shutterstock (https://www.shutterstock.com); third row, left, adapted with permission from ref. [120]; bottom row, leftmost and rightmost, Shutterstock.

non-computational systems[18–26], such as photodetectors and modulators for image sensors, light detection and ranging (LiDAR) and data communications (Fig. 2), as well as lasers, piezoelectrics, nano-electromechanical systems (NEMS), radio-frequency devices, magnetic devices, Hall sensors, and all sorts of gas, chemical and biological sensors. These diverse applications can be categorized as non-computational systems (colloquially termed 'more than Moore') and ideally realized on an integrated CMOS chip where Si devices provide the driver, read-out and peripheral circuitry necessary to form a complete system. Towards this goal, fully integrated prototype graphene–Si chips have been recently demonstrated, including graphene gas sensors[20], optical receivers[27] and image sensor arrays[19] on top of foundry or commercial chips with Si read-out electronics. (Here a foundry is a semiconductor business that manufactures the designs of other companies.) Furthermore, biomedical sensors featuring graphene transistors on Si substrates have been substantially advanced and are now available as a commercial product[28]. Progress towards TMD integration with Si chips is ongoing and will very much benefit from the back-end-of-line (BEOL) process techniques developed for graphene integration.

## Image sensors and spectrometers

Digital camera technologies have experienced a revolution in the past 20 years, thanks to the progress of CMOS-based image sensors, in terms of low-cost manufacturing, high resolution, high performance and compact footprint. The image sensor market was valued at $15 billion in 2017[29], and is predicted to grow, in part driven by the automotive, mobile and medical markets. Current low-cost and high-performance image sensors are based on silicon detectors integrated with a CMOS read-out integrated circuit, and in general they are sensitive only to the visible and near-infrared range (300–900 nm wavelength).

Considering the full infrared range of the spectrum, a much wider range of applications (such as night and fog vision, biomedical imaging, food inspection, gas detection and security) can be addressed; see Fig. 2. Even at longer wavelengths, terahertz rays can penetrate commonly used dielectric materials and allow detection of substance-specific spectroscopic features. The cost of image sensors for the infrared and terahertz range is much higher, because integration with Si CMOS is not monolithic and therefore more challenging. For example, image sensors based on III–V materials are bonded to CMOS read-out integrated circuits die by die, in contrast to Si CMOS image sensors. This limits the pixel pitch (typically >12 μm for commercial technology) and increases the cost (>$10,000 for a one-megapixel InGaAs camera). For room-temperature imaging of mid-infrared (thermal) radiation, silicon bolometers integrated with CMOS electronics are the leading technology. The speed (typically <50 frames per second), sensitivity and resolution are limited ($<10^5$ pixels).

In addition, many spectroscopic applications need access to the visible and infrared range at the same time. Another emerging imaging technology is 3D imaging for autonomous vehicles and augmented/virtual reality markets. Extension of 3D imaging into the infrared range gives less interference of ambient background light, and enables lower power consumption of active sources.

As the applications mentioned above require at the same time sensitivity to a broad wavelength band, low power, and low-cost production and integration, it is clear there is a strong need for a suitable (3D) imaging and photosensing platform that is monolithically integrable

with Si CMOS. 2DM-based photodetectors meet this need, and afford a fast broadband solution across the full spectral range from terahertz to ultraviolet[30], and can be integrated monolithically with Si CMOS readout integrated circuits in a BEOL process[19].

### Integrated photonics

Future data communication technologies, notably 5G, will require several orders of magnitude more bandwidth, attributable to the growth of the internet of things, autonomous vehicles, machine communication, and so on[31]. It is expected that silicon photonics will become the key enabler for high-density optical communications with low power consumption[32,33], and is likely to be used more and more in data and regional and long-haul communications, as well as in access networks. Integrated photonic devices operate as the optical link, where data from the electrical domain are transferred to the optical domain (via modulators), then transported with very low power loss and subsequently converted back to the electrical domain (via photodetectors). The requirements for integrated photonics are very stringent: high speed, small footprint, low energy consumption and low-cost manufacturing. Current Si photonics technology is based on Si modulators and Ge photodetectors integrated on Si waveguides, with continuing efforts exploring other III–V technologies. 2DMs have emerged as the active detector and modulator components with the potential to overcome the integration, cost and power consumption challenges[34].

## Integrated 2DMs on silicon

### Transistors

In modern technology, FETs have been the most important electronic devices, with silicon by far the most dominant semiconductor. For this reason, augmenting, rather than replacing, Si CMOS technology with 2D transistors is of central interest from the industrial perspective. At the outset, extensive studies were focused on graphene transistors with much of the resulting innovation and development subsequently applied to TMD FETs, particularly with respect to common issues such as material quality, contacts, dielectrics, doping and substrates[35–37]. The widespread research on 2D transistors has been very fruitful, resulting in an assortment of classical and unique ultrathin-body device structures with diverse electrical characteristics (Fig. 3). A major feature of most of the device structures is the inherent planar profile on account of the atomic sheet, which, combined with a low-temperature integration scheme, makes it straightforward to realize on virtually any level of a standard Si CMOS process flow.

For instance, the classical 2D FET (Fig. 3a) can produce n-type, p-type and ambipolar characteristics depending on the semiconductor, contact and doping. $MoS_2$ and $MoSe_2$ are typically n-type devices, while black phosphorus and intrinsic TMDs offer ambipolar characteristics that can be selectively engineered for p- or n-type transport. For more energy-efficient transistors based on improved gate coupling, the ordinary gate dielectric can be replaced by a ferroelectric insulator[16] such as $HfO_x$. Still steeper-slope turn-off characteristics can be achieved with a semiconductor–semiconductor atomically thin heterostructure that facilitates quantum mechanical tunnelling, commonly referred to as a tunnel FET (Fig. 3)[38,39]. Similarly, non-tunnelling vertical transport can be realized in other combinations of stacked heterostructures where the channel length can be as short as the thickness of two monolayers[39], about 1 nm or 1.5 nm for graphene–TMD or TMD–TMD heterostructures, respectively. Another emerging implementation is the so-called barristor, consisting of a semimetal–semiconductor Schottky-barrier junction. It is worth noting that both the tunnel FET and the barristor can also be realized with planar heterojunctions (Fig. 3a). In addition, unconventional device concepts such as the reconfigurable FET and the single-electron transistor (Fig. 3b) have been adapted to 2DMs with enhanced performance[40,41].

Invariably, these various 2D transistor characteristics present an opportunity for an expanded design space for 3D electronics founded on robust Si VLSI technology. However, there are several challenges in terms of optimizing the material integration and device structure for

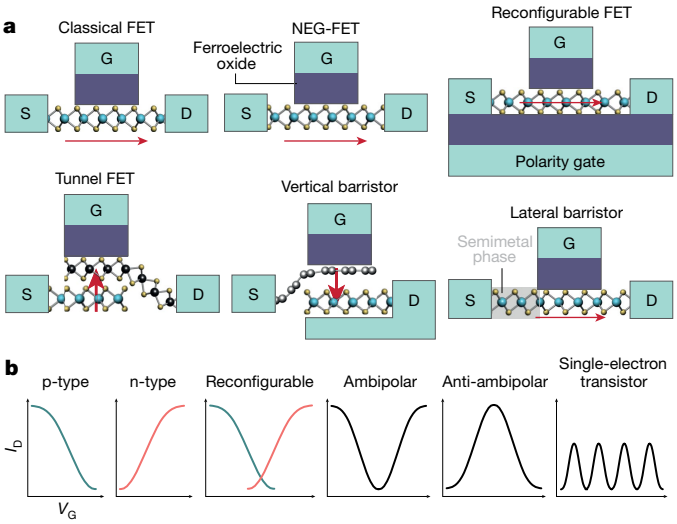


**Fig. 3 | Examples of 2D transistor devices and transport characteristics.** **a**, Illustration of various 2D planar device structures that can be readily integrated on virtually any level of a high-rise 3D silicon chip (S, source; G, gate; D, drain; NEG-FET, negative-capacitance FET). The tunnel FET is a semiconductor–semiconductor heterojunction and the barristor (vertical or lateral) comprises a semimetal–semiconductor junction. The reconfigurable FET has an additional gate, known as the polarity gate, which regulates the Schottky barrier at the metal–(ambipolar) semiconductor contact, thereby selecting on-demand either electron flow (n-type) or hole flow (p-type). These are simplified illustrations. Advanced device structures can utilize self-aligned gates or doping to minimize contact resistance, dual gates for better electrical control, and patterned polarity gates to reduce capacitance. Arrows represent the primary direction of carrier flow. **b**, The diverse electrical characteristics (drain current, $I_D$, versus gate voltage, $V_G$) afforded by 2D FETs are based on material choice and engineering of the device structure, contacts and doping. The single-electron transistor can be operated at low temperatures with constrictions or opaque contacts. This diversity opens up the design space for advanced 3D electronics.

maximum performance. Here, we highlight three device issues common to all the aforementioned transistor structures, namely contact resistance ($R_c$), doping and dielectrics/encapsulation. High contact resistance undoubtedly limits the maximum drive current in most 2D FETs. Nonetheless, in-depth research has demonstrated that relatively low $R_c$ (less than about 200 Ω μm) is achievable with good contacts[36,42]. In the ideal limit, even lower $R_c$ can be achieved at metal–TMD contacts according to the inverse relation[42] $R_c \propto n_q^{-x}$, where $n_q$ is the charge doping density and $x$ is between approximately 1 and 1.2. A value of $n_q > 10^{13}$ cm$^{-2}$ can produce $R_c < 100$ Ω μm, which satisfies the requirement of the 2015 edition of the international technology roadmap for semiconductors (ITRS) for scaled devices[39].

Contact doping is also beneficial for selecting the polarity of charge flow in ambipolar 2D semiconductors. However, conventional doping by ion implantation is not suitable for atomic materials due to physical damage, hence several alternative methods have been explored, with mixed results[36,43]. For practical adoption, process-friendly air-stable methods are most desirable and in this regard charge transfer from solid dopants using non-stoichiometric high-$k$ dielectrics via industry-friendly atomic layer deposition appears promising[44].

Another principal issue is dielectrics. 2D electron devices experience a performance boost when encapsulated with hexagonal boron nitride (hBN), a 2D dielectric, which offers a clean and smooth interface[35,36,43,45]. Despite the consensus on the benefits of hBN, progress towards wafer-scale uniform growth with quality comparable to exfoliated crystals has been rather limited. Therefore, alternative dielectrics are needed, at least in the near term. In this regard, we argue that some of the main attributes of hBN, such as the clean and smooth surface, can be accessed to some degree in conventional ALD (atomic layer

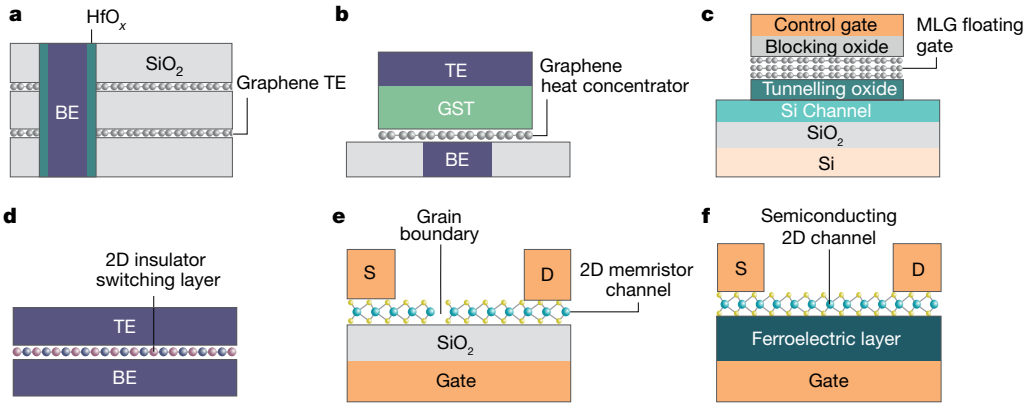


**Fig. 4 | Examples of the use of 2DMs in emerging memory types.** **a**, Monolayer graphene serves as an in-plane electrode in a 3D vertical RRAM to minimize the vertical thickness of the 3D stack[50]. BE, bottom electrode; TE, top electrode. **b**, Graphene is inserted between the $Ge_2Sb_2Te_5$ (GST) phase-change material and the bottom electrode in a PCM, and acts as a heat concentrator to reduce programming current[52]. **c**, Multi-layer graphene (MLG) is used to suppress capacitive coupling between memory cells, replacing the thick metal/nitride floating gate in conventional flash memory cells[53]. **d**, 2DMs in a vertical metal–insulator–metal (MIM) structure show a non-volatile memory effect down to a monolayer of hBN or TMDs[55–58]. **e**, Non-volatile switching behaviour is observed in the in-plane direction in gate-controlled $MoS_2$ lateral devices based on grain boundaries instead of filaments[59]. **f**, A 2DM channel is integrated with a ferroelectric memory layer to avoid diffusion of atoms from the ferroelectric material into the semiconductor transistor channel[54]. See main text for details of these memories.

deposition) dielectrics that can be engineered with a fine surface using precision nanofabrication processes. Moreover, ALD dielectrics like BeO that can also afford high thermal conductivity and optical phonon energies[46,47] may further deliver hBN-like benefits for 2D FETs.

## Memory

Solid-state memories and data storage devices have fundamentally changed the way we store and manipulate data. Consumer products such as smartphones are made possible by flash memory. Invariably, there is insatiable demand for higher-density, higher-capacity, lower-power, solid-state data storage devices. Today's computation workload requires access to massive amounts of data, resulting in substantial latency and energy consumption in moving data between off-chip memory (typically DRAM) and on-chip computation, a key bottleneck known as the memory wall[48]. To solve this problem, innovations that will provide large-capacity memory on the same chip as the computation units is called for.

Fortunately, over the past two decades, there have been plenty of innovations in memory and data storage devices. This includes non-volatile-memories, such as RRAM (resistive random-access memory), PCM (phase-change memory) and FeRAM (ferroelectric random-access memory)[49]. 2DMs have a wide range of physical characteristics that can potentially improve these emerging memories to a point where they become useful, as illustrated in Fig. 4. For instance, Sohn et al.[50] used graphene as the plane electrode of a 3D vertical RRAM. Graphene minimizes the vertical layer thickness and thereby allows more than 200 layers of vertical RRAM for high density and low cost. Similar to RRAM, PCM is a resistance-based memory but exhibits better endurance, with a lifetime[51] of more than $10^9$ cycles. However, the switching physics involve Joule heating of the PCM. To reduce PCM power consumption, Ahn et al.[52] used graphene as a thermal barrier between phase-change material, $Ge_2Sb_2Te_5$, and the bottom electrode (Fig. 4b), concluding that the small out-of-plane thermal conductivity of graphene confined the generated heat, resulting in about 40% less reset current. 2DMs have also shown promise for flash memory. For example, replacing the thick metal/nitride floating gate with one made from thinner multi-layer graphene (Fig. 4c) can suppress capacitive coupling between memory cells[53]. In ferroelectric memory, the direction of spontaneous electric polarization is used to store binary states. Much research effort has been devoted to integrating graphene, TMDs and black phosphorus[54] to FeFETs, as 2DMs naturally prevent diffusion of atoms from the ferroelectric material that cause interface instability (Fig. 4f).

In addition to integration with the conventional memory, novel switching mechanisms are also observed in 2DMs in a metal–insulator–metal (MIM) structure, as illustrated in Fig. 4d. Lanza and co-workers[55] reported multilayer hBN RRAM attributed to filamentary migration of metallic ions along hBN grain boundaries or defects, a phenomenon also reported in monolayer hBN[56]. Ge et al.[57] reported non-volatile switching in monolayer $MoS_2$, $MoSe_2$, $WS_2$ and $WSe_2$, alluding to a universal effect in TMD atomic sheets. Their area-dependent studies of $MoS_2$ memory is consistent with the theory of localized filaments. Non-volatile switching based on phase transition is also proposed in some 2DMs close to a phase boundary, such as[58] $Mo_{1-x}W_xTe_2$. A memory effect is also observed in planar $MoS_2$ configured in a transistor-like device structure (Fig. 4e), where the mechanism is based on grain boundaries[59].

Beyond memory elements, 2D transistor selectors can be useful for avoiding sneak currents (unwanted leakage currents) in memory arrays. Current 2D FET selectors employ $MoS_2$ as it is the most common 2D semiconductor, demonstrating[60] 'off' currents below 2 fA $\mu m^{-1}$. In the same spirit, integrating $MoS_2$ with a capacitor in a one transistor, one capacitor (1T1C) DRAM cell can increase the retention time[60]. These effects—reduction in 'off' current and improvement in retention time—are due to the large bandgap of $MoS_2$.

## Interconnects

Over the last few technology generations, circuit delay due to wires has required more frequent insertion of buffers, which results in larger chip area and additional power consumption, diminishing the performance gains made by transistor scaling. Since the 130-nm technology node, copper has become the dominant interconnect material owing to its superior properties compared to aluminium. However, at smaller wire pitches, the resistance of Cu interconnects rises rapidly due to surface and grain-boundary scattering[61], and also to increased self-heating. Industrial practice is to use metals that have a better trade-off between reliability and wire resistance (for example, cobalt).

When Cu interconnects are used, diffusion barriers such as TaN prevent Cu from diffusing into the dielectric between two interconnects, causing short circuits. Although the barrier material is relatively thin (about 3 nm), it is still too thick because the total wire width is less than 20 nm and the barrier material is less conductive, resulting in a higher effective resistivity of the wire. Moreover, conventional barrier materials lose their ability to block Cu diffusion at thicknesses below a few nanometres. Present industry considerations include the use of ultrathin alternative Cu barrier materials, or switching to metals that

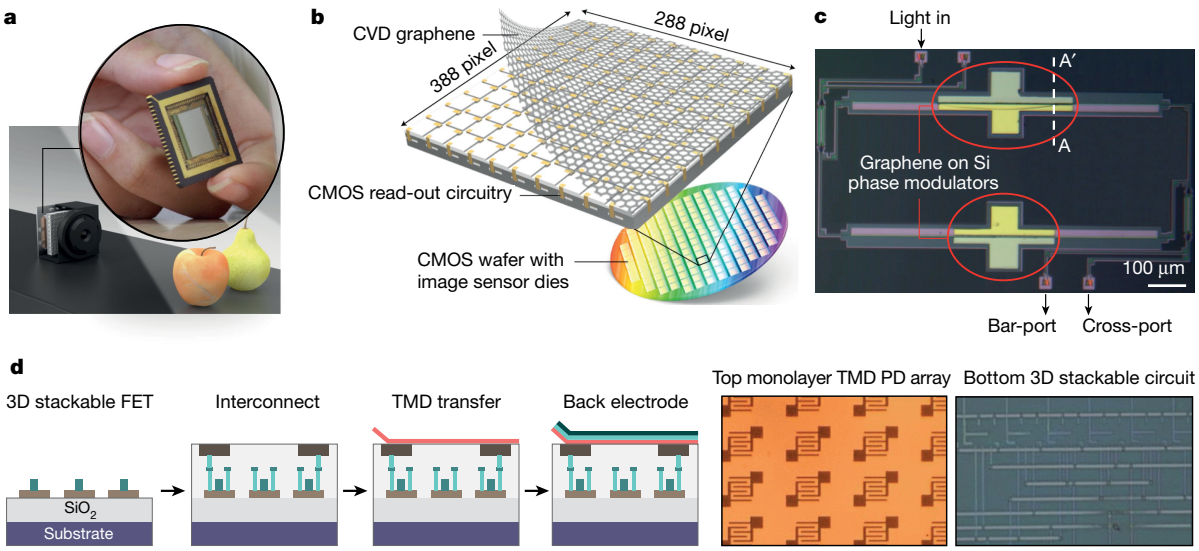


**Fig. 5 | Integrated graphene and 2D photodevices. a**, Artist's impression of a broadband camera setup based on CMOS-integrated graphene–quantum dot photodetectors. Inset, a photograph of the packaged monolithically integrated graphene-based image sensor. Image adapted from ref. [19], Springer Nature. **b**, Schematic representation of the integration process. Graphene was transferred on a read-out-integrated circuit die and processed into photodetectors by contacting, patterning and sensitization with colloidal quantum dots. Image adapted from ref. [19], Springer Nature. **c**, Graphene–silicon phase modulators with gigahertz bandwidth. The bar port and cross port are the Mach–Zehnder interferometer optical outputs. Image adapted from ref. [69], Springer Nature. **d**, A monolithic 3D image sensor with an integrated phototransistor array fabricated by using a large-area (direct-bandgap) monolayer TMD realized on a logic/memory hybrid 3D IC. Left to right, the first four panels show the process flow, the fifth shows an image of the photodetector (PD) array, and the last shows the interconnect wiring. Image adapted with permission from ref. [75], IEEE.

do not require a barrier layer. Single-layer graphene is an effective Cu diffusion barrier despite its atomic thinness[62], with analysis predicting an 8% boost in processor speed mainly due to reduced effective resistivity[63]. Besides graphene, $MoS_2$ and hBN are also capable of suppressing Cu diffusion into surrounding dielectrics[64]. It is also important that a CMOS compatible process is available for integrating these new materials into the nanoelectronic fabrication process. Li et al.[65] reported graphene growth directly on a Cu wire at a temperature below 400 °C.

In short, 2DMs would be beneficial for lower-level, tight-pitched metal wires. In this regard, engineered 2D wires—such as $FeCl_3$-doped multilayer graphene ribbons—have higher current-carrying capability and improved resistivity (compared to Cu wires scaled below 30 nm); such wires are therefore potential candidates to augment Cu interconnects for future technology nodes that require smaller wires[66].

## Graphene–integrated photonics

Graphene detectors, modulators and switches have a wide range of advantages, as they offer high speed, wide spectral bandwidth, low power consumption and monolithic integration with Si CMOS electronic drivers[30,34]. In addition, the production process is very versatile: very similar fabrication processes can be used to make ultrafast photodetectors, modulators and switches. One graphene layer can be used to gate another graphene layer, and so there is no need for chemical doping. Devices based on such double-layer designs can be used for both detector and modulator[67,68]. Owing to its broadband character, graphene has been integrated with several types of optical circuitry based on Si (using wavelengths around 1,500 nm) or SiN (wavelengths around 800 nm)[34]. Moreover, graphene-based modulators can operate[68] with a drive voltage below 2 V, and thus can be driven by conventional CMOS circuitry. Both phase and absorption modulators have been integrated with silicon photonics, and high-rate (10 Gbit $s^{-1}$) binary transmission of a non-return-to-zero data stream over 50 km of single-mode fibre was recently demonstrated[69] (Fig. 5c). A comparison of the relevant figures of merit using commercial and competing technologies is provided in the tables of ref. [34].

In addition, photodetectors with an operation speed above 180 Gbit $s^{-1}$ have been realized[70,71] by exploiting the ultrafast dynamics of photothermoelectric effects. Using gate-defined junctions[72], device schemes for zero-bias operation have been devised[70]. The highest reported responsivity[73] was 0.34 A $W^{-1}$, although the relevant figure of merit for graphene-based photodetectors is the voltage responsivity because graphene detectors are typically based on the photothermoelectric effect (that is, light absorption effectively acts as a voltage source). This implies that the device can be operated without a trans-impedance amplifier as the conversion from voltage to current can be omitted. Although substantial progress has been made in the fabrication of photonics devices in a pilot CMOS foundry environment[74], current challenges for integration with Si photonics include: the large-area transfer of graphene with mobility of at least a few thousand $cm^2\ V^{-1}\ s^{-1}$; appropriate dielectric and encapsulation schemes for low-voltage and hysteresis-free operation; and low-resistance contacting through a 'damascene' process (in which the contact is made by first depositing the dielectric onto the substrate, and subsequently patterning the contact hole which is then filled by metal deposition).

## Graphene camera for visible and infrared light

Hybrid integration of TMD-based phototransistors with high-density interconnects has been demonstrated in a 5 × 5 pixel array[75] (Fig. 5d). By employing graphene–quantum dot photodetectors, a fully integrated image sensor array of 388 × 288 pixels has been realized by integrating graphene with a CMOS readout integrated circuit[19], and operation as a digital camera was shown for both visible and infrared light (300–2,000 nm; Fig. 5a, b). This wavelength range is currently not available for any commercial photodetector or image sensor. The integration was based on a BEOL process of graphene onto the Si CMOS die, including a sensitizing layer of PbS colloidal quantum dots that was spin-cast on top of graphene. The functional elements of the CMOS circuitry contained all the trans-impedance amplifiers, compensation resistors and biasing/processing circuits. Despite the high yield of working detector pixels (>98%), the uniformity of the image sensor is expected to improve a great deal in the future by employing a dry-transfer approach. The figures of merit and comparison with competing technology can be found in the supplementary information of ref. [19], indicating compelling performance characteristics.

Future graphene–CMOS integrated image sensors based on side contacts will increase the active area and improve the contact resistance.

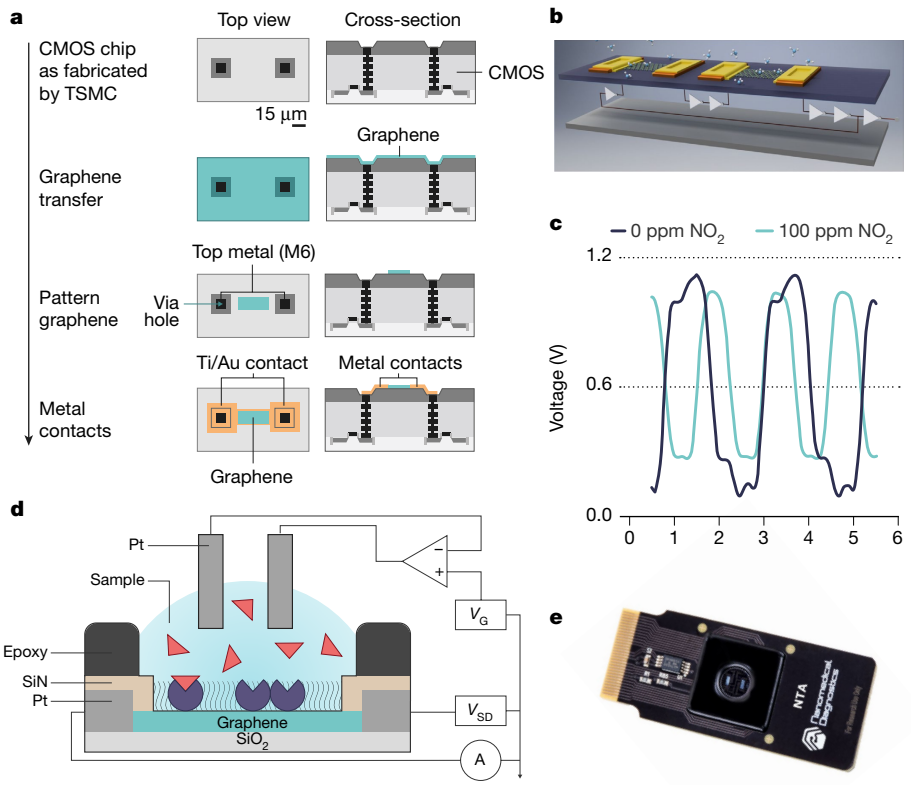


**Fig. 6 | Graphene sensors integrated with Si read-out electronics.** **a**–**c**, A graphene gas sensor. **a**, BEOL process flow for integrating a graphene gas sensor on top of a foundry Si CMOS chip. TSMC, Taiwan Semiconductor Manufacturing Company. **b**, 3D illustration of the monolithic graphene–Si sensor platform, featuring graphene chemiresistor gas sensors (formed as in **a**) integrated with Si transistors (shown schematically as triangles) to form a ring-oscillator circuit. **c**, Changes in ring-oscillator frequency and phase in response to a changed concentration of $NO_2$ gas. **d**, **e**, A graphene bio-sensor. **d**, Illustration of the device structure and read-out circuitry of a graphene field-effect bio-sensor. **e**, Picture of the complete packaged commercial bio-sensor. **a**–**c**, Images adapted from ref. [20], Springer Nature; **d**, **e**, images adapted from ref. [28], Springer Nature.

In general, these advances in BEOL integration of graphene photodetectors with Si CMOS pave the way to the development of 2DM-based image sensors for infrared and terahertz frequencies.

### Sensors

Contemporary articles provide broad reviews and benchmarking of a wide variety of sensors based on 2DMs[23–25], and represent an excellent resource for readers interested in sensor science, progress and challenges. From a technology perspective, sensors using 2DMs for gas, chemical and biological detection are straightforward to integrate with Si CMOS technology because only the last layer of the BEOL integration is necessary, which relaxes process and contamination requirements and ensures exposure of the sensor material. A practical 2D-Si sensor chip platform will consist of Si read-out electronics connected through interlayer vias to the top layer of the chip, where graphene or TMDs have been transfer integrated and patterned accordingly to utilize a specific sensor modality. Such an integrated platform was recently demonstrated by Zanjani et al.[20], where graphene resistance-change devices (chemiresistors) were employed for toxic-gas sensing on top of a foundry Si CMOS chip containing the application-specific read-out circuitry (Fig. 6a–c). Moreover, commercial chips are now available featuring functionalized graphene field-effect bio-sensors (Fig. 6d, e) for selective biomolecular detection with comparable (or superior) performance to conventional devices[28]. Rapid development of commercial 2D-Si sensor platforms is probably imminent as the transfer integration or low-temperature selective growth of suitable 2DMs on Si progresses.

## Practical matters and integration challenges

There are hundreds of predicted stable layered materials[18,76–78] in a portfolio including semiconductors, semimetals, superconductors, insulators, and the new state of condensed matter known as topological insulators. To advance these materials for use in integrated 2D-Si CMOS applications, several notable challenges require further research and engineering efforts. (1) Ideally, the growth of single-crystal monolayers needs to be developed. The key step is to control the orientation of each grain during the nucleation or initial growth stage. It is anticipated that a single orientation could lead to a grain-boundary-free layer, which is beneficial for high-performance device applications and uniformity. (2) Nearly wrinkle-free and residue-free benign transfer processes are required. (3) The development of a bottom-up approach to enable the area-selective growth of 2D layers on a CMOS-ready substrate may be another attractive option. To achieve this goal, a location-selective nucleation process compatible with the underlying devices is needed.

### Wafer-scale growth

Wafer-scale high-quality graphene growth has been reported, and several approaches have been used. To combine fast growth (numerous nucleation points) and large-scale synthesis of single-crystal graphene, one has to rely on the preferential epitaxial organization of the graphene nuclei on the substrate. This has been shown on single-crystal catalytic metallic templates[79–82], such as Cu <111>, CuNi, Co and Pt, and on semiconducting Ge. $Cu/SiO_2/Si$ and Ge substrates[83,84], in particular, offer a wafer-based chemical vapour deposition (CVD) platform compatible with microelectronic processing. For 2D semiconductors, wafer-scale growth of TMDs using various methods—including CVD, metal-organic CVD (MOCVD), ALD and molecular beam epitaxy (MBE)—have also been reported[85–87]. CVD and MOCVD both rely on a nucleation step followed by the TMD lateral growth, a promising route that can be combined with predefined nucleation sites to grow localized single-crystal domains. Submicrometre devices could readily be achieved in a single-crystal domain with a size greater than[87]

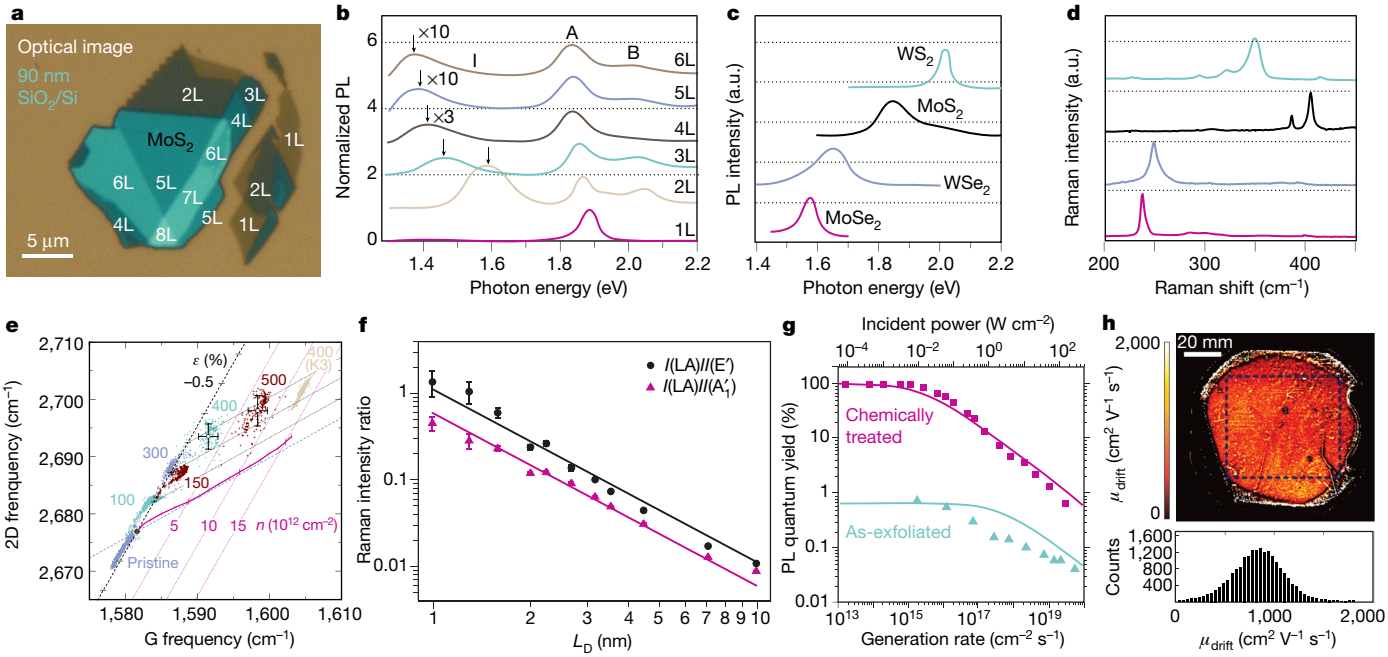


**Fig. 7 | Optical characterization of 2DMs suitable for inline metrology.** **a**, Optical colour image of a multi-layer $MoS_2$ flake on $SiO_2$/Si, revealing layer-dependent contrast sufficient for characterization. *n*L, number of layers. Image adapted from ref. [107], American Chemical Society. **b**, Normalized layer-dependent photoluminescence (PL) spectra of $MoS_2$ with three characteristic peaks; A and B are direct bandgap transitions, while I is an indirect transition. Image adapted from ref. [109], American Physical Society. **c**, **d**, Characteristic PL and Raman spectra of the four prototypical monolayer semiconducting TMDs. a.u., arbitrary units. **e**, Correlation between the frequencies of the G and 2D Raman modes of graphene. The green dot represents pristine graphene, with the black dashed line representing the effects of strain ($\varepsilon$) and the red line the effect of carrier density ($n$). The groups of colours are associated with the anneal temperature from pristine to 500 °C. Image adapted from ref. [110], Springer Nature. **f**, Dependence of Raman intensity ratios on the average interdefect distance ($L_D$) in monolayer $MoS_2$, providing a facile route for characterizing point defects. Error bars represent the standard error from the fitting process. Image adapted from ref. [112], American Physical Society. **g**, PL quantum yield as a function of pump power of as-exfoliated and superacid-treated (chemically treated) $MoS_2$ with much brighter photoluminescence from the (higher-quality) treated sample. Image adapted from ref. [111], AAAS. **h**, Main panel, non-contact terahertz-derived charge mobility ($\mu_{drift}$) map of 100-mm-wafer-scale graphene. Side panel, the mobility histogram. Such methods based on the Drude model of terahertz absorption can be broadly applied to 2DMs on insulating or semi-insulating substrates. Image adapted from ref. [114], Optical Society of America.

100 μm. An additional degree of freedom would be the formation of lateral heterojunctions between different TMDs[88,89] or between graphene and a TMD[90]. This could result in a very compelling and flexible method to manufacture 1D junctions at dedicated locations, or to fabricate van der Waals stacks of selected 2DMs[91].

## Direct-transfer-free growth methods

Conventional CVD requires a temperature of 900 °C or more to produce good-quality graphene[83,84,92], or 600–900 °C for crystalline TMDs[85,86,93], which hinders direct growth on CMOS-ready wafers with integrated circuits. To avoid the use of transfer processes, which are non-standard in microelectronic production, low-temperature direct growth (at <400–500 °C) of 2DMs are of great interest. On the other hand, direct growth places constraints on temperature, template choice and interface engineering. These constraints have an impact on the achievable material quality.

Plasma- or microwave-assisted CVD has been adopted to activate decomposition of the carbon source, and the growth temperature of graphene can be lowered[94,95] to 400–600 °C. Adding aromatic seeds such as polycyclic hydrocarbons or using certain carbon sources (for example, benzene) can further reduce the CVD growth temperature[96,97] to <300 °C. Recently, a low barrier has been reported for methane dissolution decomposition in bulk liquid gallium, which can produce graphene on various substrates at a temperature[98] of 50–100 °C.

For TMDs, the growth of $MoS_2$ single crystals on polyimide substrates at 450 °C has been achieved by simple CVD processes using ammonium molybdate or $Mo(NMe_2)_4$ as a precursor[99]. Delabie et al. have shown the growth of $WS_2$ atomic layers with the $WF_6$ and $H_2S$ precursors at a low temperature (300–450 °C) using Si or $H_2$ plasma as the reducing agent in CVD and ALD, respectively[100]. Although the quality of the obtained 2D layers needs further examination, these low-temperature growth approaches will probably enable the transfer-free integration of desired 2DMs into existing CMOS production technologies for applications where highly crystalline material is not necessary, such as sensors and interconnect stacks. Moreover, 2DMs will need to have a high purity, with metal contamination below $10^{11}$ atoms per square centimetre, for compatibility with silicon cleanroom processing.

## Scalable clean automated transfer

As mentioned earlier, several options are available to achieve large-area growth of 2DMs at wafer level if template choice and temperature budget are not restricted. During the subsequent transfer, 2DMs will form interfaces with manipulating polymers and transfer media[101]. Residues leading to doping effects, cracks and wrinkles are an unwanted by-product of the mechanical forces involved[102]. The most widely used method is polymer-assisted transfer, where various organic polymers are used as a mechanical support layer to protect and transfer the grown 2D layer. The most challenging step is to completely remove the residual debris and solvent without damaging the film. To avoid this step, direct-transfer methods have been proposed where the 2DM is directly transferred to the target substrate[82,103].

Arguably, the most promising approach is to combine polymer-assisted transfer with direct transfer, as follows. A layer of 2DM is grown on a polymer substrate. Under vacuum conditions, a movable polymer support is used to pick up a first layer of 2DM from the substrate, and this first layer is then used to directly pick up a second layer, mimicking the small-scale pick-up methods for flake stacking. Such a method has enabled the realization of hetero-stacks of $MoS_2/WS_2$

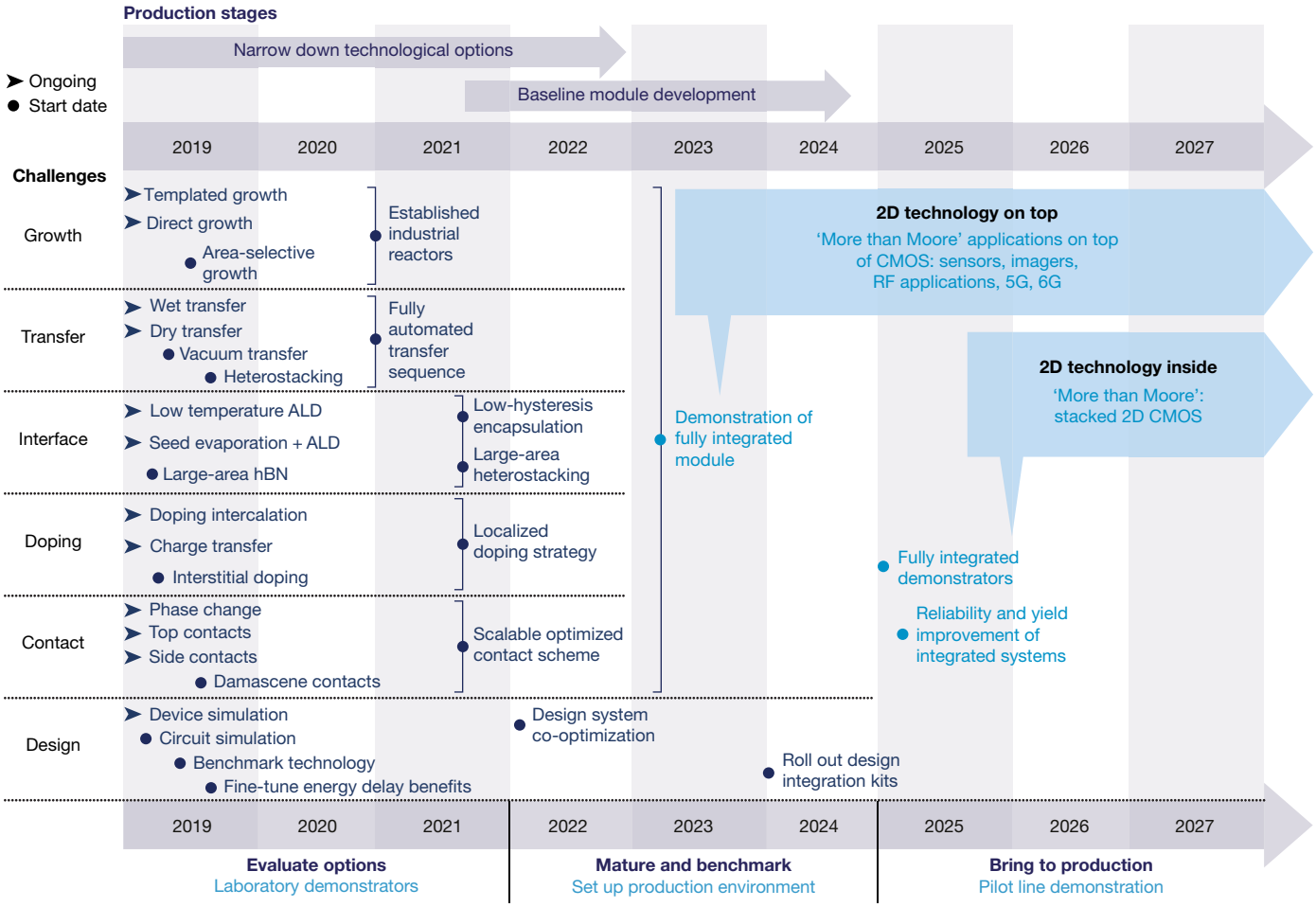


**Fig. 8 | Schematic visualization of the technology roadmap for the introduction of 2DMs in CMOS-compatible technology.** The effort to introduce 2DMs to enhance the ultra-scaled Si CMOS process ('2D technology inside') requires absolute control of the full integration process, and can only be successful if all the device and integration challenges listed in the left column are resolved. However in the near-term, 2DMs could also be integrated on top of CMOS circuitry mainly for optical input/output, imagers, sensors and radiofrequency applications ('2D technology on top'). These applications will be placed earlier in the market, as the material and integration requirements are less stringent compared to the needs for CMOS. As soon as automated transfer infrastructure can secure a high-yield transfer, the first 2D devices co-integrated with Si CMOS could be made available for these applications. It is important to make choices in the coming near-term and intensively upscale the growth and transfer processes by building infrastructure that is compliant with the needs and specifications of the CMOS industry. This roadmap has inherent uncertainty and should be interpreted accordingly.

with pristine interlayer interfaces and high spatial uniformity over the wafer scale[104]. This hetero-stacking procedure can be extended to diverse 2DMs if the delamination from the growth template is precisely understood and engineered. For example, graphene is easily peeled from Cu without damage after oxidation of the Cu interface. Recently, it was also demonstrated that in so-called electrochemical delamination, it is not the $H_2$ or $O_2$ bubbles[105] that are generating the delamination force, but an ionic intercalation effect. These studies highlight the importance of adhesion engineering of 2DMs and their growth templates in order to ensure a scalable, clean and automated transfer for building designer hetero-stacks with pristine interfaces at the wafer level.

## Inline metrology

Methods to rapidly characterize 2DMs at various stages of wafer-scale microelectronic fabrication processes are essential for quality control and industrial adoption of 2D-Si heterogeneous technology. In particular, optical methods are preferred owing to their non-contact simplicity, high-speed wafer mapping and micrometre spatial resolution, and this has led to their widespread adoption in the semiconductor industry. Several non-destructive optical methods have been developed for characterizing layer-dependent properties of different 2DMs (Fig. 7)[106]: (i) optical microscopy on optimized insulating underlayers offers sufficient contrast for estimating coverage, purity, number of monolayers and uniformity of graphene and TMD films[106,107]; (ii) ellipsometry can provide similar information on virtually any application-relevant substrate beyond the substrate restrictions of optical microscopy[108]; and (iii) Raman and photoluminescence (PL) spectroscopy are very powerful in their ability to simultaneously identify a wide variety of 2DMs, and the number and uniformity of the layers[57,106,109]. Moreover, PL can provide a direct measurement of the layer-dependent bandgap for semiconducting TMDs (Fig. 7b). In addition, the width or the intensity of the characteristic peaks in the Raman or PL spectra are indicators of the quality of the film (Fig. 7e–g), which can be correlated with disorder, doping or strain[110–112]. Furthermore, advanced optical techniques such as second-harmonic generation can map the strain gradients in non-centrosymmetric 2D layers[113], and terahertz time-domain spectroscopy can map the electrical properties and mobility of 2DMs on non-conducting substrates (Fig. 7h)[114]. Above all, these methods can be adapted inline in a cleanroom environment in order to monitor the quality of 2D sheets during microfabrication.

## Device aspects

In existing studies, important device aspects (such as contact resistance, doping and interfaces) have been shown to exhibit large

variability. This variability is partially linked to the fact that most of these devices were processed in laboratory environments, which are focused on innovation rather than on reproducibility. On the other hand, 2DM wafer-level growth and transfer are not as mature as modern Si CMOS processing, which is realized in industrial environments with precision process control. Increased control of the material interface environment will strongly reduce the variability of contact and doping. Localized introduction of molecules offering charge-transfer doping has been demonstrated, but it much reduces the process window for further integration[115]. Encapsulation of 2DMs in a dielectric with fixed charges for remote doping is probably the most CMOS-compatible method[44].

## Outlook and roadmap

Hetero-integration of specialized components and circuitry for novel computing paradigms (for example, quantum computing and brain-inspired/neuromorphic computing) with Si CMOS platforms will ensure the pace of steady improvements in computing power as classical scaling fades away. 2DMs are natural candidates for monolithic 3D integration for advanced functionality. Initially specialized components (for example, sensors, imagers, modulators and detectors) that can afford a reduced 2DM performance will enhance the functionality at the last layer of the BEOL. Later on, deeply embedded functionality with 2DM–Si co-optimization could advance emerging computing paradigms that require maximal material performance. However, at the moment, integration of synthetic graphene and 2DMs on Si wafer substrates is lacking production-suitable tools and associated infrastructure[116], which is holding back reproducible device fabrication and limits the performance compared to record device results achieved with exfoliated hetero-stacked flakes. Only a concerted effort of the research community and the semiconductor industry can overcome the hurdles preventing 2DMs from becoming a heterogeneous complementary technology.

In Fig. 8, we outline a roadmap for 2D device integration with Si CMOS. On the left are listed several generic challenges for 2D integration on CMOS. Initially in the laboratory fundamental properties are explored; in a subsequent phase, the research targets are redefined towards the development of up-scalable options that are found in a real production environment. In the mature and benchmarking phase, tools developed from research knowledge will be introduced in early pilot lines to assess the base steps in initial integration modules. These building blocks will be used for realization of the first circuitry in pilot lines. Finally, functional devices will be demonstrated in in the pilot-line phase. During this whole journey from first demonstration towards a product, technological options to meet the different challenges have to be assessed, and choices have to be made when selecting mature options. In Fig. 8 one can see that integration on top of CMOS (represented by the upper device inset) could come earlier to the market as the requirements are less demanding compared to those of 2DMs co-integrated in the BEOL (represented by the lower device inset). These early access technologies will pave the way to deeper integration levels of 2DMs.

As the semiconductor industry is a ubiquitous global business subject to many influences, this roadmap should be interpreted with caution: it covers areas of substantial uncertainty, particularly with respect to the timeline. The route to using 2DMs in future computing systems is via sustained research and development in order to meet the tightly defined requirements of contemporary semiconductor integration.

## Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41586-019-1573-9.

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