# Large-Area Monolayer $MoS_2$ for Flexible Low-Power RF Nanoelectronics in the GHz Regime

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A major contemporary challenge concerns the choice of semiconducting thin-film materials suitable for high-performance field-effect transistors on flexible substrates. Enhanced device performance has been achieved by utilizing conventional semiconductor materials, including crystalline Si and III–V semiconductors;[1–3] however, considering the overall device mechanical flexibility and thickness scalability for high mechanical performance and low operating power,[4] 2D materials have attracted substantial interest in this regard for flexible nanoelectronics. Graphene offers the fastest charge transport (carrier mobility ≈10 000 $cm^2\ V^{-1}\ s^{-1}$);[5–11] however, its lack of a bandgap makes it difficult to turn off (on/off current ratio <10) which is a major drawback for low-power electronics. Alternatively, molybdenum disulfide ($MoS_2$), a semiconducting 2D material with sizable bandgaps (≈1.8 eV for monolayer $MoS_2$ and ≈1.3 eV for bulk $MoS_2$)[12] can achieve on/off current ratio ≈$10^8$, a promising metric for digital electronics.[13] $MoS_2$ has shown mobilities as high as ≈170 $cm^2\ V^{-1}\ s^{-1}$ for few layers,[14] and ≈102 $cm^2\ V^{-1}\ s^{-1}$ for monolayer at room temperature,[15] which is comparable to poly-Si, and higher than metal oxide thin film transistors (TFTs).[4] The experimental effective velocity ($v_{eff}$) under high-field current saturation region of $MoS_2$ transistors were reported to be about $2.8 \times 10^6$ cm $s^{-1}$ for few-layer $MoS_2$,[16,17] and $1.1 \times 10^6$ cm $s^{-1}$ for monolayer $MoS_2$.[18] This range of $v_{eff}$ is sufficient to enable GHz speeds at submicron channel lengths, which is not accessible with organic and metal oxide TFTs.[19] The relatively high velocities, when combined with the large bandgap of $MoS_2$, make it very attractive for low-power radio-frequency (RF) applications. Moreover, 2D materials possess clear advantages, both in the scalability to ultrathin layer and elastic limit. In comparison with traditional semiconductors for flexible nanoelectronics, 2D materials can afford high electronic performance as well as high mechanical flexibility on arbitrarily large substrates.[4]

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We note that for RF circuits, effective saturation velocity rather than mobility is usually the relevant device metric due to the high terminal electric fields.[4] Previous studies have revealed the potential of few-layer exfoliated $MoS_2$ on $SiO_2$/Si substrate that achieved a transit frequency, $f_T$, of 42 GHz at a gate length of 68 nm (13.5 GHz for similar device on flexible substrate);[14] however, the exfoliation process is not scalable for practical or large-area applications. Very recently, monolayer $MoS_2$ grown by chemical vapor deposition (CVD) has been shown to achieve an $f_T$ of 6.7 GHz at a gate length of 250 nm on rigid substrates.[18] In this work, we demonstrate the first RF performance for $MoS_2$ field-effect transistors (FETs) on flexible substrates based on CVD-grown monolayers, featuring record GHz cutoff frequency and effective saturation velocity. Our result suggests that CVD-grown $MoS_2$ is suitable for high-frequency operation in large-area flexible nanoelectronic applications.

Large-area (millimeter-scale) monolayer $MoS_2$, the prototypical transitional-metal dichalcogenide (TMD) was grown by CVD on $SiO_2$/Si (**Figure 1**a). Figure 1b shows the transmission electron microscopy (TEM) image of monolayer CVD $MoS_2$ with lattice spacing of 0.27 nm confirming the as-grown material quality. Poly(methyl methacrylate) (PMMA) supported wet transfer process was used to transfer $MoS_2$ to various substrates, including $SiO_2$/Si and polyimide (PI). (The detailed information about the CVD-growth, uniformity of the CVD-grown $MoS_2$ film, and the transfer process can be found in Figure S1 and S2 in the Supporting Information). Figure 1c shows the comparison between the transferred and the as-grown $MoS_2$ samples from Raman and photoluminescence (PL) spectrum. A blue shift of the $E^1_{2g}$ peak in the Raman spectra (≈1.0 $cm^{-1}$) and the optical bandgap (≈45 meV) in the photoluminescence spectra are observed after transfer. It was reported by Conley et al. that with increased tensile strain, the $E^1_{2g}$ peak in Raman spectra shows phonon softening and photoluminescence shows bandgap reduction.[20,21] Our results suggest that there is a release of tensile strain (<1%) after transfer that can be attributed to the high-temperature CVD-growth process which induces residual tensile strain in the as-grown sample. Our observation is in agreement with similar trends as reported previously.[22] Moreover, the Raman and PL spectra also confirm the preserved quality of $MoS_2$ after the transfer process.

CVD-$MoS_2$ devices on $SiO_2$/Si were evaluated under ambient conditions for the initial investigation of the electronic performance of monolayer $MoS_2$. A schematic of the top-gate device structure with overlap between S/D and gate is shown in the inset in Figure 1d (the optical image and the mask design can be found in Figure S5 in the Supporting Information).

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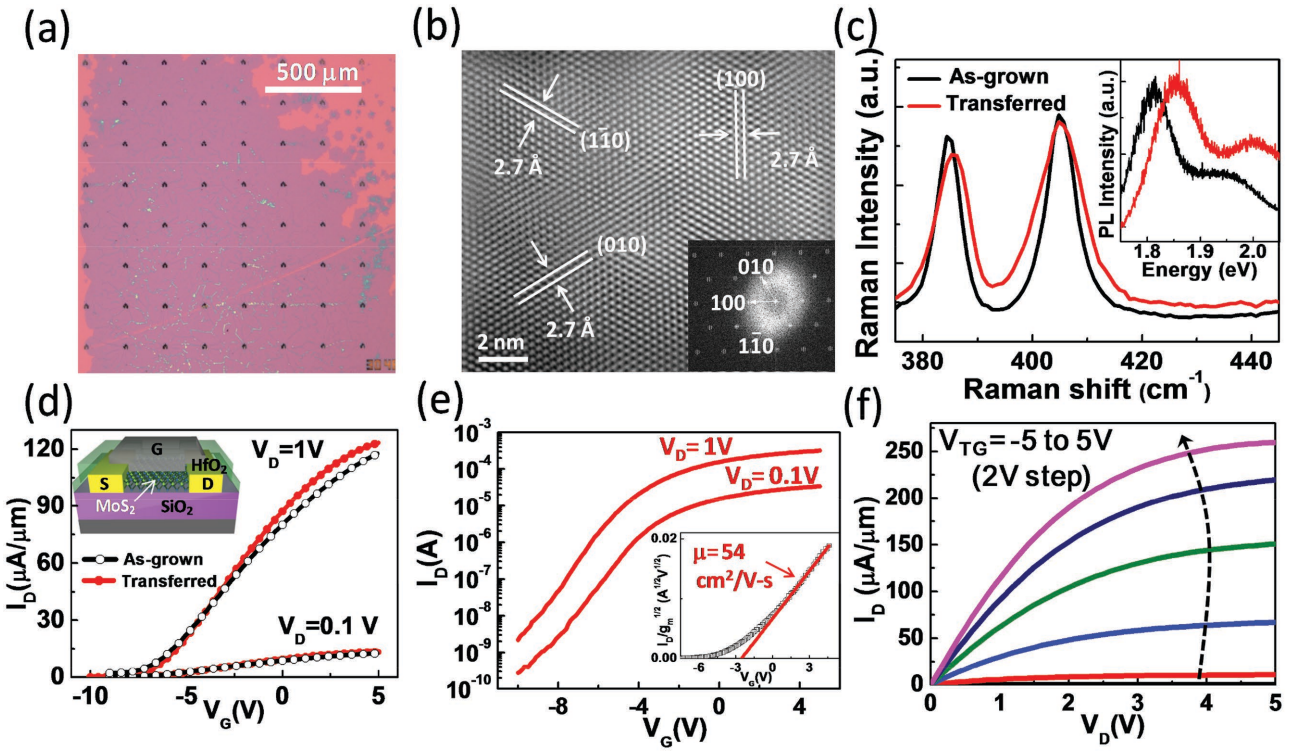


**Figure 1.** a) Optical image of mm-scale monolayer. b) FFT-filtered TEM image of monolayer CVD $MoS_2$ with lattice spacing of 0.27 nm and the inset is the corresponding FFT showing the spots that were used in the filter. c) Raman and photoluminescence (inset) spectrum before and after transfer confirming the preserved quality. d) $I_D$–$V_G$ characteristics are shown in linear scale. A comparison between the as-grown CVD $MoS_2$ FET and the transferred sample ($L_g$ = 1 μm) on $SiO_2$/Si confirming that the transfer process used in our process does not degrade the performance. Inset is a schematic of the top gate device structure with overlap between source/drain and gate. e) Transferred CVD-grown $MoS_2$ FET. $I_D$–$V_G$ with ON/OFF ratio ≥$10^5$ and $\mu_o \approx 54$ cm$^2$ V$^{-1}$ s$^{-1}$ based on the *Y*-function ($I_D/\sqrt{g_m}$) method (inset) that excludes $R_c$.[23] $L_g$ = 1 μm, $W$ = 2.6 μm. f) Transferred CVD-grown $MoS_2$ FET. $I_D$–$V_D$ characteristics in linear scale shows good saturation. High saturation current ($I_{sat}$) density ≈250 μA μm$^{-1}$ is achieved.

To verify the effect of the wet transfer used in our process, the transfer ($I_D$–$V_G$) characteristics of the as-grown and the transferred $MoS_2$ FET on $SiO_2$/Si are compared in the linear scale, as shown in Figure 1d. The comparison confirms that the wet transfer used in our process does not degrade the electronic performance. Representative $I_D$–$V_G$ characteristics of the transferred $MoS_2$ FET are shown in Figure 1e. The switching ratio ($I_{on}/I_{off}$) is greater than $10^5$. A low-field mobility ($\mu_o$) of 54 cm$^2$ V$^{-1}$ s$^{-1}$ and an $R_c$ of 2.7 kΩ μm are extracted based on the *Y*-function ($I_D/\sqrt{g_m}$) method.[23,24] Figure 1f represents the output characteristics ($I_D$–$V_D$) showing good current saturation with an ON-current of about 250 μA μm$^{-1}$. The enhanced device performance can be attributed to the high-*k* doping effect of the gate dielectric on the $MoS_2$ channel, wherein, the $HfO_2$ dopes the $MoS_2$ owing to its interfacial oxygen vacancies.[25] These device characteristics represent the state-of-the-art for CVD-grown monolayer $MoS_2$ FETs. Table S1 (Supporting Information) summarizes the device performance of previously reported CVD-grown $MoS_2$.[18,26–30]

Similar fabrication process was applied for top-gated dual-finger RF TFTs with gate-source/drain underlap to minimize the parasitic capacitance at high frequencies ($L_g$ = 500 nm, $W$ = 9 μm for each finger and the total width = 18 μm). The optical image and the mask design can be found in Figure S5 in the Supporting Information. **Figure 2**a,b shows the $I_D$–$V_G$ and $I_D$–$V_D$ characteristics of the transferred CVD-grown $MoS_2$ FETs on flexible PI substrate, respectively. $\mu_o$ = 22 cm$^2$ V$^{-1}$ s$^{-1}$ and $R_c$ = 9.4 kΩ μm are extracted from the *Y*-function method (more information about the $G_m$, and mobility extraction from different devices can be found in Figure S6 and S7 in the Supporting Information). The saturation current ($I_{sat}$) is about 85 μA μm$^{-1}$, an order of magnitude higher than our previous result on flexible exfoliated $MoS_2$.[31] The increase of the contact resistance in this case, however, is due to the underlap design resulting in ungated source/drain access regions. **Table 1** summarizes the performance of contemporary flexible $MoS_2$ FETs including both CVD-grown and exfoliated devices.[31–36] It is noted that mobility can be improved by increasing the layers of $MoS_2$, and a degradation of mobility is often found while converting the substrate from rigid to flexible substrate with a similar fabrication process, which can be attributed to the increased surface roughness and poor thermal conductivity of common flexible substrates.[14,35] Multicycle three-point mechanical bending experiments demonstrate the robustness of our flexible $MoS_2$ device. As shown in Figure 2c, RSA-G2 dynamic mechanical analyzer (DMA) with three-point bending fixture is used for repeated bending up to 10 000 cycles. The devices were at the center of curvature of the substrate for the bending experiments. A tensile strain of 1% was applied during the multicycle bending test. The transfer characteristics of flexible $MoS_2$ transistors reveal a strong stability even after 10 000 cycles of bending (more information about the




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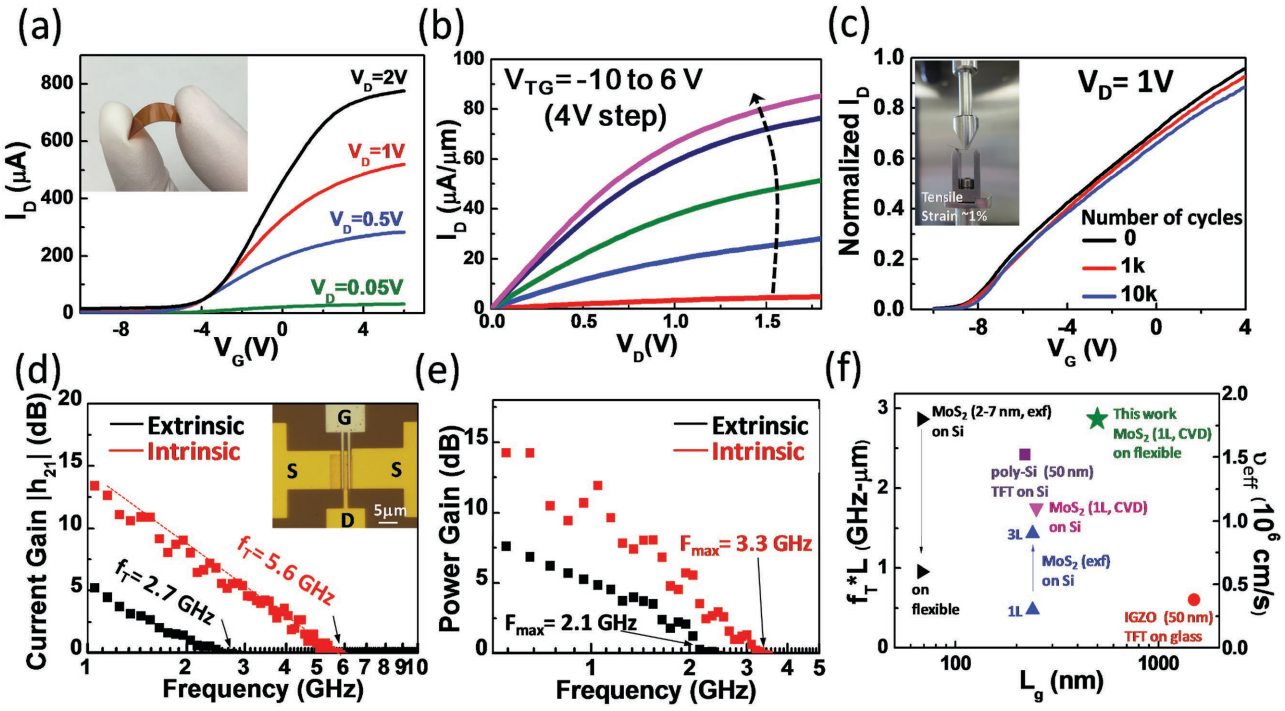


**Figure 2.** a) Electrical characteristics of flexible $MoS_2$ FETs ($L_g$ = 500 nm) at 300 K. Inset is an optical image of the flexible sample. b) $I_D$–$V_D$ characteristics indicate negligible Schottky barrier in the linear region, and current saturation at high fields. Drain current achieves ≈85 μA μm$^{-1}$, which is an order of magnitude higher than our previous result on exfoliated $MoS_2$.[31] c) A tensile strain of 1% was applied during the multicycle bending test. The transfer characteristics of the flexible $MoS_2$ transistors demonstrate strong stability even after 10 000 cycles of bending. Inset is the optical image of the three-point bending fixture. d) Intrinsic $f_T \approx 5.6$ GHz was achieved. Device width is 18 μm. The gate bias is at peak $G_m$ and $V_D = 2$ V. Inset is an optical image of the RF TFT. e) The power gain (U) versus frequency. The power gain considered is the unilateral power gain. Operating at the same DC bias point, an intrinsic $f_{max}$ of 3.3 GHz was extracted. f) RF TFT performance benchmarking to prior $MoS_2$ FETs and similar inorganic TFTs (<100 nm film thickness). The comparison indicates our $f_TL$ and $v_{eff}$ are the highest on flexible substrates and similar to the highest exfoliated $MoS_2$ values on rigid substrate. Data taken from ref. [14] (right triangles), ref. [39] (square), ref. [18] (down triangle), ref. [40] (up triangles), and ref. [19] (circle).

strain-dependent DC performance can be found in Figure S8 in the Supporting Information).

We investigated the high-frequency properties of flexible CVD $MoS_2$ TFTs based on two well established RF performance metrics; the unity current gain and unity power gain cutoff frequencies. The frequency where the current gain is unity is called the transit frequency ($f_T$) and, similarly, where the power gain becomes unity is called the maximum oscillation frequency ($f_{max}$).[37] S-parameter measurements were conducted to determine the $f_T$ and $f_{max}$ using an Agilent Vector Network Analyzer (VNA-E8361C) and cascade electrical probe station. The high-frequency measurement results are illustrated in Figure 2d,e as current gain ($h_{21}$) and power gain ($U$), respectively. The power gain considered is the unilateral power gain. For maximum charge transport, the $MoS_2$ RF TFT was biased at the peak $G_m$ where $V_G = -1$ V and $V_D = 2$ V, yielding an extrinsic $f_T \approx 2.7$ GHz and $f_{max} \approx 2.1$ GHz. Subsequently, standard RF de-embedding was conducted using identical OPEN and SHORT structures[8,38] to de-embed the effect of parasitic capacitances and resistances in the device structure, and extract the intrinsic monolayer CVD $MoS_2$ RF performance metrics: $f_T \approx 5.6$ GHz and $f_{max} \approx 3.3$ GHz. Alternatively, another metric to evaluate the speed performance of RF TFTs is the effective saturation velocity.[4] Analytically, $f_T = v_{eff}/2\pi L$ under high-field conditions that yield maximum transport. In this regime, $v_{sat}$ can be estimated from the measured $f_T$ L$^{-1}$. As shown in Figure 2f, our $MoS_2$ RF TFTs afford $f_T$ L$^{-1}$ ($v_{eff}$) of 2.8 GHz μm$^{-1}$ ($1.8 \times 10^6$ cm s$^{-1}$) which is similar to the best exfoliated $MoS_2$ values on rigid substrates and higher than previously reported flexible $MoS_2$ and other inorganic TFTs with sub-100 nm thickness.[14,18,19,39,40]

Having obtained good mobility, drain-current saturation and $f_T$ and $f_{max}$ in the GHz range, flexible CVD $MoS_2$ amplifier and mixer circuits, the basic building blocks of RF systems, were fabricated and demonstrated for the first time. A flexible $MoS_2$ common source (CS) amplifier ($L_g$ = 0.5 μm, $W$ = 18 μm) is

**Table 1.** Summary of contemporary flexible $MoS_2$ thin-film transistors.

| Max mobility [cm$^2$ V$^{-1}$ s$^{-1}$] | $L_g$ [μm] | $MoS_2$ | Substrate | Reference |
|---|---|---|---|---|
| 22[a)] | 0.5 | CVD, 1L | PI | This work |
| 19[a)] | 0.5 | CVD, 1L | PI | [32] |
| 3 | 480 | CVD, 3L | PI | [33] |
| 30[a)] | 1 | Exf, ≈10 nm | PI | [31] |
| 19[a)] | 4.3 | Exf, ≈3.5 nm | PI | [34] |
| 29 | 1 | Exf, 3L | PEN | [35] |
| 8 | 4 | Exf, ≈58 nm | PET | [36] |

[a)]Mobility excludes $R_c$. Exfoliation (Exf); layer (L).

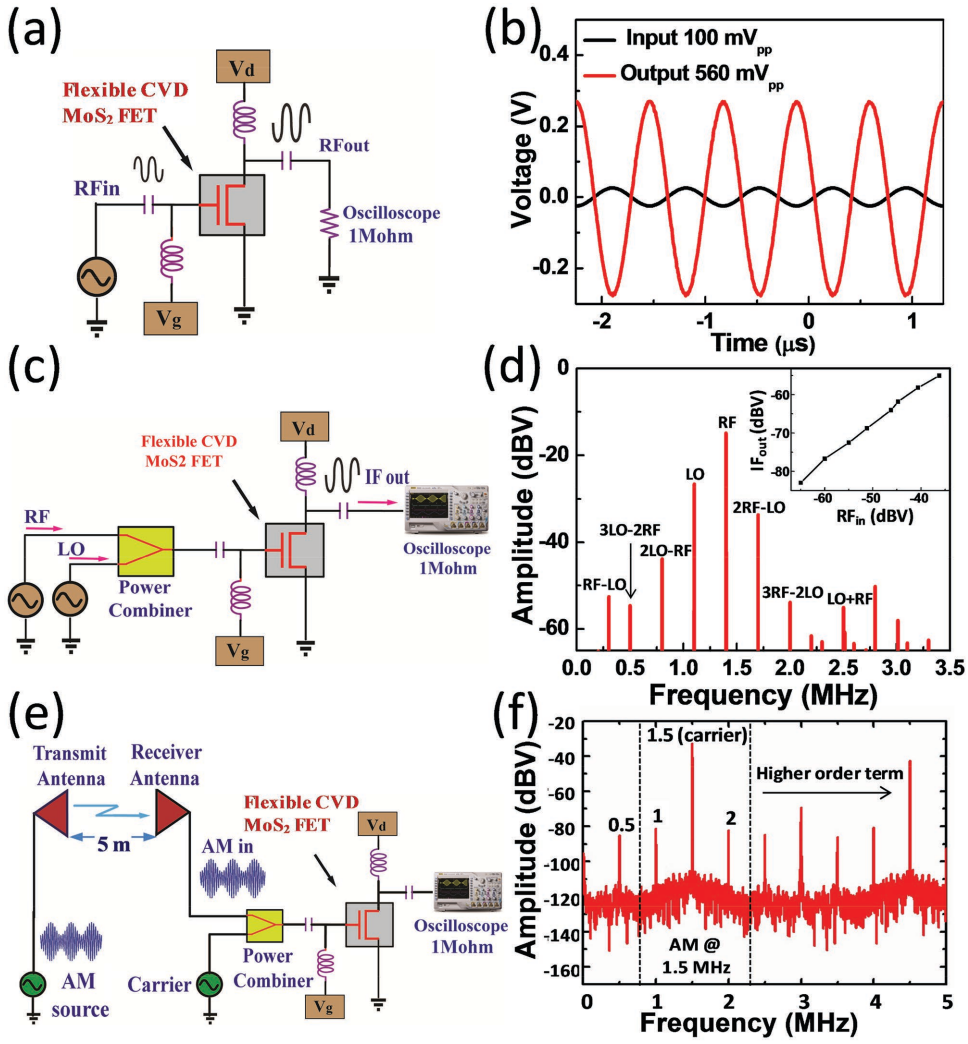


**Figure 3.** a) Circuit schematic of common-source amplifier based on $MoS_2$ flexible TFT ($f_{RF} \approx 1.4$ MHz). b) Input and output voltage waveforms of CS amplifier showing 15 dB gain. c) Circuit schematic of $MoS_2$ FET-based RF mixer ($f_{RF} \approx 1.4$ MHz, $f_{LO} \approx 1.1$ MHz, $f_{IF} \approx 300$ kHz). d) Output frequency spectrum of the mixer. The inset shows the conversion gain of the mixer is ca. –17 dB. e) Circuit schematic of $MoS_2$ FET-based wireless AM receiver. The distance between transmit and receiver antenna is 5 m, and the carrier frequency ($\omega_C$) is 1.5 MHz. f) AM receiver output spectrum showing clearly demodulated signal at 500 kHz.

shown in **Figure 3**a. The TFT is biased at the peak $G_m$ point ($V_G = -1$ V, $V_D = 2$ V). The RF input ($f_{in} \approx 1.4$ MHz) is provided by an Agilent signal generator and fed to the gate input of the TFT. The output of the TFT is connected to an oscilloscope (load resistance = 1 MΩ) and affords a gain of 15 dB at 1.4 MHz as shown in Figure 3b. In this work, the amplifier operating frequency is limited by the measurement setup. Further research is necessary to realize matched input and output impedance networks for resonant or broadband GHz operation.

In addition, a single transistor active mixer using flexible CVD $MoS_2$ FET was developed as shown in Figure 3c. In this design, we operate the FET in the nonlinear region of its output characteristics ($I_D \propto V_G^n$, where $n$ is ≈1.5–2 in FETs) for nonlinear signal processing such as frequency translation or mixing. The RF input ($f_{RF} \approx 1.4$ MHz) is power combined with a local oscillator ($f_{LO} \approx 1.1$ MHz) and fed to the gate input of the mixer. The output of the nonlinear mixer typically contains all the generated harmonics. It is low-pass filtered to obtain the intermediate frequency signal ($f_{IF} = f_{RF} - f_{LO}$). This IF output signal is measured using an oscilloscope and the frequency spectrum is displayed in Figure 3d. Equation S1–S5 in the Supporting Information describes mathematically the operation of this nonlinear mixer. The inset of Figure 3d shows the linearity of the mixer ($IF_{out}$ power vs $RF_{in}$ power) offering a maximum conversion gain of –17 dB. By improving the layout design, reducing parasitic capacitance and contact resistance, the conversion gain is expected to improve significantly, potentially affording positive gains.

We also demonstrate for the first time wireless amplitude modulation (AM) receiver using the flexible CVD $MoS_2$ RF FET. The schematic of the receiver is shown in Figure 3e. AM signal is generated by an Agilent signal generator with modulating frequency ($\omega_m$) = 500 kHz, carrier frequency ($\omega_C$) = 1.5 MHz, and the depth of modulation = 50%. The wireless communication distance between the transmit and receive antenna is 5 m. The



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received signal is combined with the carrier frequency through a power combiner, and fed to the gate input of the $MoS_2$ RF FET. Our flexible CVD $MoS_2$ FET performs analog signal processing by multiplying the carrier and modulating signals received from the antenna resulting in demodulated and harmonic signals at the transistor output as shown in Figure 3f. The detailed information about the measurement setup and the working principle are described in the Supporting Information (Figure S9).

In conclusion, flexible CVD-grown $MoS_2$ TFTs were demonstrated to be suitable for high-frequency operation. Our studies yield the highest performance for CVD-grown monolayer $MoS_2$ device properties on flexible substrates to date. Intrinsic transit frequencies of 5.6 GHz and maximum oscillation frequencies of 3.3 GHz have been achieved. The radio frequency performance of our device corresponds to $f_T L_g$ of ≈ 2.8 GHz μm, and $v_{eff}$ of ≈$1.8 \times 10^6$ cm $s^{-1}$ which are comparable to the best results obtained utilizing exfoliated multilayer $MoS_2$ on rigid substrates. Furthermore, multicycle three-point bending results demonstrated the electrical robustness of our flexible $MoS_2$ transistors after 10 000 cycles of mechanical bending. Additionally, basic RF circuit building blocks such as amplifier, mixer, and wireless AM receiver have been demonstrated. These collective results indicate that $MoS_2$ can serve as a suitable semiconducting material for low-power, high-frequency devices for large-area flexible nanoelectronics and smart nanosystems owing to its unique combination of large bandgap, high effective saturation velocity, and high mechanical strength.

## Experimental Section

*Device Fabrication*: For the devices made on Si, degenerately doped Si substrate was used as the bottom gate, and 270 nm $SiO_2$ grown by thermal oxidation was used as the gate dielectric. CVD $MoS_2$ was transferred (the detailed information about the CVD-growth and the transfer process can be found in Figure S1 and S2 in the Supporting Information). The active region was defined by electron beam lithography, followed by a dry etching process ($Cl_2$, 75 W, 1 min). Ag/Au (20/20 nm) deposited by electron beam evaporation was used as the source/drain electrode, and $HfO_2$ (30 nm) was deposited at 200 °C by the atomic layer deposition (ALD) method as the top gate dielectric. Pd (40 nm) deposited by electron beam evaporation was used as the top gate.

For the flexible devices, we used commercially available polyimide (Kapton) with a thickness of 125 μm as the flexible substrate, and spin-coated an additional liquid polyimide film (PI-2574 from HD Micro Systems) on the surface with a thickness of 13 $\mu$m to reduce the surface roughness. The liquid polyimide was cured at 300 °C for 1 h. The same spin-coating/curing process was repeated again on the opposite side in order to balance the residual strain induced by the curing process. $HfO_2$ (30 nm) was deposited at 200 °C by ALD on the bare PI for subsequent device fabrication.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] C. Wang, J. C. Chien, H. Fang, K. Takei, J. Nah, E. Plis, S. Krishna, A. M. Niknejad, A. Javey, *Nano Lett.* **2012**, *12*, 4140.
[2] H. Zhou, J. H. Seo, D. M. Paskiewicz, Y. Zhu, G. K. Celler, P. M. Voyles, W. Zhou, M. G. Lagally, Z. Ma, *Sci. Rep.* **2013**, *3*, 1291.
[3] C. Yoon, G. Cho, S. Kim, *IEEE Trans. Electron Devices*, **2011**, *58*, 1096.
[4] D. Akinwande, N. Petrone, J. Hone, *Nat. Commun.* **2014**, *5*, 5678.
[5] A. K. Geim, K. S. Novoselov, *Nat. Mater.* **2007**, *6*, 183.
[6] N. Petrone, C. R. Dean, I. Meric, A. M. van der Zande, P. Y. Huang, L. Wang, D. Muller, K. L. Shepard, J. Hone, *Nano Lett.* **2012**, *12*, 2751.
[7] N. Petrone, I. Meric, J. Hone, K. L. Shepard, *Nano Lett.* **2012**, *13*, 121.
[8] Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, P. Avouris, *Science* **2010**, *327*, 662.
[9] M. E. Ramón, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, D. Akinwande, *IEEE Trans. Nanotechnol.* **2012**, *11*, 877.
[10] J. Lee, K. N. Parrish, S. F. Chowdhury, T.-J. Ha, Y. Hao, L. Tao, A. Dodabalapur, R. S. Ruoff, D. Akinwande, presented at *IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, December 2012.
[11] L. Tao, J. Lee, H. Li, R. D. Piner, R. S. Ruoff, D. Akinwande, *Applied Phys. Lett.* **2013**, *103*, 183115.
[12] S. Han, H. Kwon, S. K. Kim, S. Ryu, W. S. Yun, D. Kim, J. Hwang, J.-S. Kang, J. Baik, H. Shin, *Phys. Rev. B* **2011**, *84*, 045409.
[13] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[14] R. Cheng, S. Jiang, Y. Chen, Y. Liu, N. Weiss, H. C. Cheng, H. Wu, Y. Huang, X. Duan, *Nat. Commun.* **2014**, *5*, 5143.
[15] A. Rai, A. Valsaraj, H. C. P. Movva, A. Roy, R. Ghosh, S. Sonde, S. Kang, J. Chang, T. Trivedi, R. Dey, S. Guchhait, S. Larentis, L. F. Register, E. Tutuc, S. K. Banerjee, *Nano Lett.* **2015**, *15*, 4329.
[16] G. Fiori, B. N. Szafranek, G. Iannaccone, D. Neumaier, *Appl. Phys. Lett.* **2013**, *103*, 233509.
[17] X. Zou, J. Wang, C. H. Chiu, Y. Wu, X. Xiao, C. Jiang, W. W. Wu, L. Mai, T. Chen, J. Li, *Adv. Mater.* **2014**, *26*, 6255.
[18] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande, S. Banerjee, *Nano Lett.* **2015**, *15*, 5309.
[19] L.-Y. Su, J. Huang, *Solid-State Electron.* **2015**, *104*, 122.
[20] H. J. Conley, B. Wang, J. I. Ziegler, R. F. Haglund , Jr., S. T. Pantelides, K. I. Bolotin, *Nano Lett.* **2013**, *13*, 3626.
[21] C. Rice, R. Young, R. Zan, U. Bangert, D. Wolverson, T. Georgiou, R. Jalil, K. Novoselov, *Phys. Rev. B* **2013**, *87*, 081307.
[22] M. Amani, M. L. Chin, A. L. Mazzoni, R. A. Burke, S. Najmaei, P. M. Ajayan, J. Lou, M. Dubey, *Appl. Phys. Lett.* **2014**, *104*, 203506.
[23] G. Ghibaudo, *Electron. Lett.* **1988**, *24*, 543.
[24] H. Y. Chang, W. N. Zhu, D. Akinwande, *Appl. Phys. Lett.* **2014**, *104*, 113504.

[25] A. Rai, A. Valsaraj, H. C. P. Movva, A. Roy, E. Tutuc, L. F. Register, S. K. Banerjee, presented at *Device Research Conf. (DRC)*, Columbus, OH, USA, June 2015.
[26] R. Kappera, D. Voiry, S. E. Yalcin, W. Jen, M. Acerce, S. Torrel, B. Branch, S. Lei, W. Chen, S. Najmaei, *APL Mater.* **2014**, *2*, 092516.
[27] L. Yu, Y.-H. Lee, X. Ling, E. J. Santos, Y. C. Shin, Y. Lin, M. Dubey, E. Kaxiras, J. Kong, H. Wang, *Nano Lett.* **2014**, *14*, 3055.
[28] H. Schmidt, S. Wang, L. Chu, M. Toh, R. Kumar, W. Zhao, A. H. Castro Neto, J. Martin, S. Adam, B. Özyilmaz, *Nano Lett.* **2014**, *14*, 1909.
[29] H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, P. D. Ye, *Nano Lett.* **2013**, *13*, 2640.
[30] H. Wang, L. Yu, Y. Lee, W. Fang, A. Hsu, P. Herring, M. Chin, M. Dubey, L. Li, J. Kong, T. Palacios, presented at *2012 IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, December 2012.
[31] H. Y. Chang, S. Yang, J. Lee, L. Tao, W. S. Hwang, D. Jena, N. Lu, D. Akinwande, *ACS Nano* **2013**, *7*, 5446.
[32] M. Amani, R. A. Burke, R. M. Proie, M. Dubey, *Nanotechnology* **2015**, *26*, 115202.
[33] J. Pu, Y. Yomogida, K. K. Liu, L. J. Li, Y. Iwasa, T. Takenobu, *Nano Lett.* **2012**, *12*, 4013.
[34] G. A. Salvatore, N. Munzenrieder, C. Barraud, L. Petti, C. Zysset, L. Buthe, K. Ensslin, G. Troster, *ACS Nano* **2013**, *7*, 8809.
[35] G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M. S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, *ACS Nano* **2013**, *7*, 7931.
[36] J. Yoon, W. Park, G. Y. Bae, Y. Kim, H. S. Jang, Y. Hyun, S. K. Lim, Y. H. Kahng, W. K. Hong, B. H. Lee, H. C. Ko, *Small* **2013**, *9*, 3295.
[37] F. Schwierz, *Proc. IEEE* **2013**, *101*, 1567.
[38] J. Lee, T.-J. Ha, H. Li, K. N. Parrish, M. Holt, A. Dodabalapur, R. S. Ruoff, D. Akinwande, *ACS Nano* **2013**, *7*, 7744.
[39] K.-M. Chen, T.-I. Tsai, T.-Y. Lin, H.-C. Lin, T.-S. Chao, G.-W. Huang, T.-Y. Huang, *Electron Device Lett., IEEE* **2013**, *34*, 1020.
[40] D. Krasnozhon, D. Lembke, C. Nyffeler, Y. Leblebici, A. Kis, *Nano Lett.* **2014**, *14*, 5905.



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ADVANCED MATERIALS

# Supporting Information

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## Large-Area Monolayer $MoS_2$ for Flexible Low-Power RF Nanoelectronics in the GHz Regime

*Hsiao-Yu Chang, Maruthi Nagavalli Yogeesh, Rudresh Ghosh, Amritesh Rai, Atresh Sanne, Shixuan Yang, Nanshu Lu, Sanjay Kumar Banerjee, and Deji Akinwande**

# Supporting Information

**Title** Large-area monolayer $MoS_2$ for flexible low-power RF nanoelectronics in the GHz regime

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## CVD Growth and transfer process for $MoS_2$

The $MoS_2$ atomic layer films were grown by a standard vapor transfer growth process (schematic of growth setup shown in Figure S1) within a quartz tube with an inner diameter of 22 mm and a single zone Lindberg/Blue M furnace. The starting materials were $MoO_3$ (15 mg) and sulfur (1 g) powder loaded in separate alumina crucibles, with the sulfur crucible outside the actual furnace and heated independently

using a heating tape. The substrates used for this work were surface cleaned 285 nm $SiO_2$ on Si.

The procedure for the growth consisted of loading the starting material and the substrates, followed by pumping down to base pressure (< 10 mTorr), and followed by purging the tube and the gas lines by flowing in UHP $N_2$ gas at 200 sccm. After 4 purging cycles the tube was filled with $N_2$ to 1 atm pressure at flow rate of 10 sccm. Then temperature of the furnace was raised to 850 ℃ at a rate of 50 ℃/min. When the temperature of the tube furnace was at 650 ℃, the sulfur was heated to 150 ℃ (+/- 5 ℃) and held at that temperature. The growth continued for 5 min at 850 ℃, and the heater to the furnace was turned off for cooling without any feedback. Heating of the sulfur was cut off once the furnace cooled down to 650 ℃.

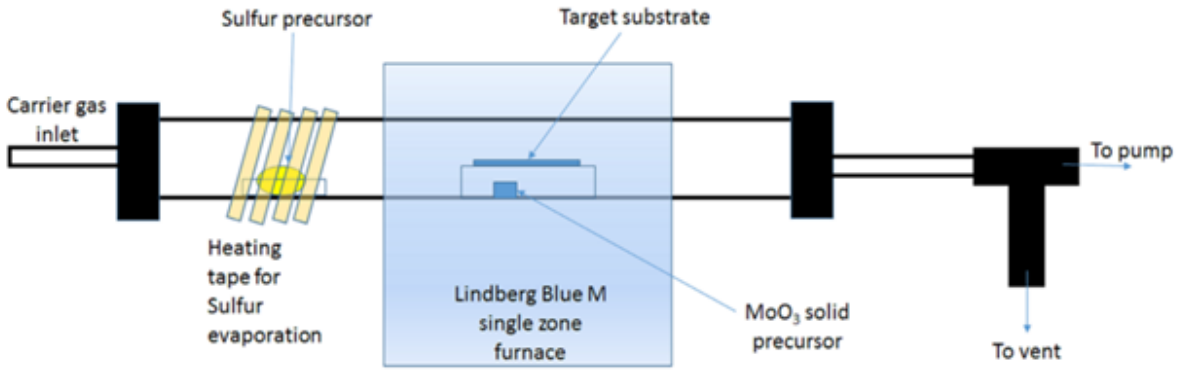


**Figure S1**. Schematic of the $MoS_2$ growth setup starting from $MoO_3$ and S.

To transfer the as–grown $MoS_2$ from $SiO_2$ to the target substrate, PMMA (A4) was spin-coated at 4000 rpm for 40 s and baked at 180℃ for 2 min. The coating and

baking process was repeated four times in total. Sodium hydroxide solution (NaOH, 2M) heated at around 80℃ was used to etch away the $SiO_2$ under $MoS_2$. This enabled the PMMA-supported $MoS_2$ to be separated from the original substrate which was then transferred on to the target substrate. After the transfer, the sample was stored in the desiccator overnight and baked at 180℃ for 2 min to improve the adhesion, and then soaked in acetone for 2 hours to remove the PMMA layer. Figure S2 shows the optical microscope images taken after completing the whole transfer process, showing that large area CVD $MoS_2$ can be successfully transferred to $SiO_2$ (Figure S2a) and PI (Figure S2b) substrate.

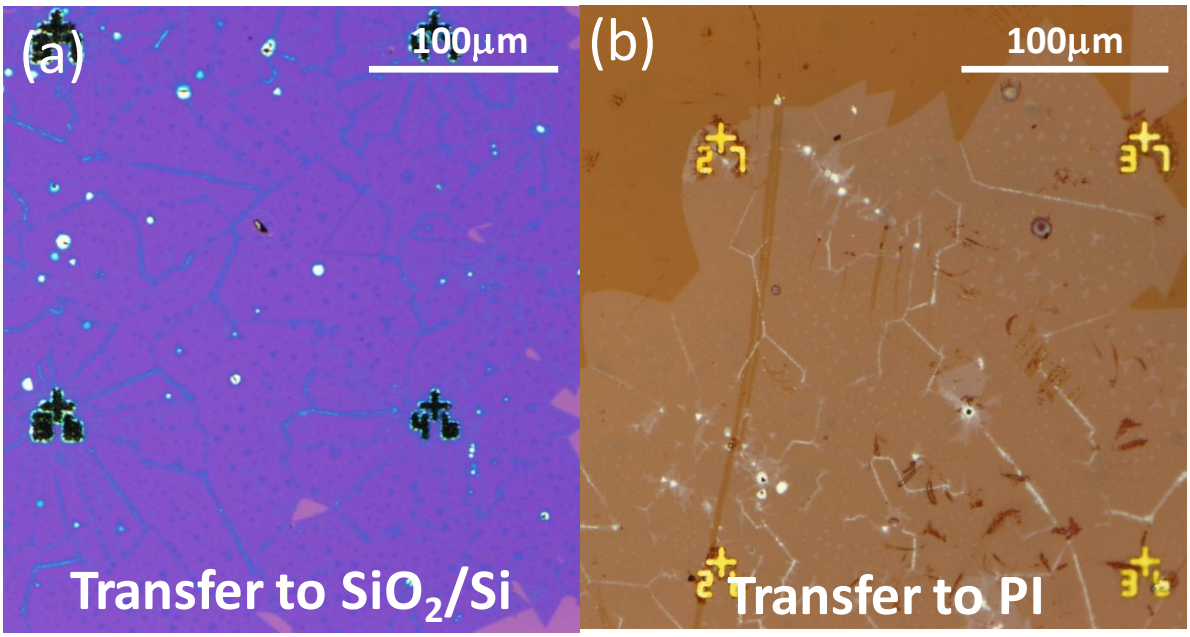


**Figure S2**. (a) and (b) are optical microscope images of CVD-growth $MoS_2$ transferred to $SiO_2$/Si and polyimide substrate respectively.

**Material Characterization:**

Raman and PL spectroscopy were done using a Witec Alpha 300 micro-Raman confocal microscope, with the laser operating at wavelength of 488 nm. Parameters in our mapping were (i) grating (Raman) = 1800 g/mm, (PL) = 600 g/mm; (ii) integration time/pixel = 1 s; (iii) resolution = 3 pixels/µm.

**Uniformity of CVD grown $MoS_2$**

In order to show the uniformity of the CVD grown film we obtained Raman spectra from 100 points over a 2 mm x 2 mm continuous region. Raman spectrum from points 200 microns apart were taken. In Figure S3a we point out the various typical features inside the continuous monolayer region. These features include grain boundaries (two or more domains coming together), bi-layer regions, few layer regions (3-5 layers) and bulk regions (> 6 layers). Each of these regions have specific Raman spectra that correspond to different peak separations between the $E^1_{2g}$ and $A_{1g}$ peaks as shown in Figure S3b. In Figure S3c we show the frequency of these different peak separations for the 100 spectra obtained. The results show that around 70% of the film is monolayer, 18% bi-layer regions and the rest is few layer or bulk region. In addition, from AFM analysis as shown in Figure S4, a scratch was made in the center region of

large area $MoS_2$ thin film to obtain the step height~0.8nm, which is consistent with monolayer thickness.

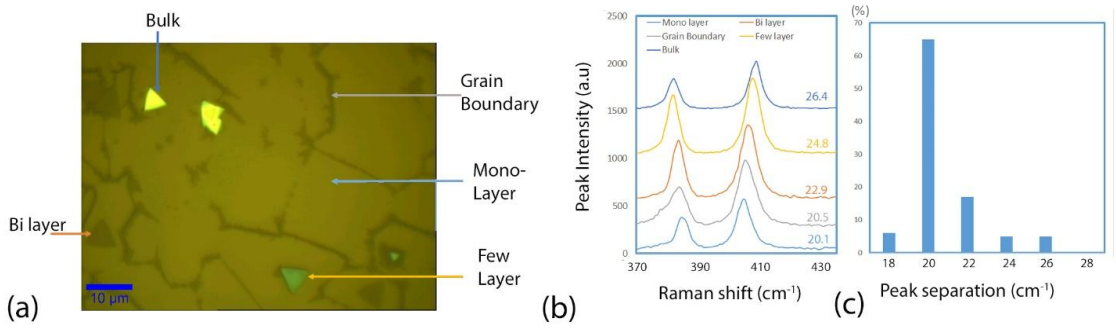


**Figure S3.** (a) Optical microscope image of a typical region for CVD grown $MoS_2$. (b) Raman spectra from regions marked in the optical image, (c) Frequency plot of peak separations for 100 points in 2 mm x 2mm area.

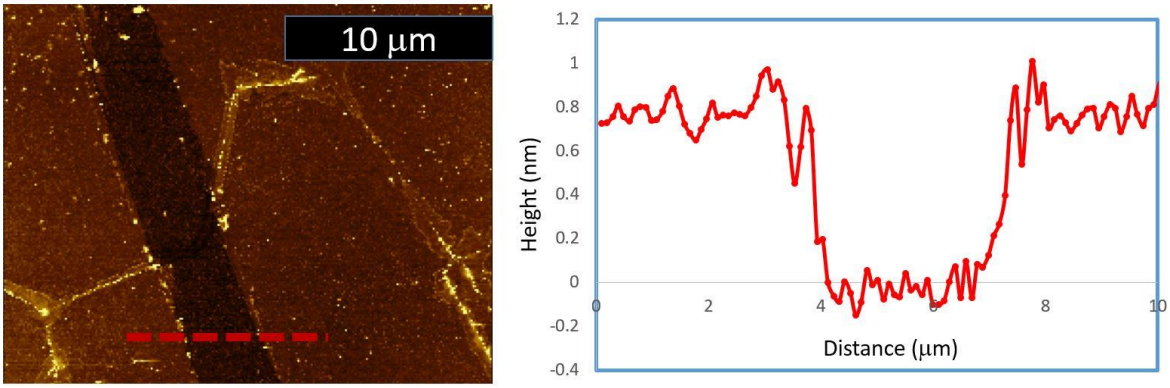


**Figure S4.** AFM analysis. A scratch was made in the center region of large area $MoS_2$ thin film to obtain the step height~0.8nm, which is consistent with monolayer thickness.

**Device layout on different substrates**

For device on Si, channel length is 1um determined by the gap between source and drain. For device on PI, gate length is 0.5um, and the gap between S/D and gate at each side is 0.125um. Optical image and mask design for both devices are shown in Figure S5. The contact resistance increase on flexible substrate is mainly due to the

underlap between source/drain and gate. The ungated source/drain access regions result in additional contact resistance compared to the device with overlapped source/drain and gate.

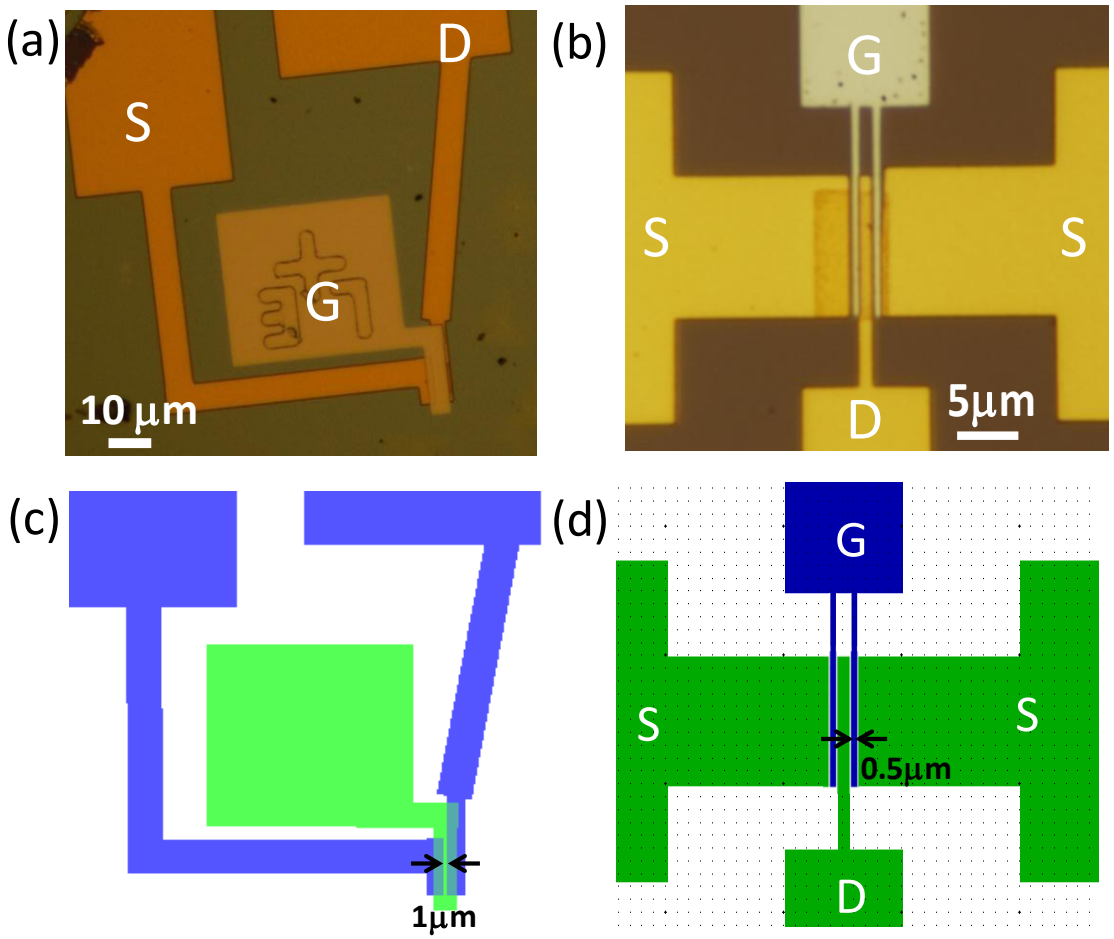


**Figure S5**. (a) Optical image for $MoS_2$ device on Si. Channel length is 1µm determined by the gap between source and drain. (b) Optical image for $MoS_2$ device on PI. Gate length is 0.5µm, and the gap between S/D and gate at each side is 0.125µm. (c) and (d) are the mask design for device on Si and PI respectively. The physical channel dimensions are typically within ±10% of the mask design.

**Table S1**. Summany for CVD-grown $MoS_2$ FET

| Gate Stack & Contacts | TG/$HfO_2$ Ag/Au | TG/$HfO_2$ Ag/Au | BG/$SiO_2$ 1T $MoS_2$ | BG/$SiO_2$ Au | BG/$SiO_2$ Ti/Au | TG/$HfO_2$ Ti/Au |
|---|---|---|---|---|---|---|
| Max Mobility ($cm^2/V \cdot s$) | 54 [a)] | 63 [a)] | 56 | 45 | 21 [a)] | 40 |
| $L_g$ (μm) | 1 | 4 | 2 | 10 | 1 | 1 |
| Ref | This work | [1] | [2] | [3] | [4] | [5] |

[a)] Mobility excludes $R_c$

**Device performance variation**

The low field mobility extracted from different devices on PI is in the range of 19~31 $cm^2/Vs$ attributed to slight material variations and device-device variations from microfabrication (Figure S6). A representative $G_m$ versus $V_G$ of the device on PI is shown in Figure S7.

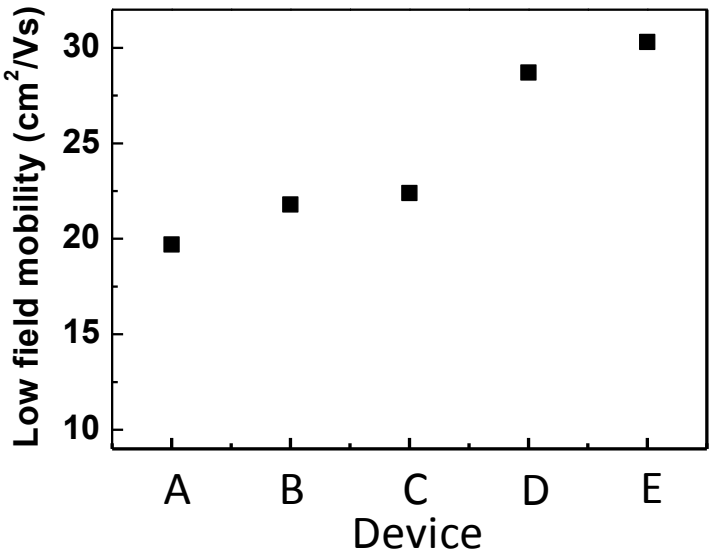


**Figure S6**. The low-field mobility extracted from different devices on PI is in the range of 19~31 $cm^2/Vs$.

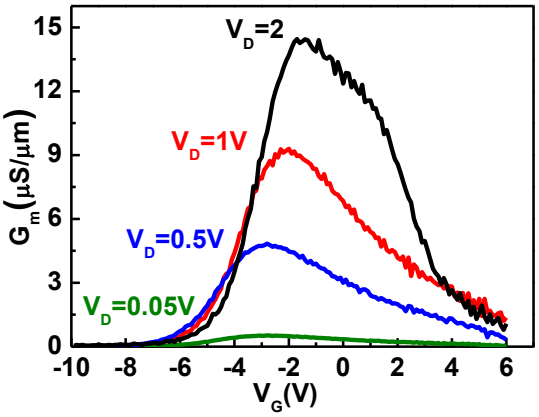


**Figure S7**. A representative $G_m$ versus $V_G$ of the device on PI.

**Device flexibility**

According to previous studies, cracks formation happens in high-k dielectric under ~2% tensile strain, and the device may fail.[6] As a result, DC performance under 1% was selected to verify the device flexibility. As shown in Figure S8, our devices show device stability within ±10% change for 4 out of 5 devices. We attribute slight sliding between the metal contact to $MoS_2$ as the main reason affecting the device performance under strain,[7] since no cracks or delamination were observed. Further studies to improve the adhesion between S/D metal to $MoS_2$ are required to improve reliability under strain.

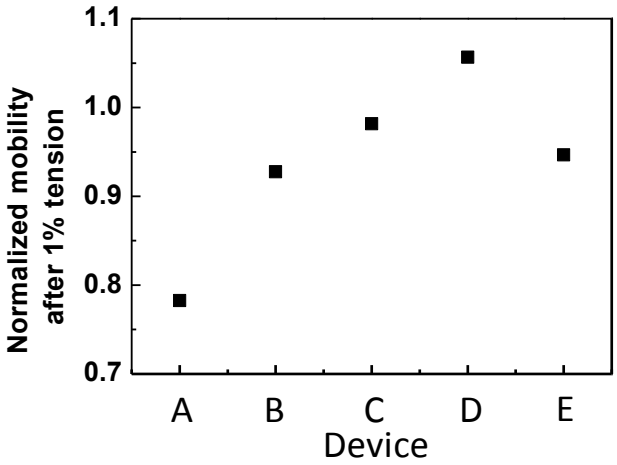


**Figure S8**. Normalized mobility after 1% tension. Our devices show device stability within ±10% change for 4 out of 5 devices.

**Active Mixer Analysis:**

Figure 3c shows the schematic of $MoS_2$ FET based mixer. The gate input ($v_G$) of this mixer is the sum of the RF input ($v_{RF}$) and the LO signal ($v_{LO}$).

$$v_G = v_{RF} + v_{LO} \quad \text{(S1)}$$

Where $v_{RF} = A_{RF}\, cos(\omega_{RF}\, t)$; $A_{RF}$ and $\omega_{RF}$ are the amplitude and frequency of RF input, respectively;

$v_{LO} = A_{LO}\, cos(\omega_{LO}\, t)$; $A_{LO}$ and $\omega_{LO}$ are the amplitude and frequency of LO input, respectively.

Substituting $v_{RF}$ and $v_{LO}$ into Equation S1 yields

$$v_G = A_{RF}\, cos(\omega_{RF}\, t) + A_{LO}\, cos(\omega_{LO}\, t) \quad \text{(S2)}$$

$MoS_2$ FET is biased in the current saturation region, where the output drain current can be approximated by a second-order series

$$I_D = a_0 + a_1 * v_G + a_2 * {v_G}^2 \quad \text{(S3)}$$

Substituting Equation S2 in Equation S3

$$I_D = a_0 + a_1(A_{RF}\, cos(\omega_{RF}\, t) + A_{LO}\, cos(\omega_{LO}\, t)) + a_2(A_{RF}\, cos(\omega_{RF}\, t) +$$

$$A_{LO}\, cos(\omega_{LO}\, t))^2 + higher\ order\ terms \quad \text{(S4)}$$

Expanding

$$I_D = a_0 + a_1 A_{RF} \cos(\omega_{RF}\, t) + a_1 A_{LO} \cos(\omega_{LO}\, t) + a_2 \frac{{A_{RF}}^2}{2}(1 + \cos(2\omega_{RF}\, t)) +$$

$$a_2 \frac{{A_{LO}}^2}{2}(1 + \cos(2\omega_{LO}\, t)) +$$

$$\boldsymbol{A_{RF} A_{LO} a_2\, (\cos((\omega_{RF} - \omega_{LO})t)} + A_{RF} A_{LO} a_2(\cos(\omega_{RF} + \omega_{LO})t) +$$

$$higher\ order\ terms \quad \text{(S5)}$$

In Equation S5 the down converted signal is shown in red. We also observe higher order frequency components at $\boldsymbol{\omega_{RF}}$, $\boldsymbol{\omega_{LO}}$ , $(\boldsymbol{\omega_{RF}} + \boldsymbol{\omega_{LO}})$, **….**These can be filtered by passing mixer output through low pass filter.

**Amplitude Modulation (AM) Receiver Analysis**

AM signal is given by

$$v_{AM} = A_C\big(1 + B * m(t)\big)\cos(\omega_C t) \quad \text{(S6)}$$

Where $A_C$ is carrier amplitude, $\omega_c$ is carrier frequency, $m(t)$ is modulating signal, $B$ is modulation index

The input gate voltage of FET in Figure 3e is given by

$$v_G = v_{AM} + v_C \quad \text{(S7)}$$

Where $v_{AM}$ is the AM signal received by the antenna (Equation S6) and $v_C$ is the local carrier signal having same frequency and phase of the carrier signal used for AM generation.

Expanding

$$v_G = A_C\big(1 + B * m(t)\big)\cos(\omega_C t) + A_C \cos(\omega_C t) \quad \text{(S8)}$$

Flexible $MoS_2$ FET is biased in the current saturation region, where similar to above analysis, the output drain current can be approximated by a second-order power series given by

$$I_d = a_0 + a_1 * v_G + a_2 * {v_G}^2 \quad \text{(S9)}$$

Substituting $v_G$ into Equation S9 yields

$$I_d = a_0 + a_1 * \{A_C\big(1 + B * m(t)\big)\cos(\omega_C t) + A_C \cos(\omega_C t)\} + a_2 * \{A_C\big(1 + B * m(t)\big)\cos(\omega_C t) + A_C \cos(\omega_C t)\}^2 \quad \text{(S10)}$$

Expanding

$$I_d = a_0 + a_1 * \{A_C\big(1 + B * m(t)\big)\cos(\omega_C t)\} + a_1 * \{A_C \cos(\omega_C t)\} + a_2 * \{A_C\big(1 + B * m(t)\big)\cos(\omega_C t)\}^2 + a_2 * \{A_C \cos(\omega_C t)\}^2 + 2 * a_2 * A_C\big(1 + B * m(t)\big)\cos(\omega_C t) * A_C \cos(\omega_C t) \quad \text{(S11)}$$

Equation S11 has frequency components at DC, $\omega_m$, $(\omega_c - \omega_m)$, $(\omega_c + \omega_m)$, $(2\omega_c - \omega_m)$, $(2\omega_c + \omega_m)$, higher order terms. Expanding Equation S11 and low pass filtering ( cutoff frequency < $\omega_c$ )

$$I_d = 2 * a_2 * {A_c}^2 * B * m(t) \quad \text{(S12)}$$

Output voltage of AM receiver

$$v_{out} = I_d * R_L$$

$$\boldsymbol{v_{out} = 2 * a_2 * {A_c}^2 * B * m(t) * R_L} \quad \text{(S13)}$$

The output of AM receiver mainly depends on modulation index $B$, carrier amplifute $A_c$, load resistance $R_L$ and device coefficient $a_2$.

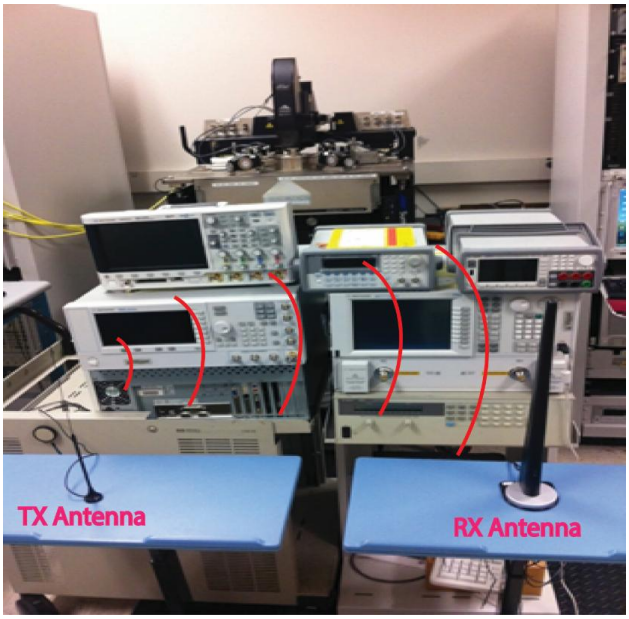


Figure S9: AM transmitter and receiver measurement setup

References

[1] A. Sanne, R. Ghosh, A. Rai, M. N. Yogeesh, S. H. Shin, A. Sharma, K. Jarvis, L. Mathew, R. Rao, D. Akinwande, S. Banerjee, Nano letters 2015.

[2] R. Kappera, D. Voiry, S. E. Yalcin, W. Jen, M. Acerce, S. Torrel, B. Branch, S. Lei, W. Chen, S. Najmaei, APL Materials 2014, 2, 092516.

[3] H. Schmidt, S. Wang, L. Chu, M. Toh, R. Kumar, W. Zhao, A. H. Castro Neto, J. Martin, S. Adam, B. Özyilmaz, Nano letters 2014, 14, 1909.

[4] H. Liu, M. Si, S. Najmaei, A. T. Neal, Y. Du, P. M. Ajayan, J. Lou, P. D. Ye, Nano letters 2013, 13, 2640.

[5] H. Wang, L. Yu, Y. Lee, W. Fang, A. Hsu, P. Herring, M. Chin, M. Dubey, L. Li, J. Kong, T. Palacios, "Large-scale 2D electronics based on single-layer MoS2 grown by chemical vapor deposition", presented at *Electron Devices Meeting (IEDM), 2012 IEEE International*, 10-13 Dec. 2012, 2012.

[6] H. Y. Chang, S. Yang, J. Lee, L. Tao, W. S. Hwang, D. Jena, N. Lu, D. Akinwande, ACS nano 2013, 7, 5446.

[7] T. Jiang, R. Huang, Y. Zhu, Advanced Functional Materials 2014, 24, 396.