A 1-V 0.25-μW Inverter Stacking Amplifier With 1.07 Noise Efficiency Factor

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***Abstract*— This paper presents a highly power-efficient amplifier. By stacking inverters and splitting the capacitor feedback network, the proposed amplifier achieves six-time current reuse, thereby significantly boosting the transconductance and lowering noise but without increasing the current consumption. A novel biasing scheme is devised to ensure robust operation under 1-V supply. A prototype in 180-nm CMOS has 5.5-μV_{rms} noise within 10-kHz BW while consuming only 0.25-μW power, leading to a noise efficiency factor of 1.07, which is the best among reported amplifiers.**

***Index Terms*— Current reuse, inverter-stacking amplifier, noise efficiency factor (NEF), power efficient, replica-based bias.**

I. Introduction

THE overall noise of a sensor read-out circuit is typically dominated by the front-end amplifier. For a given amplifier topology, there exists a fundamental tradeoff between noise and power. Thus, to suppress the noise below a certain target, it is necessary to consume a sufficiently large amount of power. In addition, the amplifier power does not decrease with technology scaling, as it is noise-limited rather than technology-limited. As a result, for low-noise sensor applications, the front-end amplifier usually takes up a significant portion of the overall system power budget [1]–[5]. Therefore, it is highly desirable to develop design techniques that can relax this tight noise and power tradeoff. Reducing amplifier power while keeping the same noise level is crucial for a wide range of power- and energy-constrained applications. For example, in the Internet-of-Things era, to ensure a long lifetime without battery replacement, the power of the amplifier in the sensor node needs to be ultralow [6], [7]. Similarly, biomedical implants have a stringent requirement on the amplifier power due to limited battery size as well as safety concerns regarding heat dissipation [8]–[11].

There have been many excellent research works in the past that aim to mitigate the amplifier noise-power tradeoff [6], [7], [12]–[16], [18], [19]. Essentially, the goal is to decrease the product of power and noise for an amplifier. Thus, for the same noise, the amplifier power can be reduced; or for the same power, the amplifier noise can be minimized. These two scenarios are directly interchangeable. The central idea is to boost the overall amplifier transconductance g_m but without increasing the bias current I_D. The classic design technique is to bias the input transistors in weak inversion to maximize their g_m/I_D [12]. To further increase g_m, a PMOS input pair can be stacked on top of an NMOS input pair to form an inverter-based input stage, so that the overall amplifier g_m is doubled but without requiring any extra bias current (it is shared by both NMOS and PMOS input pairs) [13], [14]. The challenge for the scheme of [13] is that it requires multiple power supplies and has to deal with the common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR) degradation due to its pseudo-differential input pair. The work of [14] not only achieves two-time current reuse but also operates the amplifier first-stage under a low voltage of 0.2 V, thereby further reducing the amplifier power; however, it also needs extra dc–dc converters for multiple power supplies, which increase the hardware complexity and incur additional area and power costs. The orthogonal current reuse technique of [15] boosts the level of current reuse, allowing N-time current reuse among N-channel inputs, but it has $2N$ number of output branches to combine, leading to increased complexity and power of the peripheral circuits and thus loss in the overall amplifier power efficiency. In addition, it can only be applied for applications with multi-channel inputs like neural recording. Recently, by using ac coupling and multi-chopper, the work of [16] realizes six-time current reuse for a single-channel input. It also reduces the number of current summing branches to $2^{N/2}$ by using both NMOS and PMOS pairs, but it still does not eliminate the exponential dependence. It obtained the previously best measured noise-power tradeoff, but this is achieved in open loop. When placing this amplifier in a practical closed-loop configuration to ensure an accurate gain and high linearity, its power efficiency would inevitably degrade due to intrinsically increased input-referred noise, especially considering the parasitic capacitance at the virtual ground nodes. Moreover, it needs complicated demodulation and a fourth-order filter to attenuate the ripple, which increases the overall complexity and requires additional power and area.

This paper presents a novel power-efficient amplifier. By vertically stacking N inverters, it achieves $2N$-time current reuse for a single-channel input. Unlike [15] and [16], it has only N output current branches to combine, thus, turning the prior exponential dependence into a mild linear dependence. As a result, it reduces the power of the peripheral circuits and

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boosts the overall amplifier power efficiency. The proposed amplifier fits well in a closed-loop capacitive feedback configuration. The required ac coupling to the multiple amplifier input nodes can be realized by splitting the input and feedback capacitors into multiple paths. As a result, it does not require any additional hardware which would incur extra cost in chip power and area. To minimize the requirement on the power supply voltage, the tail current sources between stacked inverters are eliminated but without sacrificing CMRR and PSRR. A replica circuit ensures that input pairs with tight coupling are robustly biased against process, voltage, and temperature (PVT) variations. Two prototype amplifiers are implemented in 180-nm CMOS process [20]. The stack-2 version achieves a measured noise efficiency factor (NEF) of 1.26 in closed loop under the supply voltage of 0.9 V. The stack-3 version achieves an NEF of 1.07 under the supply voltage of 1 V. To the best of our knowledge, this NEF is the best among all measured amplifiers so far. The second best NEF achieved by a closed-loop amplifier is 1.64, which translates to over 2.3-time more power consumption compared with the proposed amplifier assuming the same noise performance.

This paper is organized as follows. Section II reviews classic low-power design techniques and the core concept of current reuse. Section III presents the proposed inverter stacking amplifier focusing on the stack-2 configuration. Section IV presents the stack-3 version. Section V shows the detailed circuit implementation. Measurement results are shown in Section VI. The conclusion is in Section VII.

II. Concept of Noise Efficiency Factor and Current Reuse

Fig. 1(a) shows the schematic of a basic fully differential common-source amplifier. Its input-referred thermal noise power spectral density (PSD) can be calculated as

$$N_{\mathrm{PSD}} = \frac{8kT\gamma}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}\right) \tag{1}$$

where k is Boltzmann's constant, and γ is the noise model parameter. The power consumption is given by

$$P = V_{\mathrm{DD}} \cdot I_{\mathrm{tot}} \tag{2}$$

where V_{DD} denotes the supply voltage, and I_{tot} denotes the total current consumption. Thus, its power and noise product is given by

$$P \cdot N_{\mathrm{PSD}} = 8kT\gamma \cdot V_{\mathrm{DD}} \cdot \frac{I_{\mathrm{tot}}}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}\right). \tag{3}$$

To achieve a higher power efficiency and minimize this power-noise product, classic design techniques include: 1) biasing the input transistors in weak inversion to maximize g_m/I_D [12] and 2) biasing the load transistors in strong inversion to decrease its g_m/I_D and thus reducing g_{m2}/g_{m1} [21]. Sometimes if V_{DD} is tunable, people also try to lower it as much as possible to reduce power [14], [22], but there is usually restriction due to signal swing requirement and system-level consideration.

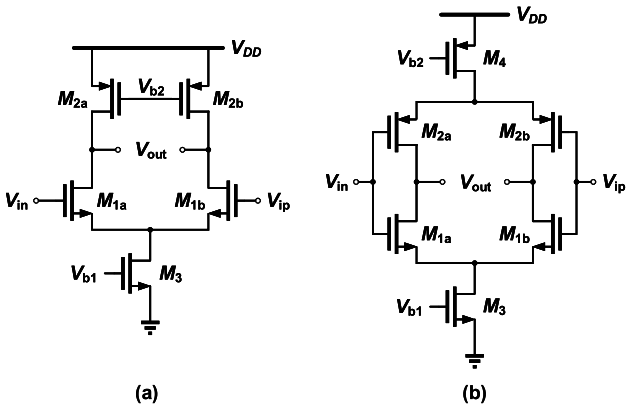

Fig. 1. (a) Fully differential common-source amplifier. (b) Inverter-based amplifier.

To characterize the power or noise efficiency of an amplifier, researchers have come up with a figure-of-merit called NEF, which is given by [23]

$$\mathrm{NEF} = v_{\mathrm{ni,rms}}\sqrt{\frac{2}{\pi}\cdot\frac{I_{\mathrm{tot}}}{V_T \cdot 4kT \cdot BW}} \tag{4}$$

where $v_{\mathrm{ni,rms}}$ is the input-referred rms noise of the amplifier in a given bandwidth BW, and V_T is the thermal voltage given by kT/q. Different from (3), the NEF of (4) is defined as a unitless ratio and easy to compare. It essentially normalizes the power and noise product of a given amplifier against that of a single bipolar transistor. NEF is usually greater than 1 for a typical MOSFET amplifier, because: 1) g_m/I_D of an MOSFET is smaller than that of a bipolar transistor; 2) an MOSFET produces much larger $1/f$ noise; and 3) a practical amplifier always has other devices that contribute noise and consume power. Assuming that the amplifier noise is dominated by thermal noise, the NEF of any differential amplifier can be simplified to

$$\mathrm{NEF} = \sqrt{4\gamma \cdot \alpha \cdot \eta \cdot \frac{q/kT}{m \cdot g_m/I_D}} \approx \sqrt{\frac{4\gamma \cdot \alpha \cdot \eta \cdot n}{m}} \tag{5}$$

where α is the noise excess factor defined as the total amplifier noise normalized against the noise from the input transistors (if $\alpha = 1$, noise from all other devices is ignored), η is the current excess factor defined as the total amplifier current divided by the current of the input transistor (if $\eta = 1$, all bias current goes through the input pair), and m is the current reuse times [$m = 1$ for a fully differential common-source amplifier of Fig. 1(a)]. In simplifying (5), we also assume input transistors are biased in the subthreshold region where $(q/kT)/(g_m/I_D)$ is equal to the subthreshold slope factor n. As a result, the theoretical lower bound of the NEF for the amplifier of Fig. 1(a) is about 2 assuming $\gamma = 0.7$, $\alpha = \eta = 1$, and $n = 1.4$. For a realistic amplifier, assuming that the input pair consumes 80% of the total current ($\eta = 1.25$) and contributes 80% of the total noise ($\alpha = 1.25$), the practical lower bound of NEF is about 2.5.

To improve the amplifier power efficiency and minimize NEF, the key idea is to boost g_m but without increasing the

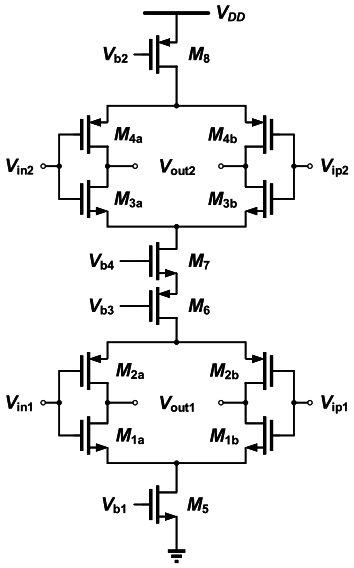

Fig. 2. Natural inverter stacking topology.

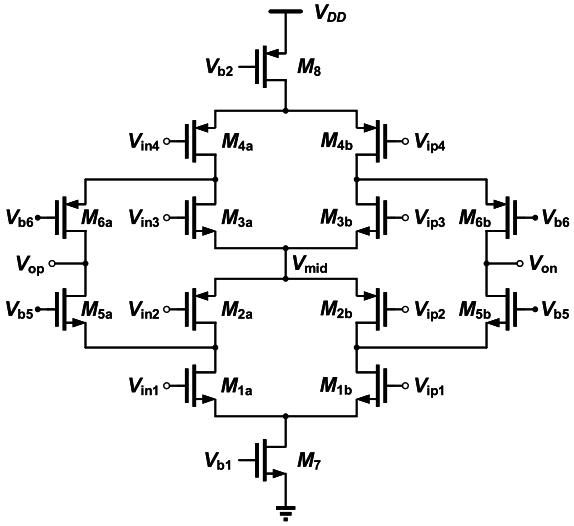

Fig. 3. Stack-2 inverter stacking amplifier schematic.

amplifier current. An effective way is through current reuse. Fig. 1(b) shows an inverter-based amplifier that reuses its bias current for both NMOS and PMOS input pairs. Assuming that both pairs have the same transconductance, the overall amplifier g_m is doubled for the same bias current, leading to 2-time reduction in noise power and 1.4-time reduction in NEF. One tradeoff of using an inverter-based amplifier is reduced output signal swing, but this can be alleviated by adding a second-stage amplifier that follows it [16]. Other tradeoffs include: 1) increased requirement on the power supply voltage; 2) increased input capacitance; and 3) reduced input CM range. However, for applications that care most about power efficiency, it is worthwhile to pay the price of these.

If we can achieve more times of current reuse (i.e., increasing m), then g_m can be further boosted and NEF can be further reduced. To calculate the practical limit, we assume $\alpha = \eta = 1.25$. Four-time and six-time current reuse would reduce the practical NEF lower bound to 1.25 and 1, respectively, indicating significant power reduction.

The direct way of achieving more times of current reuse is to vertically stack inverter-based amplifiers as shown in Fig. 2. This way, the bias current is reused four times and thus boosting g_m by four times. Nonetheless, directly stacking inverters brings several challenges. First, the required minimum power supply voltage, given by $4|V_{\rm gs}|+4|V_{\rm ds}|$, is larger than a single inverter-based amplifier of Fig. 1(b). Typically, the minimum required $|V_{\rm ds}|$ for a transistor to have a reasonably large output impedance is 100 mV. For a transistor with $|V_{\rm th}|$ of 400 mV, even if it is biased in the deep subthreshold region with an overdrive voltage of -100 mV, the corresponding $|V_{\rm gs}|$ is 300 mV, leading to a minimum power supply voltage of 1.6 V. One way to reduce the supply voltage is to use a native transistor with low $|V_{\rm th}|$ (e.g., 100 mV). However, this comes with a price. As shown in Fig. 2, it is easy to derive that $|V_{\rm gs1}| + |V_{\rm gs2}| = |V_{\rm ds1}| + |V_{\rm ds2}| \geq 200$ mV. Thus, each $|V_{\rm gs}|$ is greater than 100 mV. This means that the overdrive voltage is greater than 0 mV, leading to a limited current efficiency (g_m/I_D). Second, there is more than one input node, and thus, we need a method to couple the amplifier input to all input pairs. This method is preferred to be simple, low-noise, and low-cost. Third, there are multiple output nodes, which also call for a low-cost way to aggregate all small-signal currents. In addition, when addressing these challenges, we cannot sacrifice CMRR, PSRR, as well as PVT robustness.

III. Proposed Inverter Stacking Amplifier: Stack-2 Version

A. Core Schematic of Proposed Inverter Stacking Amplifier

The core schematic of the proposed fully differential stack-2 inverter stacking amplifier is shown in Fig. 3. Compared with the schematic of Fig. 2, there are several changes. First, the four input pairs are separated. As will be shown later, the input signal is ac coupled to all four input nodes. This way, the input pairs can be biased at different voltage levels. Second, the two current source transistors between the stacked inverters are removed. These modifications allow a significant reduction of the minimally required power supply voltage to $6V_{ov}$. Third, four common-gate transistors (M_{5a}/M_{5b} and M_{6a}/M_{6b}) are added to aggregate the small-signal currents from all input pairs.

B. Small-Signal Gain, Input-Referred Noise, Offset, CMRR, and PSRR Analyses

Let us first analyze the small-signal behavior of the proposed amplifier. It is simple to derive that the total amplifier transconductance g_{mt} is

$$g_{mt} = \frac{g_m}{I_D} \cdot (2I_D + 2I_D \cdot 0.9) \approx 4g_m \tag{6}$$

where I_D is the bias current for the input transistor. In deriving (6), we assume all input transistors have similar g_m/I_D and the intrinsic gain ($g_m r_o$) for all transistors is much greater than 1. The same assumption is made for all later derivations.

For M_2/M_3, their currents are 90% of the amplifier bias current. The remaining 10% current flows through the cascode transistors (M_5/M_6).

In differential mode (DM) operation, the node V_{mid} serves as the virtual ground, and thus the amplifier output impedance r_{ot} is given by

$$r_{ot} = (g_{m5}r_{o5}(r_{o1}//r_{o2}))//(g_{m6}r_{o6}(r_{o3}//r_{o4})) \tag{7}$$

where g_{mi} is the transconductance of transistor M_i, and r_{oi} is the small-signal output resistance of transistor M_i. Thus, we can derive the amplifier open-loop DM gain A_{DM}

$$A_{\text{DM}} \equiv g_{mt}r_{ot} \approx g_m^2 r_o^2. \tag{8}$$

This shows that its DM gain is the square of the transistor intrinsic gain, which is comparable to that of a telescopic or folded cascode amplifier. In fact, the proposed amplifier can be viewed as a hybridization of a telescopic amplifier and a folded cascode amplifier. If we only consider the lower NMOS input pair (M_{1a}/M_{1b}) and assume that all other input pairs are connected to dc biases, then its overall structure behaves the same as a telescopic amplifier. By contrast, if we only look at the lower PMOS input pair (M_{2a}/M_{2b}), its input and output relationship is identical to that of a folded cascode amplifier. The same analogy applies for the upper NMOS and PMOS pairs (M_{3a}/M_{3b} and M_{4a}/M_{4b}).

Assuming that the input transistors dominate the overall amplifier noise, the overall input-referred thermal noise can be derived as

$$N_{\text{PSD,th}} = \frac{8kT\gamma \cdot (g_{m1}+g_{m2}+g_{m3}+g_{m4})}{(g_{m1}+g_{m2}+g_{m3}+g_{m4})^2} \approx \frac{2kT\gamma}{g_m}. \tag{9}$$

Comparing with (1), it is clear that the noise PSD is reduced by four times due to g_m increase.

The input-referred $1/f$ noise PSD of the proposed amplifier can be derived as

$$N_{\text{PSD},1/f} = \frac{K_f}{C_{ox} \cdot 4WL} \cdot \frac{1}{f} \tag{10}$$

where K_f is a process-dependent parameter, W and L are the transistor width and length, respectively. In the proposed amplifier, the $1/f$ noise is suppressed by increasing the input transistor size, so that the in-band noise is dominated by the thermal noise.

The overall input-referred offset $V_{\text{os,in}}$ can be derived as

$$V_{\text{os,in}} = \frac{\sum_{i=1}^{4} g_{mi}V_{\text{osi}}}{g_{m1}+g_{m2}+g_{m3}+g_{m4}} \approx \frac{\sum_{i=1}^{4} V_{\text{osi}}}{4}. \tag{11}$$

Assuming that the offset voltages V_{osi} all have the same distribution with the standard deviation of σ_{os}, then the overall input-referred offset standard deviation $\sigma_{\text{os,in}}$ can be derived as

$$\sigma_{\text{os,in}} = \frac{\sigma_{\text{os}}}{2}. \tag{12}$$

This reduction in the input-referred offset results from the increased total input transistor size.

For CMRR calculation, we apply a CM input and derive the DM output in the presence of mismatch, as shown in Fig. 4. Based on definition [17], the CMRR can be calculated as

$$\text{CMRR} \equiv \frac{A_{\text{DM}}}{A_{\text{CM-DM}}} \approx \frac{2g_m r_o}{\frac{\Delta V_{\text{th}}}{nkT/q}} \tag{13}$$

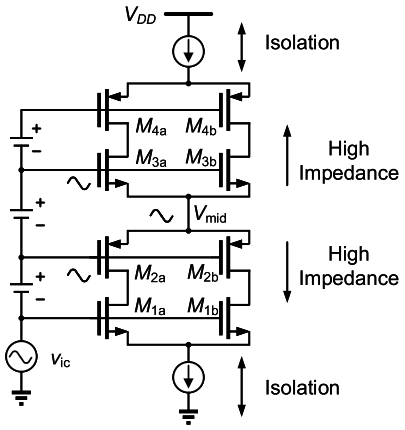

Fig. 4. CM circuit analysis.

where $A_{\text{CM-DM}}$ denotes the CM-to-DM gain. To simplify (13), we have assumed that all transistors have the same g_m and r_o, and the threshold voltage mismatch ΔV_{th} between different input pairs has the same distribution. The result of (13) is comparable to that of a telescopic amplifier, indicating that stacking inverters but without current source isolation of Fig. 2 does not degrade CMRR. This result may seem counterintuitive. The node V_{mid} is a low-impedance node with all source connections. At first glance, this would lead to large CM voltage gains for the upper NMOS (M_{3a}/M_{3b}) and lower PMOS (M_{2a}/M_{2b}) input pairs. However, a careful examination shows that V_{mid} tracks the input CM voltage variation. Thus, from CM analysis point of view, V_{mid} is effectively ac short with the CM input, creating a large output resistance (either looking up or looking down at V_{mid}) that degenerates both middle input pairs. Similarly, PSRR can be derived in the same way as CMRR, and the result is given by

$$\text{PSRR} \equiv \frac{A_{\text{DM}}}{A_{V_{\text{DD}}-\text{DM}}} \approx \frac{2g_m r_o}{\frac{\Delta V_{\text{th}}}{nkT/q}} \tag{14}$$

where $A_{V_{\text{DD}}-\text{DM}}$ denotes the voltage gain from V_{DD} to the differential output. This result is also comparable to that of a telescopic amplifier.

C. Bias Voltage Generation

To minimize the supply-voltage requirement, the dc bias voltages for all four input pairs in Fig. 3 are different. The lower NMOS (M_{1a}/M_{1b}) and upper PMOS (M_{4a}/M_{4b}) pairs are relatively simple to bias, as a small deviation from ideal bias voltage has minimal influence on the overall amplifier operation. Nevertheless, with the removal of middle current sources (M_6 and M_7) in Fig. 2, the bias voltages for the lower PMOS (M_{2a}/M_{2b}) and upper NMOS (M_{3a}/M_{3b}) need to be generated very carefully, because their difference directly sets ($|V_{\text{gs2}}| + |V_{\text{gs3}}|$) and the bias current. In order to ensure the PVT robustness, a replica-based bias circuit is developed as shown in Fig. 5. It ensures that M_2 and M_3 are biased at the target current level with the right gate voltages. A negative feedback loop also ensures that V_{mid} stays at the intended voltage $V_{\text{ref}} = V_{\text{DD}}/2$. The replica-based bias branch and common-mode feedback (CMFB) circuit are given in Fig. 6.

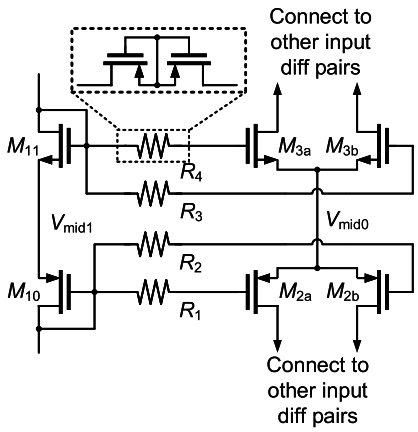

Fig. 5. Replica-based bias circuit.

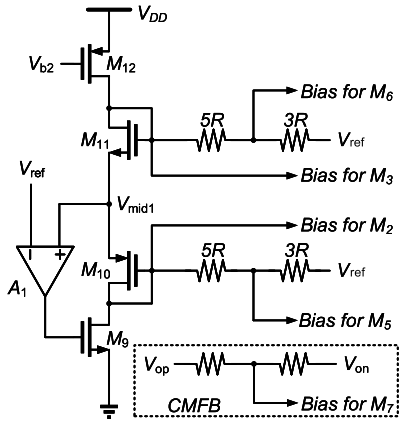

Fig. 6. Bias branch and the CMFB circuit.

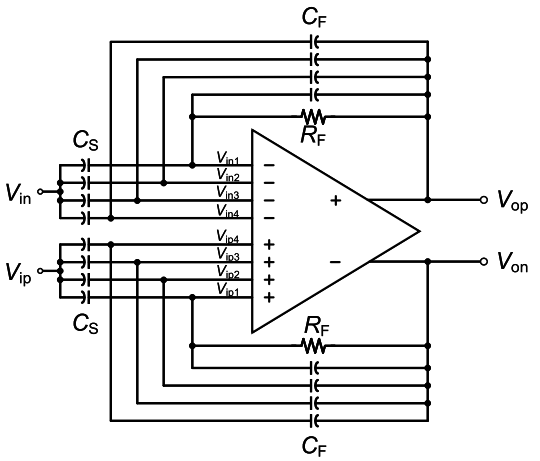

Fig. 7. Block diagram of the closed-loop amplifier with split capacitor feedback.

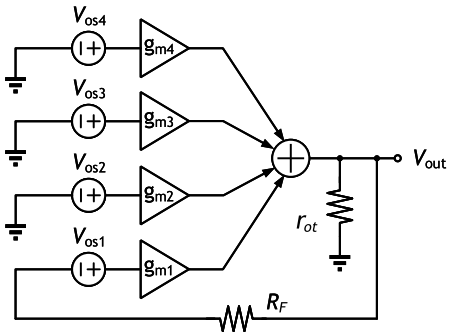

Fig. 8. Offset averaging model.

M_{10} is used to bias the PMOS (M_{2a} and M_{2b}) in the bottom inverter, and M_{11} is used to bias the NMOS (M_{3a} and M_{3b}) on the top inverter. M_5 and M_6 are cascode transistors, which provide low-impedance nodes at the drain side of M_1/M_2 and M_3/M_4. Thus, the mismatch-induced current difference between the bias (M_{10} and M_{11}) and input transistors (M_2 and M_3) will flow into the common gate transistors. 10% of the amplifier bias current is allocated to the common gate (cascode) transistors (M_{5a}/M_{5b} and M_{6a}/M_{6b}). Resistor dividers are used to generate voltages to bias the cascode transistors. The bias voltages are copied to the main amplifier using pseudo-resistors that achieve high resistance with a small chip area [24]. CM feedback is also implemented with a pseudo-resistor-based voltage averager.

D. Closed-Loop Configuration With Split Capacitor Feedback

Fig. 7 shows the block diagram of the capacitive-feedback amplifier using the proposed inverter stacking amplifier of Fig. 3. The required ac coupling can be realized by splitting the input and feedback capacitors into four pieces [13]. Although there are multiple feedback paths, the overall behavior of this amplifier is the same as a classic capacitive-feedback amplifier whose closed-loop gain $A_{\rm cl}$ is set by the capacitor ratio

$$A_{\rm cl} \approx \frac{C_S}{C_F}. \tag{15}$$

A feedback pseudo-resistor R_F connects the output with the input pair M_{1a}/M_{1b}. This dc feedback greatly reduces the output-referred offset, which would saturate the amplifier if not addressed. Note that although this feedback is formed at only one input pair, it addresses the offsets from all input pairs. Using the model of Fig. 8, we can derive the overall output-referred offset $V_{\rm os,out}$ in (16) and its standard deviation $\sigma_{\rm os,out}$ in (17)

$$V_{\rm os,out} = \frac{\sum_{i=1}^{4} g_{mi} V_{\rm osi}}{g_{m1}} \tag{16}$$

$$\sigma_{\rm os,out} = 2 \cdot \sigma_{\rm os}. \tag{17}$$

Compared with (12), (17) shows that the closed-loop output-referred offset $\sigma_{\rm os,out}$ is only four times of the open-loop input-referred offset $\sigma_{\rm os,in}$. This shows that the amplifier output would not be saturated by the offset. In such a multi-input closed-loop amplifier configuration, one path of dc feedback loop is sufficient to prevent the output from saturation. An additional benefit of having this resistor feedback is that it removes the need to generate a separate dc bias for M_{1a}/M_{1b}.

To analyze the total noise, let us examine the block diagram shown in Fig. 9, where $C_{\rm PS}$, $C_{\rm PF}$, and $C_{\rm POTA}$ represent the parasitic capacitance of C_S, C_F, and the OTA input capacitance, respectively. We can derive the overall

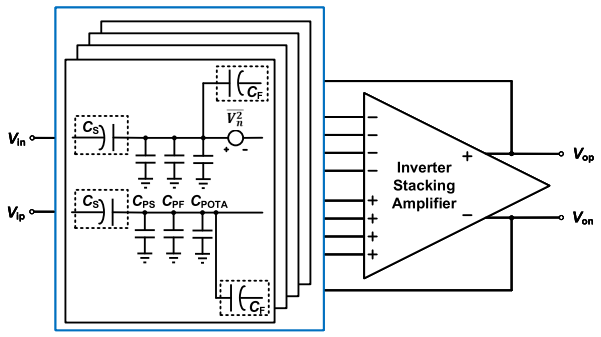

Fig. 9. Block diagram of the proposed closed-loop amplifier with parasitic capacitors.

input-referred noise PSD of the closed-loop amplifier

$$N_{\text{PSD}} \approx \frac{2kT\gamma}{g_m} \cdot \left(1 + \frac{1}{|A_{\text{cl}}|}\right)^2 \left(1 + \frac{C_P}{C_S + C_F}\right)^2 \quad (18)$$

where $C_P = C_{\text{PS}} + C_{\text{PF}} + C_{\text{POTA}}$. Comparing (9) and (18), it is clear that the input-referred noise naturally degrades going from open loop to closed loop, which is a common phenomenon in any closed-loop amplifier [25]. To minimize the degradation, it is preferred to enlarge the closed-loop gain A_{cl} and minimize the parasitic capacitance C_P. For example, for a closed-loop amplifier with a gain of 20 and 20% parasitic capacitance, the PSD is increased by 50%, leading to an enlarged NEF by 23%.

E. Limitations and Mitigations

There are several limitations of the proposed amplifier. First, as it stacks six transistors vertically, the minimum power supply voltage is $6|V_{\text{ds}}|$. Although it is higher than that for a telescopic amplifier by $|V_{\text{ds}}|$, it achieves four-time current reuse, which is a price worth to pay especially when power efficiency is the most critical consideration. Second, the output signal swing is reduced. For example, with a 1-V power supply and $|V_{\text{ds}}|$ of 100 mV, the output swing is 400 mV. It can be used as a sensor front-end amplifier as this paper intends, but it may not be suitable for applications that desire nearly rail-to-rail output swings. To increase the output swing, we can cascade the proposed amplifier with a second-stage amplifier, like a two-stage amplifier that employs a telescopic amplifier followed by a common-source stage [14], [16], [26]. Third, the proposed amplifier requires input ac coupling, and thus, as it stands, cannot be used for dc signal amplification. To address this concern, we can use chopping to up modulate the input dc signal to the chopping frequency and enable its amplification [26]. Applying chopping can also suppress the $1/f$ noise. In this paper, the $1/f$ noise is attenuated by sizing up the input transistors; however, as shown in (18), doing so comes with the cost of increased thermal noise.

IV. Proposed Inverter Stacking Amplifier: Stack-3 Version

The proposed amplifier can be generalized to the stack-3 version as shown in Fig. 10. Three inverter-based input stages

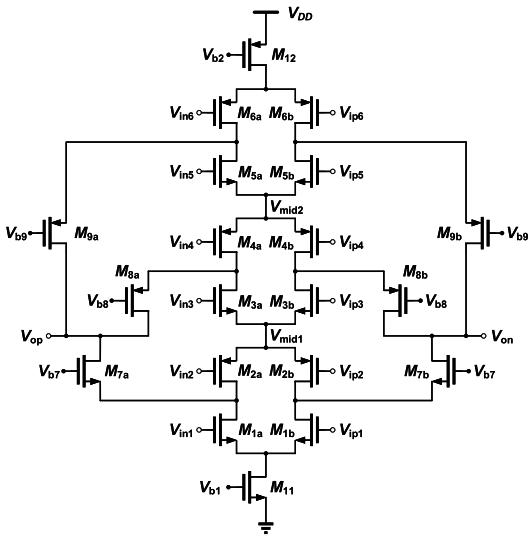

Fig. 10. Stack-3 inverter stacking amplifier schematic.

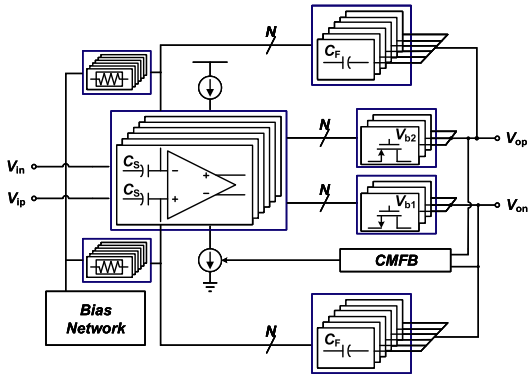

Fig. 11. Block diagram of stack-N inverter stacking amplifier.

are stacked vertically and share the same bias current. Three common-gate branches are used to aggregate the signal-signal current from all six input pairs. Therefore, the overall transconductance of this amplifier is $6g_m$. This topology can be further expanded out to stack-N version. The general approach of embedding the proposed inverter stacking amplifier inside a capacitive feedback loop is shown in Fig. 11. Similar to Fig. 7, capacitors C_S and C_F are split up and reused as ac coupling capacitors. For the open-loop and closed-loop small-signal gain, noise, offset, CMRR, and PSRR, they can be derived following the same method as explained in Section III. For brevity, we leave them out here.

Compared with the stack-2 version, the merit of the stack-3 version is increased g_m, leading to a better NEF. However, the price is increased requirement on the power supply voltage ($8|V_{\text{ds}}|$) and reduced output signal swing. The complexity of the bias and output current summation circuits also increase, leading to increased power consumption of the peripheral circuits. Thus, the benefit of stacking more layers of inverters diminishes as the number of layers increases. For practical applications, the optimum stacking number is likely to be either 2 or 3.

TABLE I
DEVICES GEOMETRY OF STACK-2 AMPLIFIER

Device	$W/L(\mu m)$	Device	$W/L(\mu m)$
M_{1a}/M_{1b}	23/5	M_{5a}/M_{5b}	1.9/4
M_{2a}/M_{2b}	11/4	M_{6a}/M_{6b}	0.6/4
M_{3a}/M_{3b}	40/4	M_7	14/4
M_{4a}/M_{4b}	10/4	M_8	10/4

TABLE II
DEVICES GEOMETRY OF STACK-3 AMPLIFIER

Device	$W/L(\mu m)$	Device	$W/L(\mu m)$
M_{1a}/M_{1b}	12/5	M_{6a}/M_{6b}	10/4
M_{2a}/M_{2b}	12/4	M_{7a}/M_{7b}	6/0.8
M_{3a}/M_{3b}	36/4	M_{8a}/M_{8b}	1/4
M_{4a}/M_{4b}	11/5	M_{9a}/M_{9b}	2/4
M_{5a}/M_{5b}	50/4	M_{10a}/M_{105b}	1/4

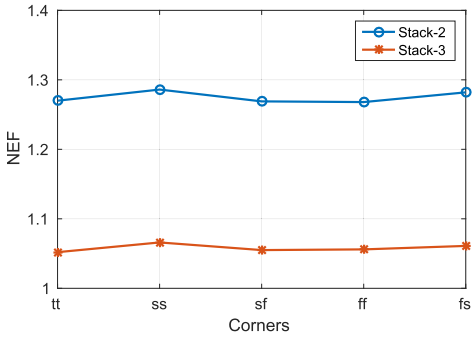

Fig. 12. Simulated NEF across corners.

V. CIRCUIT IMPLEMENTATION

Both the proposed stack-2 and stack-3 amplifiers are implemented in the 180-nm CMOS process. The intended application is action potential recording with the signal bandwidth from 250 Hz to 10 kHz and the signal amplitude up to 1 mV [19]. The dimension of the transistors in the amplifier cores is summarized in Tables I and II. Large transistor widths and lengths are chosen to boost the transistor intrinsic gain, reduce the offset, as well as suppress the $1/f$ noise corner to be below 250 Hz. All transistors operate in thje subthreshold region to boost the current efficiency g_m/I_D. The current of the amplifier core is 220 nA. The common-gate transistors used for current summation are biased at 20 nA. The output CM is set to $V_{DD}/2$ using the classic resistor-averaging CM feedback circuit.

The open-loop gain of the amplifier is designed to be 76 dB. C_S and C_F are chosen to be 8 pF and 400 fF, respectively, leading to the nominal closed-loop gain of 26 dB. The SPICE simulated closed-loop NEF for the stack-2 and stack-3 versions are 1.26 and 1.07, respectively. Fig. 12 shows the simulated NEF across different process corners. This consistent result is enabled by the robust replica-based bias circuit of Fig. 5.

The simulated CMRR distribution among 1500 Monte Carlo simulations is shown in Fig. 13. The CMRR is higher than 81 dB assuming the yield of 90%. Fig. 14 shows the simulated PSRR distribution. The PSRR is higher than 81 dB assuming the yield of 90%. Both CMRR and PSRR simulation results match the analytical results of (13) and (14).

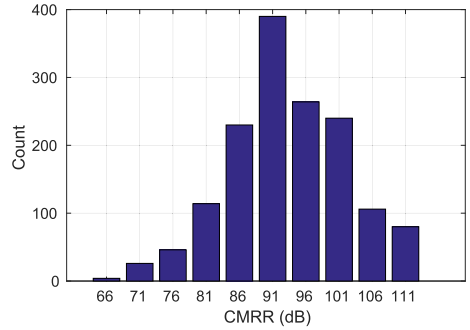

Fig. 13. CMRR distribution among 1500 Monte Carlo simulations.

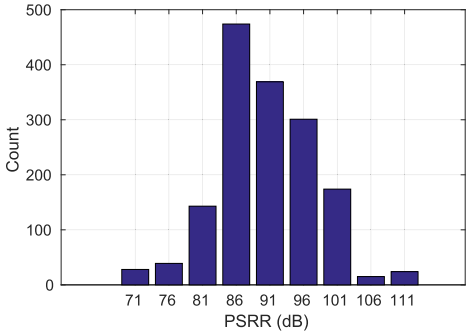

Fig. 14. PSRR distribution among 1500 Monte Carlo simulations.

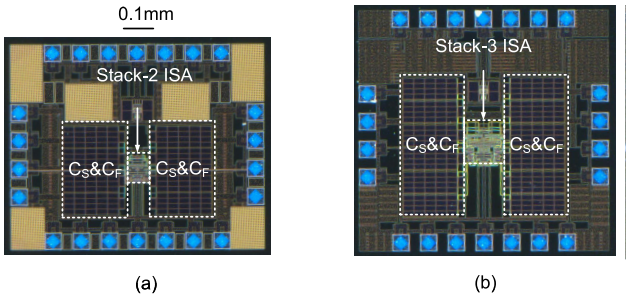

Fig. 15. Die photograph of (a) stack-2 and (b) stack-3.

The capacitors C_S and C_F are implemented using MoM capacitors. As shown in Fig. 9 and analyzed in (18), their parasitic capacitances facing the amplifier virtual ground node degrade the noise performance. To minimize this parasitic capacitance, a polysilicon layer is inserted below the MoM capacitor. It connects with the capacitor side that faces away from the virtual ground. Although the parasitic capacitance from this plate to the substrate increases, it significantly reduces the parasitic capacitance of the other virtual-ground connecting plate by isolating it from the substrate. Parasitic extraction results show that this layout technique reduces the parasitic capacitance by 50% and improves the NEF by 17%.

VI. MEASUREMENT RESULTS

The die photographs of the prototype amplifiers are shown Fig. 15. The amplifier core areas for stack-2 and stack-3

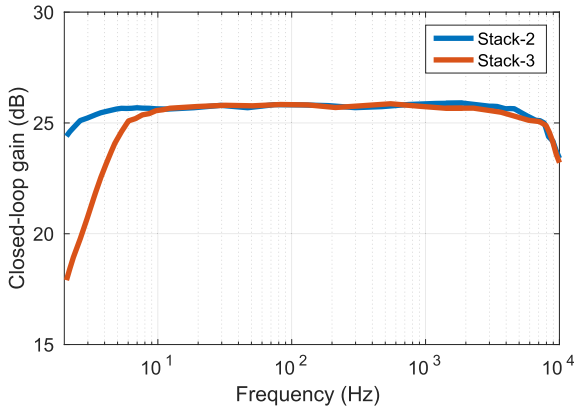

Fig. 16. Measured ac transfer of amplifier.

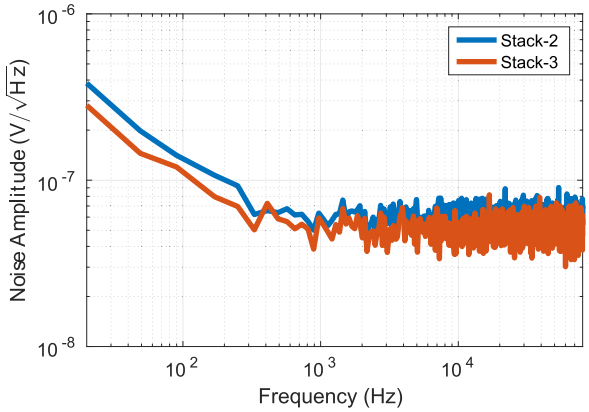

Fig. 17. Measured amplifier input-referred noise PSD.

versions are 0.01 and 0.02 mm^2, respectively. The total closed-loop amplifier areas for stack-2 and stack-3 versions are 0.22 and 0.29 mm^2, respectively, mainly dominated by capacitors.

The supply voltage for the stack-2 and stack-3 versions is 0.9 and 1.0 V, respectively. Their measured power consumptions are 226 and 246 nW, respectively. Their measured frequency responses are shown in Fig. 16. The flat-band gains are 25.4 and 25.6 dB, respectively, over the frequency range of 4 Hz to 10 kHz. Fig. 17 plots the measured input-referred noise. The 1/f noise corner is about 300 Hz. The total integrated rms input-referred noise over the signal bandwidth (250 Hz to 10 kHz) is 6.7 and 5.6 μV, respectively. These results translate to the NEF of 1.26 and 1.07 for the stack-2 and stack-3 versions. The measured closed-loop CMRR and PSRR are 82 and 81 dB for the stack-2 version and 84 and 76 dB for the stack-3 version.

Fig. 18 shows the measured NEF over the temperature range from 0 to 60 °C for both stack-2 and stack-3 prototypes. The NEF variations are within 15%. Figs. 19 and 20 show the measured NEF at different supply voltages for stack-2 and stack-3 versions, respectively. Both achieve consistent NEF results. For the stack-2 version, the measured NEF maintains at 1.26 for supply voltage beyond 0.9 V; while for the stack-3 version, the NEF maintains at 1.07 for supply voltage beyond 1 V.

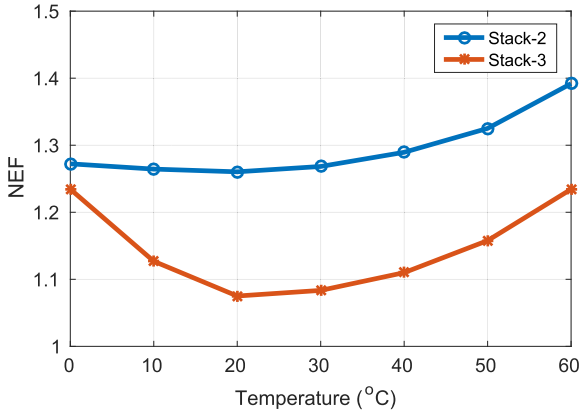

Fig. 18. Measured NEF versus temperature.

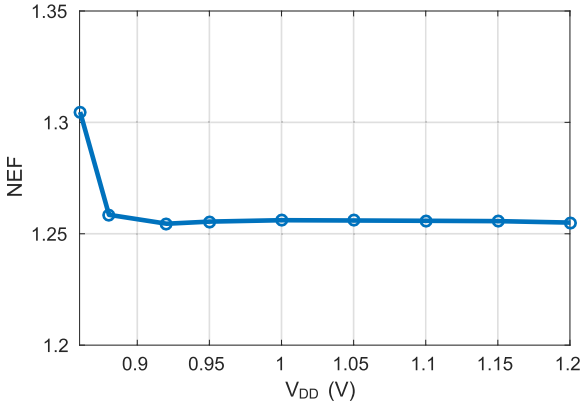

Fig. 19. Measured NEF of the stack-2 amplifier versus power supply.

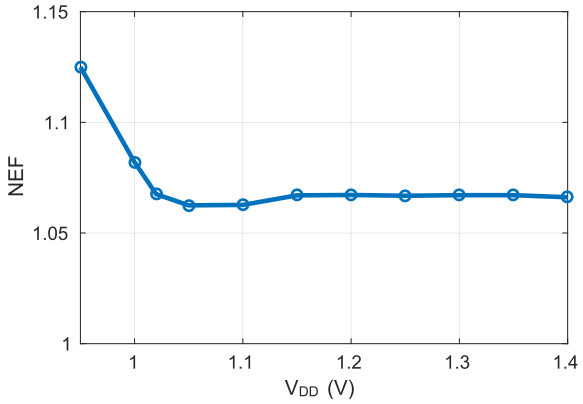

Fig. 20. Measured NEF of the stack-3 amplifier versus power supply.

Table III summarizes the performance of the prototype amplifiers and compares them with latest closed-loop amplifier works with comparable specifications. To emphasize the power efficiency of the proposed amplifier, Fig. 21 plots the reported measured NEF results of latest amplifiers. The dotted lines indicate the equivalent NEF value. It can be seen that the proposed work establishes a new tradeoff between the noise and power and pushes the NEF boundary to a new level.

TABLE III
PERFORMANCE COMPARISON

	This work		[3]	[13]	[14]	[15]	[21]	[27]	[28]
	Stack-2	**Stack-3**							
Technology (nm)	**180**	**180**	130	180	180	130	65	130	500
Gain (dB)	**25.4**	**25.6**	40	33	57.8	40	71	68	41
CMRR (dB)	**82**	**84**	75	>70	85	78	95	60	66
PSRR (dB)	**81**	**76**	80	>70	80	80	80	70	75
V_{DD} (V)	**0.9**	**1**	1	0.6	0.2/0.8	1.5	0.5	1.2	2.8
Power (μW)	**0.23**	**0.25**	12.1	1.17	0.79	3.9	5	49	7.6
BW (Hz)	**10k**	**10k**	10k	182	670	19.9k	10k	10k	5.3k
IRN (μV_{rms})	**6.7**	**5.5**	2.2	3.7	0.34	0.94	5	6.36	3.06
NEF	**1.26**	**1.07**	2.9	1.74	2.1	1.67	6	3.8	2.67

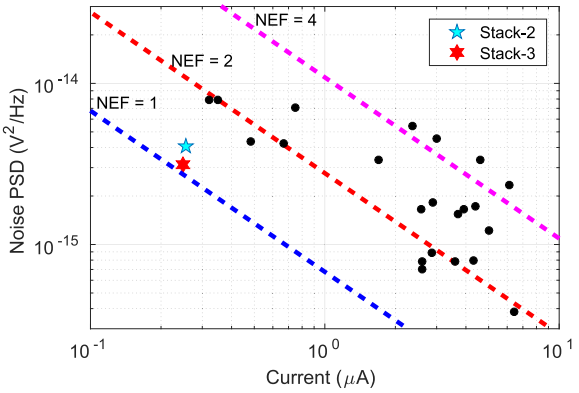

Fig. 21. Closed-loop amplifier NEF survey.

VII. CONCLUSION

This paper presented a novel power-efficient inverter-stacking amplifier. It achieves six-time current reuse under 1-V supply and obtains the best NEF among all reported amplifiers to the best of our knowledge. By splitting feedback capacitors, the required input ac coupling is realized without extra hardware cost. A simple replica-based biasing circuit is devised that ensures the robust operation across PVT variations. It is well suited to be used as the front-end amplifier for various applications that have stringent power or energy requirement, such as biomedical implants and wireless sensors.

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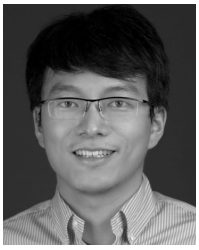

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