A 0.025-mm^2 0.8-V 78.5-dB SNDR VCO-Based Sensor Readout Circuit in a Hybrid PLL-ΔΣM Structure

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***Abstract*— This article presents a capacitively coupled voltage-controlled oscillator (VCO)-based sensor readout featuring a hybrid phase-locked loop (PLL)-ΔΣ modulator structure. It leverages phase-locking and phase-frequency detector (PFD) array to concurrently perform quantization and dynamic element matching (DEM), much-reducing hardware/power compared with the existing VCO-based readouts' counting scheme. A low-cost in-cell data-weighted averaging (DWA) scheme is presented to enable a highly linear tri-level digital-to-analog converter (DAC). Fabricated in 40-nm CMOS, the prototype readout achieves 78-dB SNDR in 10-kHz bandwidth, consuming 4.68 μW and 0.025-mm^2 active area. With 172-dB Schreier figure of merit, its efficiency advances the state-of-the-art VCO-based readouts by 50×.**

***Index Terms*— Analog-to-digital converter (ADC), continuous-time ΔΣ modulator (CTΔΣM), phase-frequency detector (PFD), phase-locked loop (PLL), sensor readout, voltage-controlled oscillator (VCO), VCO-based ADC.**

I. Introduction

With the booming trend of Internet-of-Things (IoT) and the growing focus on medical healthcare, the need for miniaturized sensors and readout circuits have been boosted to reach a whole new level. Specifically, high-performance sensor readouts have been one of the key focuses for the circuit design society in recent years. With the huge amount of sensors and their readouts to be integrated into a miniaturized form and deployed wirelessly, area and power have become more and more critical along with the conventional performance requirements for sensor readouts, such as noise and dynamic range (DR).

Manuscript received June 30, 2019; revised September 27, 2019 and November 14, 2019; accepted December 2, 2019. Date of publication December 30, 2019; date of current version February 25, 2020. This article was approved by Guest Editor Qun Jane Gu. This work was supported by NSF under Grant 1704758. *(Corresponding author: Wenda Zhao.)*

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Digital Object Identifier 10.1109/JSSC.2019.2959479

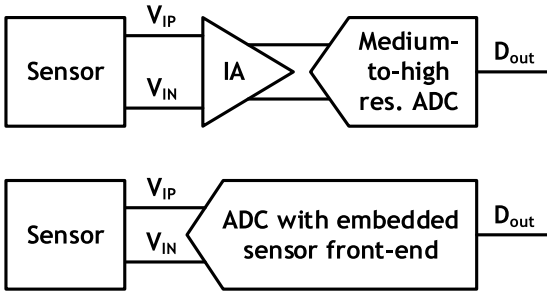

Fig. 1. Conceptual block diagram of the conventional IA + ADC sensor readout architecture (top) and direct digitizing readout architecture with a sensor front-end embedded ADC (bottom).

Existing sensor readout circuits can be broadly categorized into two general architectures: 1) classic instrumentation amplifier (IA) + analog-to-digital converter (ADC) architecture and 2) ADC direct digitizing architecture. The conceptual block diagram of the two architectures is shown in Fig. 1.

IA + ADC has been the predominant architecture for the last 10–20 years. In earlier designs, high-gain IAs (∼40–60 dB) were used so that medium-resolution ADCs with lower design complexity can be used for converting sensor output signals that typically have a small range [1]–[4]. Although many efforts have been devoted to improving the performance and power efficiency of the IA which is the critical component of the system [5]–[8], due to the high-gain IA easily saturating the system, the applications of this approach are limited to those of which have no presence of large artifacts (e.g., temperature sensing). To address the concern of limited DR and support for applications in which large artifacts may exist, such as closed-loop neural stimulation/recording and wearable sensors, recent designs propose using moderate/low-gain IAs with high-resolution ADCs, where the ADCs are typical ΔΣMs [9]–[11]. Yet, despite a better DR and lower IA complexity, the ADCs are now required to have very low noise as well. Thus, the designs taking this approach typically have high power consumption to ensure low noise on both the IA and the ADC. Moreover, they hardly benefit from process scaling due to their analog-intense nature.

As emerging IoT and biomedical applications further tightening area and power budgets, direct-digitizing sensor

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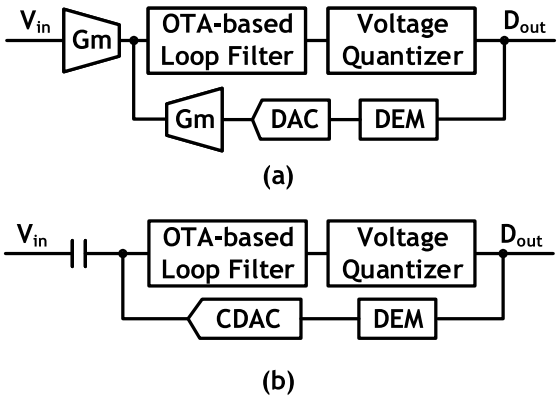

Fig. 2. Block diagram of two voltage-domain direct-digitizing readout architectures. (a) CF-CT$\Delta\Sigma$M. (b) Capacitively coupled CT$\Delta\Sigma$M.

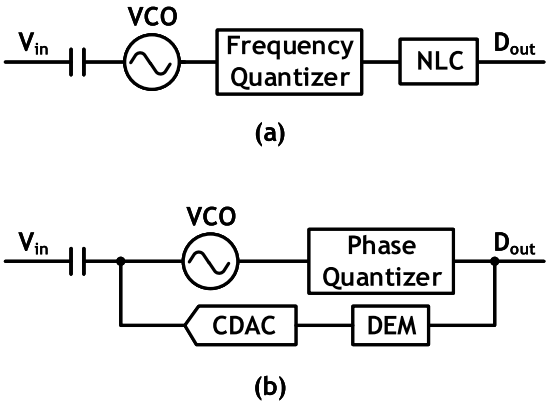

Fig. 3. Block diagram of two approaches of VCO-based sensor readout. (a) Frequency-based quantization. (b) Phase-based quantization.

readouts have drawn rising interests for their potential area efficiency improvements while achieving a high DR. Direct-digitizing sensor readouts are widely designed in modified forms of a continuous-time $\Delta\Sigma$ modulator (CT$\Delta\Sigma$M), where the IA in the classic architecture can be viewed as being embedded in the loop of the CT$\Delta\Sigma$M as the first stage. The sample-less front-end and typical high DR of the CT$\Delta\Sigma$M framework suits well for sensor readout. Fig. 2 shows two commonly used direct digitizing readout architectures: 1) CT$\Delta\Sigma$Ms with current-feedback (CF) first stage [12]–[15] and 2) CT$\Delta\Sigma$Ms featuring capacitive-coupling (CC) and Gm-C integrators [16], [17]. CF-CT$\Delta\Sigma$M provides high input impedance and common-mode rejection ratio (CMRR), but it suffers from large non-linearity because the input is directly connected to the gate of a Gm stage. CC-CT$\Delta\Sigma$M demonstrate improved noise, wider input CM range, better linearity, and gain accuracy. However, it has a lower input impedance since chopping is applied to a much larger input capacitance.

Overall, while direct-digitizing readout leveraging voltage-domain CT$\Sigma\Delta$Ms achieves high DR with a smaller area, the power-area-performance tradeoff still exists for two main reasons.

1) Voltage-domain loop filters are still analog-intense building blocks which are hard to operate under low-supply voltage with stringent requirements on noise, linearity, input/output signal swing, and so on.
2) For applications requiring high-linearity, such as temperature sensing, accelerometer, or precision MEMS microphones, explicit dynamic element matching (DEM) block is needed to guarantee multi-bit digital-to-analog converter (DAC) linearity, leading to considerable power and hardware overhead.

Recently, phase-/time-domain analog processing techniques attract increasing attention [18]–[21]. One notable example of this framework is the use of ring voltage-controlled oscillators (VCOs) as loop filter and quantizer in the phase domain.

The key concept of the VCO-based framework is to translate the amplitude-coded information into the frequency/phase domains, such that part of the information processing and quantization can take place in the frequency/phase domain decoupled from voltage amplitude. This translation makes the VCO-based framework to be more robust against process scaling effects, such as supply voltage reduction. Moreover, the phase integration not being limited by voltage swing naturally bestows the VCO integrator infinite dc gain. The multi-stage ring-VCO provides intrinsic multi-level quantization without needing multi-level reference voltage generation. Its digital-alike output allows more processing in the digital domain, which can greatly benefit from process scaling. With these benefits, the VCO-based structure exhibits the great potential to leverage technology scaling to further improve the area and power efficiency of direct-digitizing readouts.

As shown in Fig. 3, the existing VCO-based sensor readout can be categorized into two main approaches according to the way of processing information: 1) frequency-based quantization and 2) phase-based quantization.

The frequency-based quantization scheme typically utilizes the VCO as a voltage-to-frequency translator, and the digital output is generated by mapping the VCO output frequency to a range of digital codes. Thus, the implementations typically have an open-loop architecture, which is inherently stable [19], [20] but allows the VCO directly seeing the full-swing input signal. Since the VCO tuning gain is non-linear and process–voltage–temperature (PVT) sensitive, frequency-based sensor readout implementations typically require complicated non-linearity correction (NLC) and tuning to function reliably. Yet, the linearity achieved is still limited to −71-dB total harmonic distortion (THD) for 8-mV peak-to-peak (mVpp) input swing [19], and 79-dB spurious-free DR (SFDR) for 100-mVpp input swing with NLC [20].

On the other hand, in the phase-based quantization scheme, VCO can be viewed as a voltage-to-phase integrator and, thus, can be used as a loop filter in a $\Delta\Sigma$M [21]. With the VCO placed in a closed-loop, the VCO non-linearity and PVT sensitivity can be greatly suppressed. The inherently ideal frequency-phase integration of the VCO integrator provides infinite dc gain, which facilitates strong noise shaping and benefits high DR design. However, the counter-based quantization scheme applied in the majority of existing VCO-based readouts is not efficient enough when using the VCO phase information (more in Section II-A). In addition, in a closed-loop $\Delta\Sigma$M with multi-bit quantizer, the linearization

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of a multi-bit feedback DAC may require excess DEM block which may not only bring extra complexity and power/area overhead but also bring excess delay that might affect system stability.

Although the VCO-based concept shows attractive potential, existing VCO-based sensor readouts have yet to fully demonstrate it. In practical designs, special considerations are needed in VCO-based readouts to address the poor VCO linearity and PVT robustness, and inefficient frequency/phase quantization schemes [19]–[21]. To the best of our knowledge, existing works on VCO-based sensor readout have yet to simultaneously realize high resolution [>12.5 effective number of bits (ENOB)], small area (<0.05 mm^2), and low power efficiency factor (PEF) (<10).

In this article, we present a closed-loop CC-VCO-based sensor readout featuring a hybrid phase-locked loop (PLL)-$\Delta\Sigma$M structure to maximize the merits of VCO quantizer.

1) A hardware-efficient phase-frequency detector (PFD) array-based phase quantizer is proposed to directly extract the magnitude and polarity of the phase difference of the dual VCO, addressing the inefficient VCO phase information usage issue in the prior counting scheme [19]–[21].
2) The PFD array outputs directly facilitate tri-level DAC control with intrinsic clocked averaging (CLA), further obviating the high cost for the classic barrel-shifter in closed-loop direct-digitizing sensor readout.
3) A low-cost in-cell DEM scheme is proposed to guarantee linearity of the tri-level capacitive-DAC (CDAC) without requiring an accurate mid-level reference voltage (V_{REFCM}).

In addition, this article also implements a four-time expandable input range with little extra hardware. It allows the readout to embed the function of a variable gain amplifier (VGA), bringing the flexibility of multi-usage and artifact tolerance. The prototype chip fabricated in 40-nm CMOS measured a 78.5-dB SNDR with a 100-mVpp input range and 10-kHz bandwidth (BW) while consuming 4.68 μW. With a 36-nV/$\sqrt{\text{Hz}}$ input-referred noise (IRN) power spectral density (PSD), the PEF is calculated to be 8.9, which shows ten-time improvement comparing with the state-of-the-art [10] that achieves similar SNDR. Since the proposed system can also be viewed as a VCO-based $\Delta\Sigma$ ADC refined for sensor readout, we also borrow the Schreier figure of merit (FoM_S) [22] to provide another view of its power efficiency. A FoM_S of 172 dB is achieved by the proposed system, demonstrating 50× efficiency improvement over prior VCO-based sensor readouts [19]–[21].

This article is an extension of a previous work reported in [23] and is organized as follows. Section II reviews the prior counting scheme and then describes the architecture of the proposed VCO-based sensor readout using a hybrid PLL-$\Delta\Sigma$M structure. Circuit implementation is discussed in Section III. Section IV presents the measurement results and comparison. The conclusion is drawn in Section V.

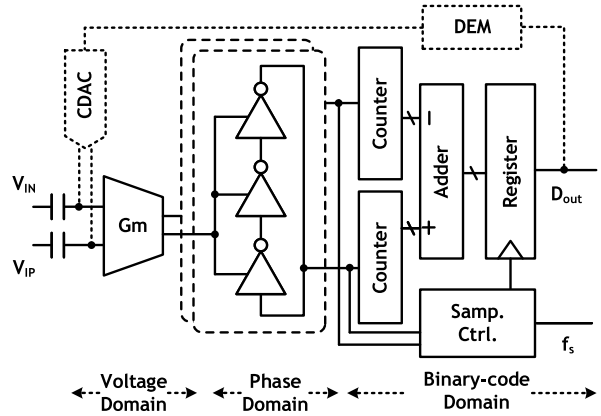

Fig. 4. Conceptual block diagram of VCO-based readouts using counting scheme.

II. Proposed Hybrid PLL-$\Delta\Sigma$M VCO-Based Sensor Readout Architecture

A. Review of the Counting Scheme in VCO-Based Readout

As mentioned earlier, the majority of existing VCO-based readouts share a common limitation of employing a counting scheme for the frequency/phase quantizer, as shown in Fig 4. This scheme digitizes the frequency/phase of the VCO by counting its edges. Despite the concept is straightforward, it is sub-optimum in terms of complexity and power. First, it requires the VCOs to run at a very high frequency (multiples of the system rate) in order to get a good resolution. This necessitates not only large bias current for the VCOs but also fast counters and adders, which makes it challenging to use a low supply. Furthermore, since the counters and adders run asynchronously to the sampling clock, a dedicated sampling control is required to avoid sampling the counter/adder's metastable region [24]. For instance, the sampler implements a triple-sampled voting method in [20], and a handshaking method is reported by [21]. These concerns are further stressed in phase-based closed-loop designs due to the loop delay consideration.

From an information processing point of view, the counting scheme only utilizes phase as a medium for binary-code conversion and place most of the processing in the binary-code domain. In fact, the VCO phase also provides useful information, such as pulsewidth and delay, which can enable a more efficient quantizer but is forfeited during counting.

B. Overview of the Proposed System

To effectively utilize phase information, we naturally turned to a classic phase information processing block, the PLL, to seek for notions that can be transferred to VCO-based sensor readout design. The block diagram of a conventional PLL is shown in the bottom left of Fig. 5(a). As shown in the diagram, to lock the output phase (Φ_{OUT}) with respect to a stable phase/frequency reference (Φ_{REF}), Φ_{OUT} first goes through a frequency divider to generate an intermediate signal (Φ_{DIV}) that has the phase information of Φ_{OUT} while having a frequency close to Φ_{REF}. Then, PFD takes in Φ_{REF} and

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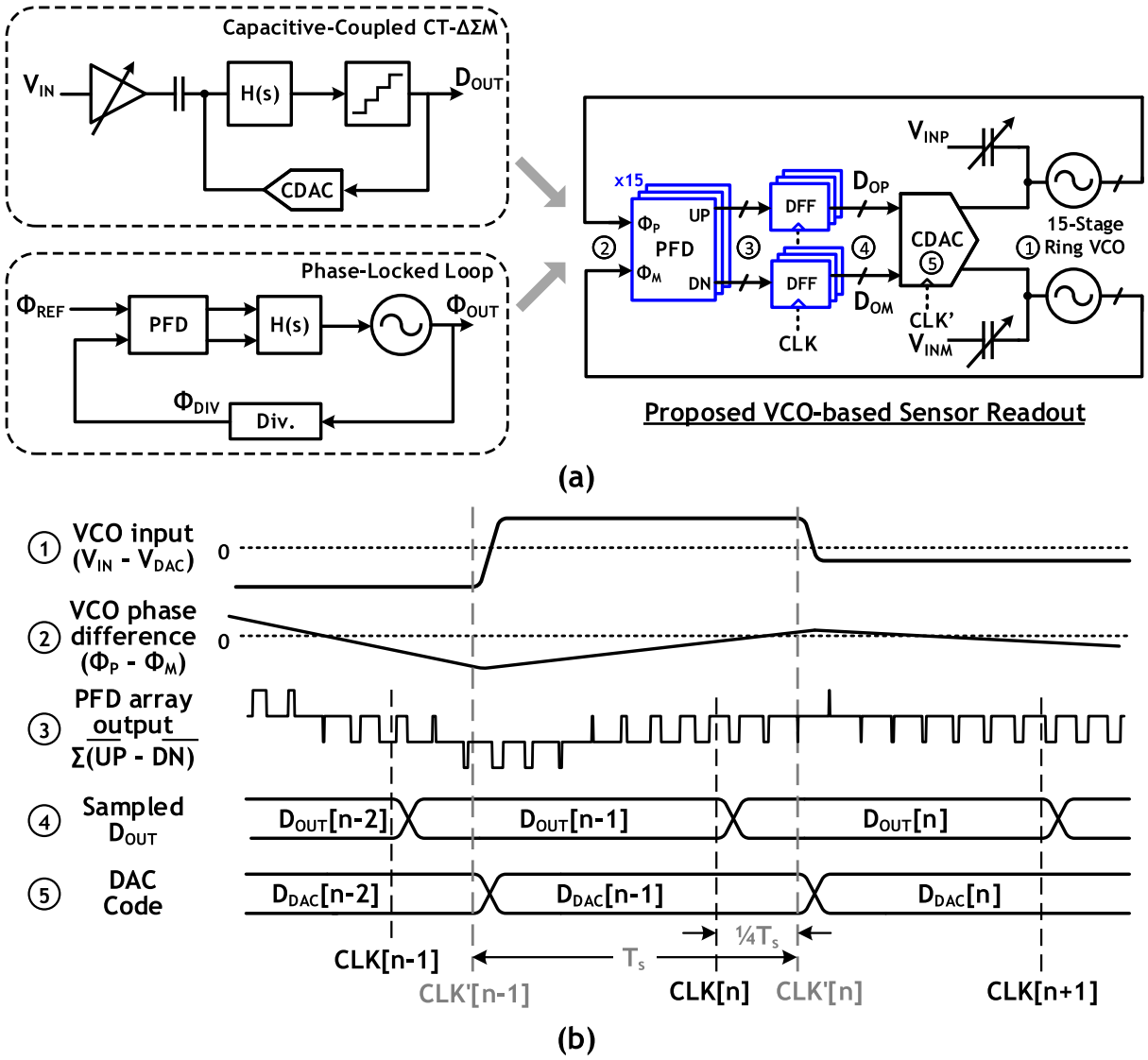

Fig. 5. (a) Conceptual block diagram and (b) operation timing diagram of the proposed hybrid PLL-ΔΣM VCO-based readout.

Φ_{DIV} and converts the phase difference of the two signals into a pulsewidth modulated (PWM) binary output. The PWM effectively retains the phase information while the binary 0/1 output enables simple loop filter control. The loop filter then converts the phase difference to VCO control voltage, which then controls the VCO to suppress phase perturbation. Viewing from the voltage perspective, the PLL takes the output phase of the VCO, uses the PFD to extract phase error, and then uses the loop filter to effectively suppress voltage perturbation at the VCO input. This inspires us to align the PLL's efficient phase-locking mechanism with the CC CT-ΔΣM to create an optimized VCO-based readout.

Fig. 5(a) shows the conceptual diagram of the proposed design, and Fig. 5(b) shows the operation timing diagram. In this PLL-ΔΣM hybrid structure, the 15-stage ring VCO assumes the role of the loop filter. Any perturbation at the VCO input, i.e., the virtual ground node (①), either coupled from input or CDAC, is reflected to the dual-VCO phase difference (②) through the Gm-CCO-based VCO. The integrated phase difference is subsequently detected by the PFD as inherited from the PLL. As will be discussed in detail in Section II-C, the PFD array output (③) reflects the VCO phase difference with a pulsewidth modulated digital output, which is sampled by the DFFs with sampling clock (CLK) as digital output (④). The digital output is then retimed with DFFs controlled by a quarter-cycle delayed clock (CLK') which is readily a set of thermometer code (⑤) for CDAC feedback to the VCO input. The simplified signal diagram is shown in Fig. 6. The loop gain can be derived as

$$\begin{aligned} Loop\ Gain &= K_{INT} \cdot K_{PFD} \cdot K_{DAC} \\ &= (K_{VCO} \cdot T_S \cdot 2\pi) \cdot (\frac{30}{4\pi}) \cdot (\beta \cdot \frac{V_{FS}}{30}) \end{aligned} \quad (1)$$

where K_{INT}, K_{PFD}, and K_{DAC} represents the gain of phase integrator, PFD, and feedback CDAC, respectively. In addition, in the equation, $K_{\mathrm{VCO}} = \mathrm{Gm} \cdot K_{\mathrm{CCO}}$ is the VCO tuning gain, consisting of the transconductance of the Gm stage and the CCO current to frequency conversion gain, T_S is the period

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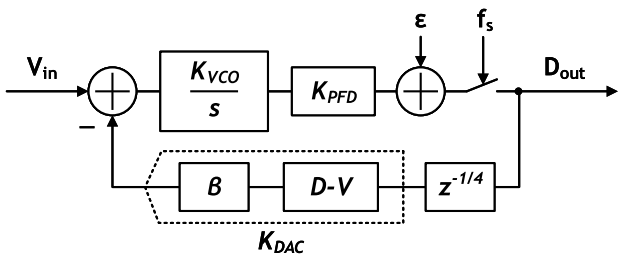

Fig. 6. Signal diagram of the proposed system.

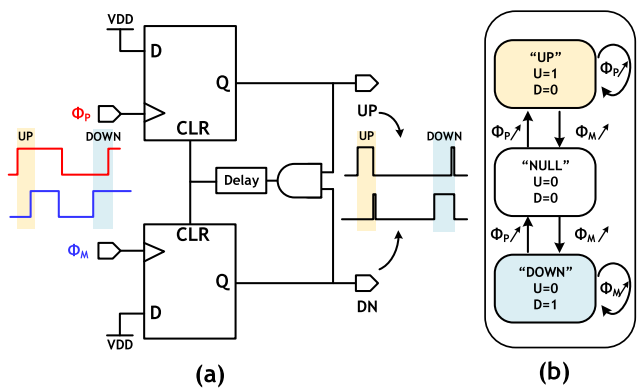

Fig. 7. (a) Schematic and (b) state diagram of the PFD.

of the clock (CLK) controlling the DFFs after the PFD array, i.e., the sampling period, β is the capacitive feedback factor of the loop, and V_{FS} is the full swing of the CDAC reference voltage. A more detailed loop analysis of the proposed system is given in the Appendix.

C. Multi-PFD Quantization Scheme

Inherited from PLL architecture, PFD was chosen to efficiently translate phase information. Before discussing our multi-PFD quantization scheme, we first briefly review the operation theory of a single PFD. The schematic and state diagram of the PFD is shown in Fig. 7. The classic PFD structure is used in this design [25].

The PFD can essentially be considered as a finite-state-machine that is triggered by the input signals. As shown in Fig. 7, assuming the PFD starts from the initial null state where both UP and DN are 0. When the rising edge of Φ_P arrives, UP will become 1 while DN stays at 0, entering the "UP" state. Similarly, when the rising edge of Φ_M arrives, DN will become 1 and UP stays at 0, entering the "DOWN" state. The state will remain until the rising edge of the other signal arrives to clear the state of either "UP" or "DOWN." This phase translation not only achieves phase difference-based PWM but also extracts the lead-lag information simultaneously.

Unlike classic PLLs, where only one PFD with an external clock is used, this design incorporates two changes to the PFD usage that transform it into an efficient quantizer. First, the dual-VCO scheme is adopted, allowing the PFD to be self-referenced without needing an external phase [26]. Second, and more importantly, an array of 15 PFDs is used to detect every delay stage of the VCOs. Through this, multi-level quantization of the phase difference can be directly generated in the form of thermometer code, which can be readily used by the DAC control, without needing an additional logic operation. Compared with prior VCO-based readouts, this approach avoids the formers' "phase-binary-thermometer" conversion routine [20], [21], thus effectively shortening the loop critical path, leading to lower quantizer power.

To elucidate this mechanism, Fig. 8 presents an illustration using a five-stage case. As is known, in each oscillation cycle, the transition edge goes through the ring twice. Leveraging this fact, we can conceptually visualize the VCO's operation as two half-cycles forming a 2π radian, as shown in Fig. 8(a). In the odd half cycle, the odd-numbered cells experience a rising transition (annotated in black), whereas even-numbered cells rise in the even half cycle. In the center of the graph, we use a "phase vector/pointer" to indicate the currently active transition location in VCOs. The phase vector is blue for the outer ring and is red for the inner ring. If there is animation, the phase vectors will move in a counterclockwise manner, with a speed depending on the corresponding VCO's frequency. Since the PFDs only care about the rising transition, if we observe the PFDs in an odd-then-even order (i.e., 1-3-5-2-4), it can be seen that all "adjacent" PFDs are updated with an identical delay when in the steady-state. In other words, the aggregated PFD outputs ($\mathrm{D}_{\Delta\Phi}[n] = \mathrm{UP}[n]\text{-}\mathrm{DN}[n]$) naturally form an array of PWM waveforms that are evenly phase-shifted over 2π, as shown in Fig. 8(c). Such a uniform phase shift allows the temporal information of the waveform to be linearly converted to the spatial pattern. That is, the expected number of "1"s (or "−1"s) in the array at any instance will reflect the pulsewidth. For this reason, it quantizes the phase as thermometer codes. Note that owing to the lead-lag detection capability of the PFD, $\mathrm{D}_{\Delta\Phi}[n]$ by definition is a tri-level PWM waveform. Though only the leading case is shown in Fig. 8(c), the discussion earlier also holds in the lagging case. Accordingly, the PFD array provides 2N-level quantization for an N-stage ring VCO.

The dual-VCO multi-PFD scheme also enables simultaneous phase information extraction of all ring VCO stages, thus breaking the link between VCO free-running frequency (f_{VCO}) and phase quantizer resolution, essentially allowing an arbitrary f_{VCO}. This means that the VCO in the proposed scheme can run at a much lower frequency compared with the conventional counter-based phase quantizer, where VCO frequency is required to be relatively high. In this design, with a sampling frequency of 2.5 MHz, the VCO free-running frequency is only 660 kHz. Putting it all together, the absence of high-speed counter/adder/glitch-free sampler and the lower VCO speed requirements bestow this article significant hardware/power reduction.

Noteworthily, the PFD array is not necessarily the only way to implement PWM-based phase quantization. An array of exclusive-OR (XOR) gates can also provide similar PWM-based thermometer codes [29]. Yet, the XOR array is not able to distinguish the lead-lag of the VCOs' phases, thus losing half of the resolution. As an upgrade to the XOR method, the phase-extended quantizer (PEQ) reported recently can realize both PWM and lead-lag detection [27], which

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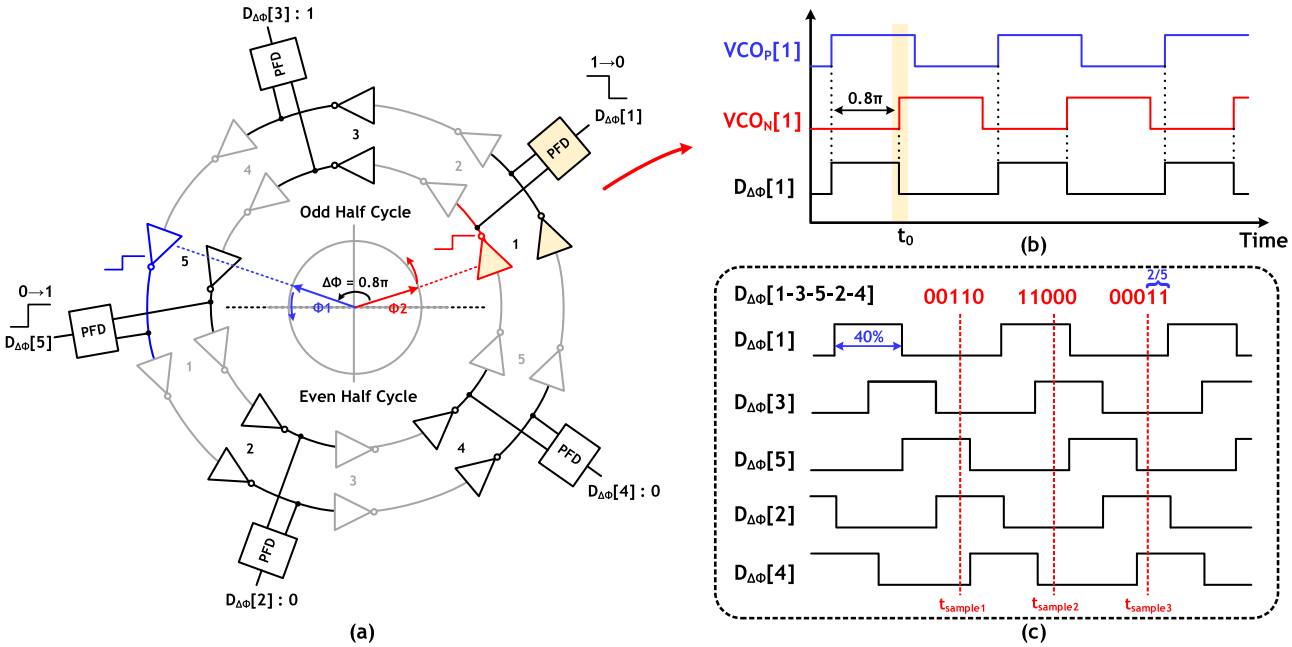

Fig. 8. (a) Conceptual representation of a full VCO period as two half cycles. The black delay cells are the ones that experiences rising in its corresponding half cycle. The blue and red phase pointer indicate the active transition at time t_0. (b) Waveforms of a single VCO-PFD slice. (c) Aggregated waveforms from all PFD outputs ($D_{\Delta\Phi}[n]$ = UP[n]-DN[n]) in steady state.

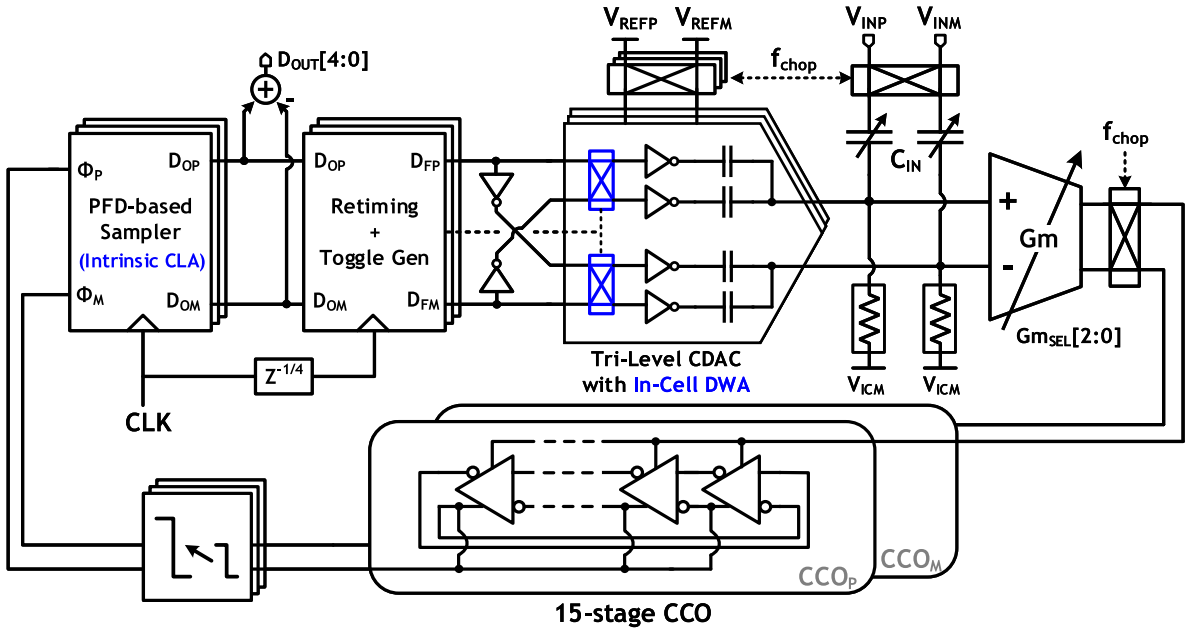

Fig. 9. Simplified schematic of the proposed VCO-based readout.

is functionally equivalent to the PFD array. Nevertheless, the PEQ is oriented to remove the pre-sampler delay for higher speed general-purpose CT-$\Delta\Sigma$Ms, and thus, is higher in complexity and power. On the other hand, though the PFD incurs some pre-sampler delay, in the context of bio/sensor readouts where speed constraints are much relaxed, it does not pose a threat to the loop stability. Hence, the PFD array is deemed a more energy-efficient choice. According to our post-layout simulation, the worst delay from the PFD is within 1 ns across all corners and the temperature range of −30 °C–100 °C, which is negligible compared with the system sampling period being 400 ns. Moreover, the proposed PFD-based approach is more advantageous over PEQ as it incurs less logic switching power. In addition, with the lead-lag information directly extracted from a single-ring VCO delay stage, the layout complexity is greatly relaxed as well. A more detailed comparison is provided in Table I.

III. Circuit Implementation

The simplified schematic of the proposed VCO-based readout is shown in Fig. 9. For simplicity, we use block diagrams to represent: 1) the PFD-based sampler discussed in Section II-C; 2) the simple retiming logic; and 3) the proposed in-cell

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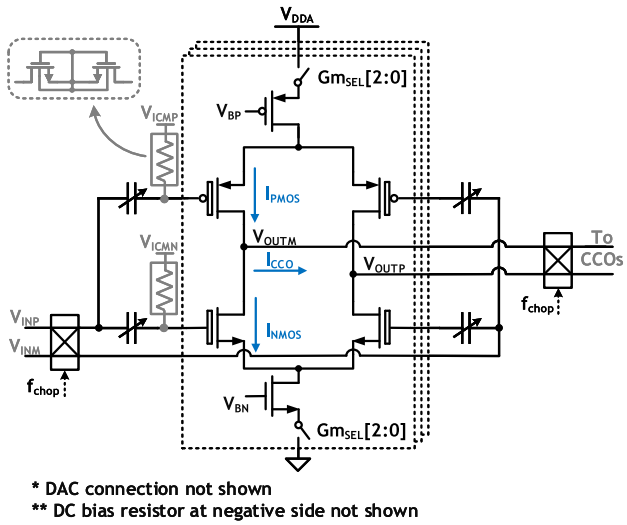

Fig. 10. Schematic of the split-driven current-reusing Gm stage.

TABLE I
COMPARISON BETWEEN PEQ [27] AND THIS ARTICLE

	PEQ [27]	This work
Logic switching activity	High (need resetting comparators)	Low (can use standard DFFs)
Routing complexity	High (need gathering bits from all ring sampler stages)	Low (allows modular-like layout, connections stay local [28])
Excess loop delay	Absorbed into retiming	PFD adds extra delay
Target application	General-purpose ADC	Bio/sensor interfaces

data-weighted averaging (DWA) logic, which will be discussed in detail in Section III-C.

A. Capacitively Coupled VCO-Based Front-End Loop Filter

The VCO is implemented by a Gm-stage-driven CCO. As shown in Fig. 10, to achieve higher noise efficiency, the Gm stage adopts the current-reusing topology, also known as the inverter-based architecture [8], [30], [31]. To cater to a lower supply, the nMOS and pMOS input pairs are split-driven using identical copies of the C_{DAC} and C_{IN} such that the input dc biases can be optimized independently. The dc biases are applied through pseudoresistor implemented by back-to-back connected deep N-well (DNW) nMOS, which is immune to leakage-induced offsets [32]. Both input pairs use a thick-oxide device to avoid gate leakage. CM feedback (CMFB) is not required for the Gm, as the drain-driven CCO provides low input impedance, which helps stabilize the output dc level. The CM output voltage of the Gm stage is 0.3 V and output swing is as small as ±10 mV due to the strong perturbation suppression at the Gm stage input node, i.e., the virtual ground node of the loop.

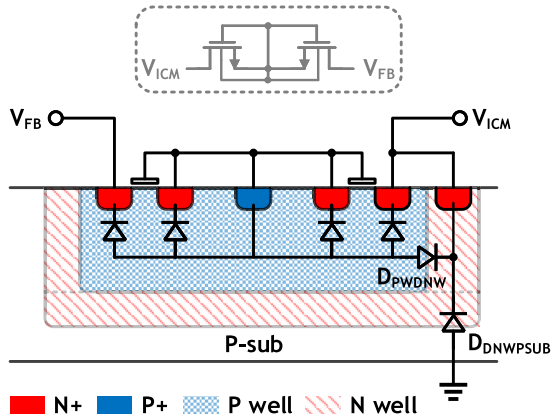

Fig. 11. Schematic and cross section of the back-to-back connected DNW nMOS pseudoresistor.

The schematic and a cross-section illustration of the back-to-back connected DNW nMOS pseudoresistor implemented in this article is shown in Fig. 11. This structure is chosen for its low leakage characteristic, thus avoiding leakage-induced offsets. By using the DNW nMOS transistor and connecting the N-well and DNW to the input bias voltage (V_{ICM}), this structure achieves minimum leakage possible. Except for the DNW to P-substrate diode (D_{DNWPSUB}) being connected between V_{ICM} and ground, all other diodes are connected within the pseudoresistor from the intermediate node to either V_{FB} or V_{ICM}, causing no leakage to supply or ground. The pseudoresistor is designed to have a nominal resistance > 1GΩ under TT corner and room temperature. It is worth noting that although the resistance of the pseudoresistor is sensitive to large voltage swing, the pseudoresistors used in the proposed system are connected to the virtual ground nodes, which only have a very small signal swing. Therefore, the resistance variation or nonlinearity caused by voltage variation is very small and will not affect system performance. Furthermore, any resistance mismatch will be dealt with by chopping applied on the Gm stage, which will be subsequently discussed.

Aside from using long channel devices with a relatively large area, chopping is also applied in this design to mitigate 1/f noise and offset from the Gm. The input chopper is placed before the ac-coupling input capacitors. The output chopper is placed at the Gm stage output before the dual CCO in lieu of simplicity considerations and the fact that CCO flicker noise and offset will be attenuated by Gm when being input-referred. Although chopping applied at Gm output will cause current settling behavior, the small time constant and large loop suppression ensure the settling transition is small and only contributes a very small portion in the integration. Therefore, the settling behavior has a negligible effect on system performance. Our design has an internally generated chopping clock that has a frequency selection from fs/128 to fs/2. With the maximum chopping frequency at 1250 kHz, the input impedance is calculated to be $R_{in} = 1/(2 \times 1250k \times 1.8p) = 222\ k\Omega$. The input impedance can be boosted to 14.2 MΩ when the chopping frequency is reduced to fs/128. Furthermore, the input impedance boosting technique [33] can be

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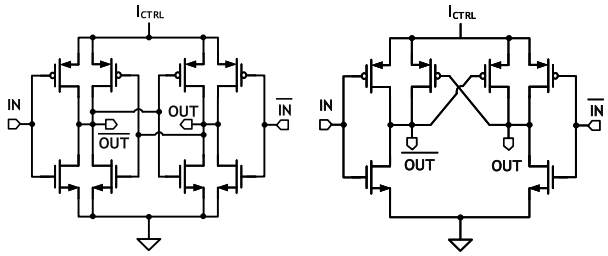

Topology	CMOS coupled	PMOS coupled
ICCO	600 nA	600 nA
KCCO	1.24 THz/A	1.63 THz/A
FCCO	860 kHz	1130 kHz
Noise PSD	447 fA/√Hz	173 fA/√Hz

Fig. 12. Schematic of CMOS-coupled (top left) and pMOS-coupled (top right) CCO delay cells and their phase noise comparison (bottom).

applied for specific applications requiring ultra-high input impedance.

This article is designed to have a nominal input range of 100 mVpp. By exploiting the CC-feedback structure, the range can be reconfigured to 200/400 mVpp by simply disconnecting partial C_{IN}. This expandable range increases the system's tolerance for large inputs, which can be used for artifact protection and a wider range of sensors. To maintain loop stability, the Gm is designed to be adjustable through parallel connection controlled by $\mathrm{Gm}_{\mathrm{SEL}}[2:0]$, as shown in Fig. 10.

B. Low Noise CCO

As labeled in Fig. 10, the CCOs are directly biased by branching the current difference between the pMOS and nMOS pair. With the multi-phase PFD quantizer allowing lower VCO speed, the sub-μA I_{CCO} results in low output swing (≈0.3 V), thus level-shifting is needed between the VCO and the quantizer. To facilitate robust level-shifting, the CCO delay cells are implemented as pseudodifferential inverters, as shown in Fig. 12 (top). The pMOS cross-coupled pair guarantees 180° out-of-phase with minimum noise addition. A simulated phase noise comparison between the pMOS-coupled CCO delay cell and CMOS cross-coupled CCO delay cell is shown in Fig. 12 (bottom). As shown in Fig. 12, the pMOS cross-coupled CCO delay cell not only provides higher tuning gain under the same bias current but also contributes less noise. Intuitively, in the CMOS-coupled design, the cross-coupled nMOS can be viewed as a common-source stage from the small-signal noise perspective. However, the cross-coupled pMOS essentially works as a common-gate stage since the source node of the pMOS connects to the high-impedance Gm output instead of the supply. Therefore, the cross-coupled pMOS structure not only reduces the CCO delay cell loading to increase f_{CCO} but also contributes less noise compared with the CMOS-coupled structure. The level shifter [34] consumes no static power and is designed to produce a sharp rising, which helps reducing PFD ambiguity. The level-shifter delay across process and temperature corners remains within 2% of the entire sampling period, and thus, has a negligible effect on system performance across PVT variations.

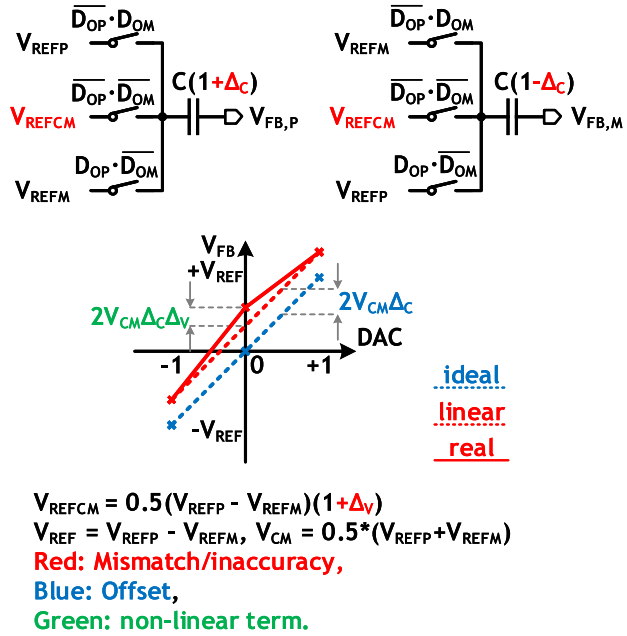

Fig. 13. Illustrations of the conventional tri-level DAC in a fully differential setup (top) and the transfer curve of the tri-level DAC with offset/nonlinear terms caused by capacitor mismatch and V_{REFCM} inaccuracy (bottom).

C. Tri-Level Capacitive Feedback DAC

As per the PFD's logic discussed in Section II-C, the output of a quantizer slice ($D_{\mathrm{OP}}\langle i\rangle$ and $D_{\mathrm{OM}}\langle i\rangle$) has three possible codes: "10," "00," and "01," which can be interpreted as "+1," "0," and "−1" from a DAC control perspective. An intuitive DAC scheme is the direct tri-level mapping to V_{REFP}, V_{REFCM}, and V_{REFM}, as shown in Fig. 13. However, as shown in the bottom digital-to-analog conversion plot, an offset term $2V_{\mathrm{CM}} \cdot \Delta_C$ is added to the tri-level DAC outputs due to differential capacitor mismatch (Δ_C), where $V_{\mathrm{CM}} = (V_{\mathrm{REFP}} + V_{\mathrm{REFM}})/2$ is the ideal mid-level reference voltage. Moreover, if the mid-level reference voltage (V_{REFCM}) also exhibits inaccuracy (Δ_V) with respect to the ideal value (V_{CM}), a mid-level non-linear term will appear as $2V_{\mathrm{CM}} \cdot \Delta_C \Delta_V$. Although the offset does not affect linearity and can be modulated out-of-band through chopping, within the direct tri-level mapping scheme, the non-linear error can only be reduced by two methods that are quite costly: 1) to improve capacitor matching, the area and size of the capacitors have to be increased, introducing the extra area and power cost and 2) to improve V_{REFCM} accuracy, a better voltage source would be required, which causes extra system complexity, area, and power. Moreover, transistors are harder to turn on when connecting to a voltage near half supply voltage, especially for low supply voltage scenarios.

Thus, to avoid these issues discussed earlier, the proposed design implements pseudotri-level feedback through capacitor splitting, as shown in Fig. 9 and more detailed in Fig. 14. As shown in Fig. 14, in each unit cell, by driving two capacitors using one PFD output and the other's complement (D_{OP} and $\overline{D_{\mathrm{OM}}}$, or $\overline{D_{\mathrm{OP}}}$ and D_{OM}), the mid-level feedback is achieved by analog averaging, thus realizing three DAC levels. Comparing with the conventional tri-level mapping, the need for a mid-level reference voltage is replaced by splitting each

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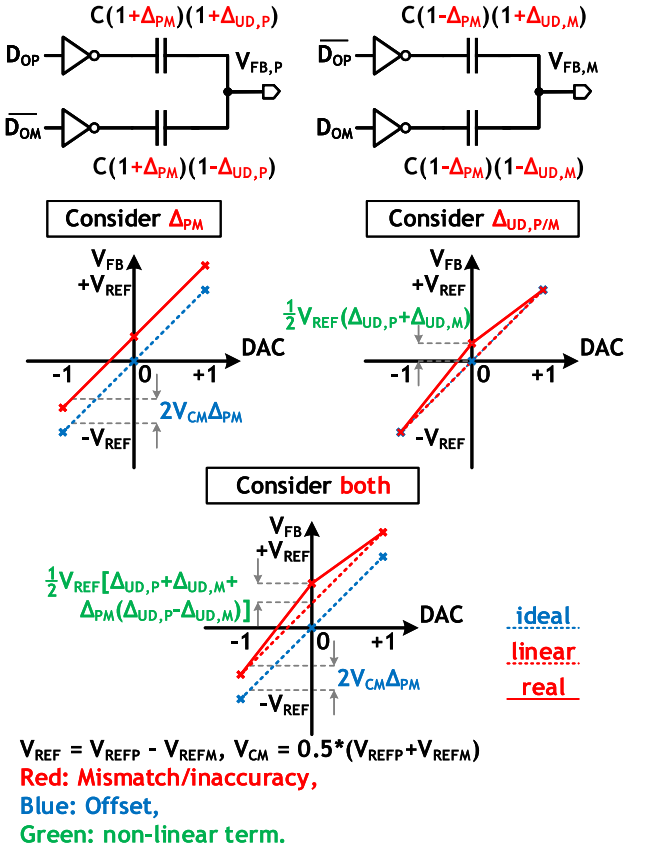

Fig. 14. Illustrations of the pseudotri-level DAC through capacitor splitting (top) and the transfer curves with offset/nonlinear terms due to different capacitor mismatch cases (bottom).

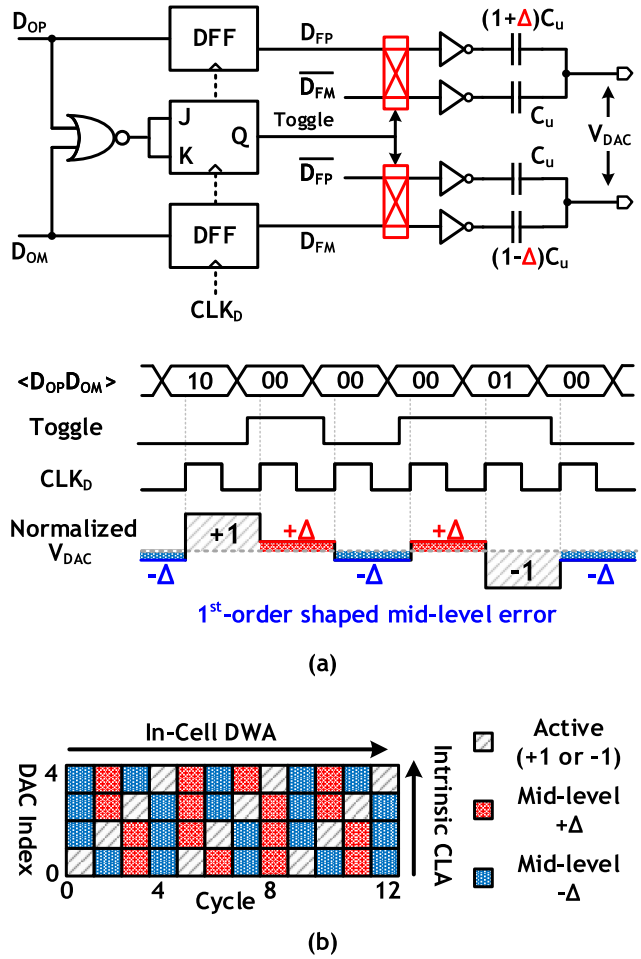

Fig. 15. (a) Illustration of the in-cell DWA implementation of a DAC unit and the timing diagram demonstrating the first-order mid-level mismatch error shaping effect and (b) illustration of the DAC selection pattern under the concurrent DEM in a four-bit DAC example assuming a constant input, only one DAC cell is activated.

of the differential capacitors into two capacitors each side. Now with four capacitors in one DAC slice, the mismatch between capacitors becomes relatively complicated. To better illustrate the effect of each mismatch, we first separate the mismatches into two categories: 1) mismatch between differential capacitors (Δ_{PM}) and 2) the mismatch between the split unit capacitors ($\Delta_{\mathrm{UD},P/M}$). We discuss each of them separately and then analyze the overall effect when combining the two mismatch categories. The corresponding transfer curves are shown in Fig. 14 bottom as labeled.

1) Mismatch Between Differential Capacitors (Δ_{PM}): When $\Delta_{\mathrm{PM}} \neq 0$ while $\Delta_{\mathrm{UD},P/M} = 0$, there is no non-linear term but only an offset term $2V_{\mathrm{CM}}\Delta_{\mathrm{PM}}$ exist for all three DAC levels, which can be modulated out-of-band through chopping.

2) Mismatch Between the Split Unit Capacitors ($\Delta_{\mathrm{UD},P/M}$): When $\Delta_{\mathrm{PM}} = 0$ while $\Delta_{\mathrm{UD},P/M} \neq 0$, there is no offset term but a mid-level non-linear term $V_{\mathrm{REF}} \cdot 1/2 \cdot (\Delta_{\mathrm{UD},P} + \Delta_{\mathrm{UD},M})$ shows up.

3) Considering Both Mismatches: When $\Delta_{\mathrm{PM}} \neq 0$ and $\Delta_{\mathrm{UD},P/M} \neq 0$, the offset term shown in *1)* still exists while the non-linear term becomes $V_{\mathrm{REF}} \cdot 1/2 \cdot [\Delta_{\mathrm{UD},P} + \Delta_{\mathrm{UD},M} + \Delta_{\mathrm{PM}} \cdot (\Delta_{\mathrm{UD},P} - \Delta_{\mathrm{UD},M})]$.

As shown in the above-mentioned analysis, although the pseudotri-level DAC scheme requires no explicit V_{REFCM} as in the conventional tri-level DAC scheme, the mismatch between split unit capacitor still causes mid-level non-linearity. Fortunately, unlike the conventional tri-level DAC scheme where there is no easy way of tackling this problem, this mid-level non-linearity issue in the pseudotri-level DAC scheme can be easily mitigated through the low-cost in-cell DWA, as shown in Fig. 15. With the in-cell DWA, the mid-level mismatch is kept toggling every time it appears and, thus, will be the first-order shaped and prevented from hurting THD. Without the proposed in-cell DWA scheme, the mid-level non-linear error is

$$+\frac{1}{2}Vref[\Delta_{UD,P} + \Delta_{UD,M} + (\Delta_{UD,P} - \Delta_{UD,M}) \cdot \Delta_{PM}]. \tag{2}$$

When the in-cell DWA triggers a toggling, the mid-level non-linear error becomes

$$-\frac{1}{2}Vref[\Delta_{UD,P} + \Delta_{UD,M} + (\Delta_{UD,P} - \Delta_{UD,M}) \cdot \Delta_{PM}] \tag{3}$$

and thus realizing a DWA within each DAC cell.

Comparing with the conventional DWA scheme for multi-bit DAC mismatch error shaping, our proposed scheme does not involve global single-bit DAC element selection, and thus, avoiding complicated logic caused excess delay and

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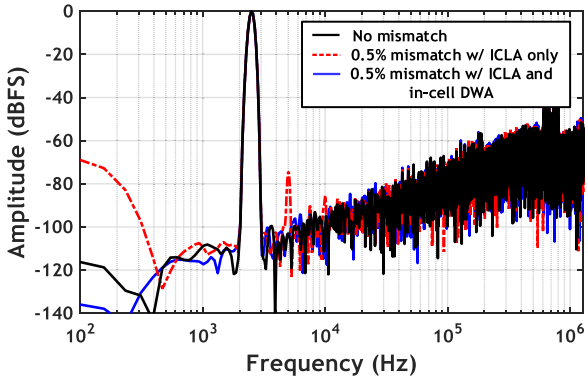

Fig. 16. Simulation result demonstrating the effectiveness of the proposed concurrent DEM scheme.

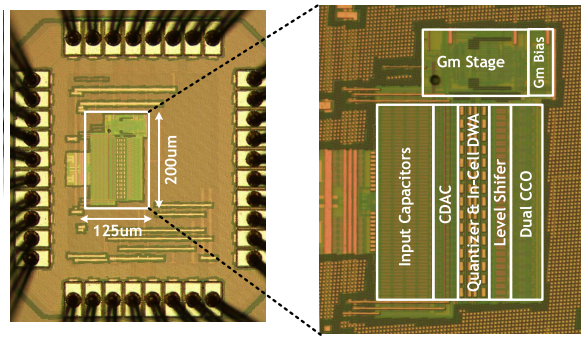

Fig. 17. Die photograph.

area/power issues. Although the proposed in-cell DWA only tackles mismatch errors within one DAC slice rather than a full multi-bit DAC DEM as the conventional DWA scheme, the proposed architecture benefited from the PFD quantizer intrinsically providing a CLA shuffling pattern thanks to its PWM nature, modulating mismatch between DAC cells out of the signal band [26]. Fig. 15 provides an illustration of the concurrent DEM schemes in the readout. In Fig. 15, the capacitor mismatch is shown in a simplified form for simplicity while keeping the generality of the illustration. Despite using only 5-fF unit capacitor, from which the Monte-Carlo simulation shows the unit mismatch error of 0.5% (1σ), the DEM schemes ensure linearity $>$ 14b. To demonstrate the effectiveness of the proposed concurrent DEM scheme featuring the in-cell DWA, the capacitor mismatch in the CDAC is modeled and simulated in the system. As shown in Fig. 16, the intrinsic CLA, though capable of modulating the mismatch-induced odd-order harmonic tones into multiples of the VCO free-running frequency, cannot effectively tackle the even-order harmonic tones caused by the mid-level mismatch. With the proposed in-cell DWA, the even-order harmonic mismatch errors are effectively suppressed and the system linearity can be greatly improved.

IV. Measurement Results

A prototype of the proposed VCO-based readout is fabricated in 40-nm LP-CMOS technology. The silicon die photograph is shown in Fig. 17. Thanks to the direct-digitizing topology obviating the separated IA and the mostly digital

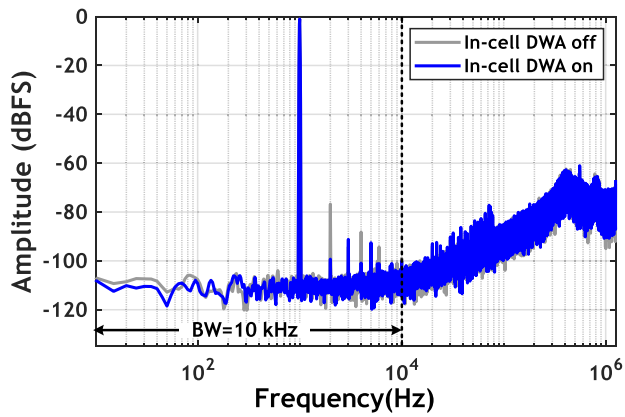

Fig. 18. Measured output spectra with in-cell DWA ON/OFF.

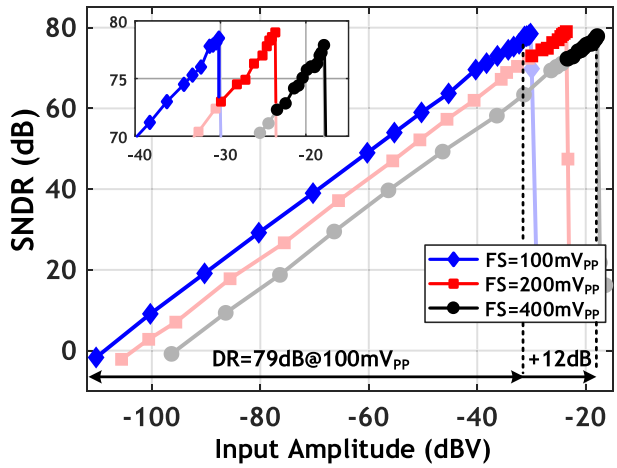

Fig. 19. Measured SNDR versus input amplitude.

scaling-friendly nature of the VCO-based architecture, the proposed readout only occupies an active area of 0.025 mm^2.

Fig. 18 shows the measured output spectrum with the 1-kHz 90-mVpp signal between the cases of the proposed in-cell DWA being ON and OFF. As shown in Fig. 18, when in-cell DWA is disabled, even-order harmonic tones stand out, limiting SFDR to only 78 dB and SNDR to 73.6 dB. Enabling the in-cell DWA, the second-order harmonic is reduced by 13 dB, along with higher even-order harmonics caused by mid-level mismatch also being greatly reduced. Thanks to the proposed in-cell DWA, an SNDR of 78.5 dB is achieved with an SFDR of 91 dB.

The DR of the readout is measured with each individual VGA gain setup, and the results are shown in Fig. 19. As shown in Fig. 19, for the original nominal setup of 100-mVpp full swing, 79-dB DR is achieved. With the other two gain mode achieving similar DR, the full DR of the readout can be extended to 91 dB which covers the most common artifact when detecting a small signal.

Operating under 0.8-V analog and 0.6-V digital/DAC supplies and at the nominal 100-mVpp mode, the readout prototype consumes 4.68 μW when sampling at 2.5 MHz. The dual-VCO loop filter, digital blocks (including PFD, the following logics and samplers) and the capacitive feedback DAC consumes 2.74, 1.16, and 0.78 μW, respectively. Fig. 20

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TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS

Specifications	[11]	[10]	[16]	[17]	[20]	[19]	[21]	This work
Architecture	CCIA + OTA CTΔΣM	CCIA + OTA CTΔΣM	CTΔΣM Incremental	Gm-C CTΔΣM	Open-loop VCO-ADC	Open-loop VCO-ADC	Closed-loop VCO-ADC	PLL-ΔΣM
Quantizer Type	1-bit Comparator	SAR	SAR	SAR	VCO-Counter	VCO-XOR-based	VCO-Counter	PFD Array
Technology [nm]	180	40	180	180	40	40	40	40
Active Area [mm^2]	0.73	0.113	0.18^d	0.55	0.135	0.0145	0.06	**0.025**
Supply [V]	1.8	1.2	1	1	1.2(A) 0.45(D)	1.2	1.2	0.8(A) 0.6(D)
Power [μW]	1200	7.3	8	6.5	7	17	21	4.68
Fs [MS/s]	2	0.4	0.001	0.0128	0.003	4.2	1	2.5
Bandwidth [kHz]	1	5	0.5	0.3	0.001-0.2	5	2	10
FS Range [mVpp]	20	200	100	360	100	8	100	100/400
CMRR/PSRR [dB]	134 (DC)/ N/A	N/A	N/A	84	66	97/91	N/A	83/80
DC Offset [mV]	0.007	N/A	N/A	N/A	<1	0.05	0.3	0.05
DR [dB]	N/A	81	90	92.3	N/A	62	76.3	79/91
SNDR [dB]	N/A	78	63.2	84.3	74	61.85	74.9	78.5
SFDR [dB]	N/A	82	73.7	104.7	79	N/A	82	91
IRN PSD [nV/$\sqrt{Hz}$]	3.7	90	71	265	368	32	142	36
FoM$_{S,SNDR}$ ^{a} [dB]	N/A	166.4	141.2	160.9	148.6	146.5	154.7	**172**
FoM$_{S,DR}$ ^{b} [dB]	N/A	169.4	168	168.9	N/A	146.7	156.1	**184.5**
PEF^c	44	87	60.8	676	1399	25.6	625	**8.9**

a. $FoM_{S,SNDR} = SNDR + 10\log_{10}(BW/Power)$
b. $FoM_{S,DR} = DR + 10\log_{10}(BW/Power)$
c. $PEF = {v_{n,rms}}^2 \cdot \frac{Power}{BW \cdot \frac{\pi}{2} \cdot 4kT \cdot V_T}$
d. Total area of a full neural recording channel

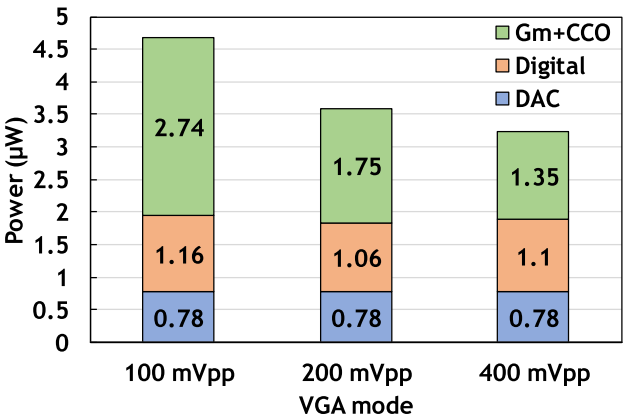

Fig. 20. Power breakdown with VGA mode of 100-/200-/400-mVpp full scale.

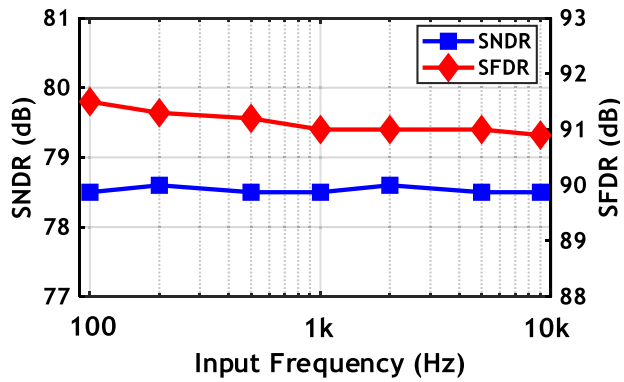

Fig. 21. Measured SNDR/SFDR versus input frequency.

shows the power breakdown when operating at the nominal 100-mVpp mode and the two range expansion modes. As can be seen from Fig. 20, the VCO power is reduced considerably when operating under 200-/400-mVpp mode due to the scaled Gm stage maintaining the same loop gain while the feedback factor and the closed-loop gain are adjusted for range expansion, resulting in extra power saving.

The SNDR and SFDR are measured versus input frequency, and the result is shown in Fig. 21. As can be observed from Fig. 21, both the SNDR and SFDR are mostly flat, demonstrating consistent performance across the signal band.

The IRN PSD is 36 nV/$\sqrt{\text{Hz}}$, leading to a PEF of 8.9. The overall noise performance is dominated by the thermal noise of the Gm stage which contributes ~60% of the total in-band noise. The total in-band quantization noise is designed to be ~1.8 μVrms. The CCO noise contribution is greatly suppressed by the Gm stage when being input-referred, and thus, only contributes less than 1%. Chopping induced noise fold back and Gm stage nonlinearity also contributes slightly to the in-band noise floor. Thanks to chopping, the design demonstrates a low dc offset of 50 μV. The measured in-band CMRR and PSRR are 83 and 80 dB, respectively. The high CMRR suggests that the design is capable of direct digitizing without needing an IA.

To demonstrate the proposed system's capability for real-world sensor readout, a three-lead on-body ECG recording is conducted, and the recorded waveform is shown in Fig. 22. This measurement uses an on-chest placement for

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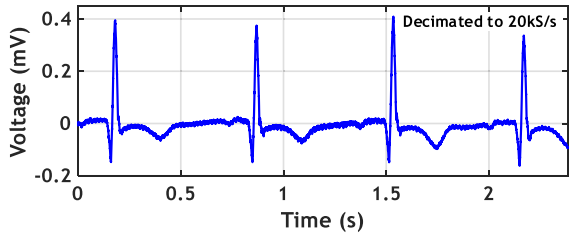

Fig. 22. On-body ECG recorded by the proposed readout.

the electrodes. The signal leads are directly connected to the sensor readout differential input, while the reference electrode is connected to the ground. The waveform shown is post-decimation. Unlike other measurements where fs/2 is used as chopping frequency, the chopping frequency applied for ECG measurement is reduced to fs/64 in order to boost the input impedance of the system.

Table II provides a performance summary and comparison with the state-of-the-art sensor readout circuits. This article achieves a peak Schreier FoM of 172 dB, advancing the highest FoM VCO-based design in [21] by 50×. The PEF of this article (8.9) also advances the state-of-the-art of sensor readout in [10] by 10×. Owing to its direct-digitizing and scaling-friendly architecture, its area is only 0.025 mm^2. It represents the state-of-the-art for both power and area efficiency for readouts with comparable performance, to the best of our knowledge. In summary, this article has demonstrated a useful perspective of designing high-performance VCO-based readout leveraging the PLL-$\Delta\Sigma$M hybrid structure.

V. Conclusion

This article presented an energy and area efficient VCO-based sensor readout circuit that leverages the hybrid PLL-$\Delta\Sigma$M structure. The VCO-based loop filter, along with multi-PFD structure, achieves first-order noise shaping and efficient use of VCO phase information for multi-bit quantization. The multi-bit CDAC feedback accuracy is guaranteed by a concurrent DEM scheme incorporating the intrinsic CLA from the VCO integrator's PWM nature and a simple in-cell DWA scheme tackling the tri-level DAC's mid-level error. To provide the capability of large artifact tolerance, a VGA mode is achieved by variable input capacitor and Gm. This article achieves the best FoM and the smallest area among all VCO-based sensor readout reported, and definitely stands among the state-of-the-art sensor readout circuits, providing another valuable solution for IoT sensor readout.

Appendix
System Loop Analysis

As discussed in Section II-B, the proposed first-order $\Delta\Sigma$ loop consists of a VCO-based phase integrator, a multi-PFD phase quantizer, and a feedback CDAC, where K_{INT}, K_{PFD}, and K_{DAC} represents the gain of those three major blocks, respectively.

Since the VCO-based phase integrator uses a VCO, i.e., a Gm stage followed by a CCO, to conduct phase integration based on input and feedback information within one sampling period, the K_{INT} can be further expanded as

$$\begin{aligned} K_{INT} &= K_{VCO} \cdot T_S \cdot 2\pi \\ &= Gm \cdot K_{CCO} \cdot T_S \cdot 2\pi \end{aligned} \tag{4}$$

where $K_{\mathrm{VCO}} = \mathrm{Gm} \cdot K_{\mathrm{CCO}}$ is the VCO tuning gain, T_S is the sampling period, and 2π is the frequency-to-phase conversion factor.

The multi-PFD phase quantizer translates input phase difference of the dual CCO into output quantization levels and a 15-stage ring CCO followed by 15 PFDs essentially creates 30 quantization levels for the $-2\pi \sim 2\pi$ phase range for each CCO output. Thus,

$$\begin{aligned} K_{PFD} &= \frac{total\ number\ of\ quantization\ levels}{phase\ range} \\ &= \frac{30}{4\pi}. \end{aligned} \tag{5}$$

The feedback CDAC can be viewed to have two functions: 1) converting the digital output back to an analog voltage and 2) closing the loop to feedback this analog voltage. Thus, the gain of this feedback stage can be separated into the corresponding two parts, K_{D-V} and β, where K_{D-V} is the digital-to-analog conversion gain which is the full-swing reference voltage divided by the total quantization levels and β is the feedback factor. Thus, K_{DAC} can be expressed as

$$\begin{aligned} K_{DAC} &= K_{D-V} \cdot \beta \\ &= \frac{V_{FS}}{30} \cdot \beta. \end{aligned} \tag{6}$$

Therefore, the loop gain of the proposed system is derived as

$$\begin{aligned} Loop\ Gain &= K_{INT} \cdot K_{PFD} \cdot K_{DAC} \\ &= (K_{VCO} \cdot T_S \cdot 2\pi) \cdot (\frac{30}{4\pi}) \cdot (\beta \cdot \frac{V_{FS}}{30}). \end{aligned} \tag{7}$$

Acknowledgment

The authors would like to thank the Taiwan Semiconductor Manufacturing Company (TSMC) University Shuttle Program, especially Dr. E. Soenen, Dr. A. Roth, and Dr. M. Kinyua, for their help on the chip fabrication.

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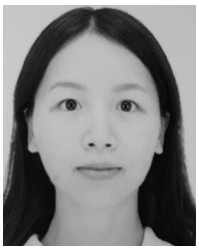

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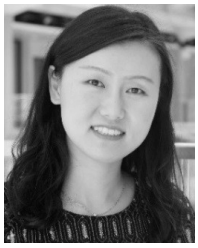

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