A 1V 0.25uW Inverter-Stacking Amplifier with 1.07 Noise Efficiency Factor

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Abstract

This paper presents a highly power efficient amplifier. By stacking inverters and splitting the capacitor feedback network, the proposed amplifier achieves 6-time current reuse, thereby significantly boosting g_m and lowering noise but without increasing power. A novel biasing scheme is devised to ensure robust operation under 1V supply. A prototype in 180nm CMOS has 5.5uV rms noise within 10kHz BW while consuming only 0.25uW, leading to a noise efficiency factor (NEF) of 1.07, which is the best among reported amplifiers.

Introduction

The front-end amplifier typically dominates the overall noise and power performance of a sensor system. There exists a fundamental tradeoff between noise and power for an amplifier, which is well captured by NEF [1]-[2]. Minimizing this tradeoff (or NEF) is crucial for a wide range of power and energy constrained applications, especially in biomedical implants due to stringent requirements on battery life and heat dissipation. Many excellent research works aim to improve the power efficiency. The central idea is to boost the overall amplifier g_m but without increasing the bias current. Classic techniques include: 1) biasing the input pair in subthreshold region to maximize g_m/I_D, and 2) adopting an inverter input stage to reuse the bias current twice. The work of [3] adopts these techniques, achieving 2-time current reuse under low voltage, but it requires multiple power supplies and has to deal with the PSRR issue due to its pseudo-differential input pair. The orthogonal current reuse technique of [4] boosts the level of current reuse, allowing N-time current reuse among N-channel inputs, but it has 2^N number of output branches to combine, leading to increased power/complexity of peripheral circuits and loss in the overall power efficiency. Recently, by using AC coupling and multi-chopper, the work of [5] realizes 6-time current reuse for a single-channel input. It also reduces the number of summing branches to $2^{N/2}$ by using both NMOS and PMOS pairs, but it still does not eliminate the exponential dependence. It obtained the previously best NEF of 1.38, but this is under open loop. When placing the amplifier in a practical closed-loop setup, the NEF would inevitably degrade due to intrinsically increased input referred noise, especially considering the parasitic capacitance at virtual ground nodes.

This work proposes a novel power efficient amplifier. By stacking N inverters and splitting the capacitive feedback into N paths, it achieves $2N$-time current reuse for a single-channel input. Unlike [4] and [5], it has only N output branches to combine, thus turning the prior exponential dependence into a mild linear dependence. It greatly reduces the total current and achieves the best-reported NEF to authors' best knowledge.

Proposed Inverter Stacking Amplifier (ISA)

Fig. 1 shows the block diagram of the proposed closed-loop ISA. Its core is an array of N vertically stacked inverter-based transconductor. The common-gate (CG) transistors are used to add up output currents from each transconductor. The capacitive feedback network is split into N paths so that the ISA input voltage can be AC-coupled to each individual transconductor. On the top level, the proposed ISA behaves the same as a classic closed-loop amplifier except that its bias current is reused by $2N$ times.

The proposed ISA topology works for any integer N. For simplicity, Fig. 2 shows an example schematic with N=2. The bias voltages of input transistors are applied using pseudo resistors [2] and are set carefully to minimize the requirement on V_{DD} as well as to ensure all input pairs are in subthreshold region to maximize g_m/I_D. Since the V_{GS} of the NMOS pair of the top inverter is tightly coupled with the V_{GS} of the PMOS pair of the lower inverter, a replica bias circuit is devised to ensure robustness against PVT variations. To minimize current, the proposed ISA has only 1 main bias branch, which also provides bias voltages for 2nd CG stage through resistive voltage dividers. The output currents from the input stages are summed up by CG transistors. Resistive averaging is also used to sense the output common-mode voltage and directly control the tail current source for CMFB.

Fig. 3 shows the equivalent circuit of the input stage. For a differential-mode input (left), the connection node between the 2 stacked inverters acts as a virtual ground, and thus, the overall g_m is boosted by 4 times. By contrast, for a common mode input (right), because of the tight coupling between the gate voltages, the connection node has a high impedance although it connects to the transistor source terminal. This property ensures a high CMRR. To obtain a high PSRR, two current sources are placed on top and bottom to isolate the inverter core from both power lines.

Fig. 4 shows the general noise analysis of the closed-loop ISA. Both signal transfer function (STF) and amplifier noise transfer function (NTF) are calculated. The amplifier noise V_n is inherently amplified more than the input V_{in}, which shows the inevitable NEF degradation in a closed-loop setup comparing to open-loop. To improve NEF and reduce NTF, the parasitic capacitance at the input nodes needs to be minimized. To this end, a semi-sandwich layout is used to reduce the top plate capacitance of C_S and C_F. According to simulation, this technique reduces the total parasitic capacitance by 50% and improves the NEF by 17%.

Measurement Results

To verify the proposed ISA topology, 2 prototypes are implemented in 180nm CMOS: one with 2 stacked inverters and the other with 3 stacked inverters. Fig. 5 shows the measured amplifier frequency response, which matches the target application of action potential recording whose signal BW is from 250Hz to 10kHz [1]. The measured input referred noise (IRN) PSD is shown in Fig. 6. The measured total in-band rms IRN are 6.7uV and 5.5uV for stack-2 and stack-3 versions, respectively. The measured NEF for stack-2/3 are 1.24 and 1.07, respectively. As shown in Fig. 7 and Table I, this work achieves the best-reported NEF. It establishes a new tradeoff between noise and power, and pushes the NEF boundary to a new level. The die photos of the 2 chips are shown in Fig. 8.

Reference

[1] R. Muller, et al, JSSC 2015. [2] R. Harrison et al, JSSC 2003.
[3] S. Song et al, BioCAS 2015. [4] J. Ben et al, JSSC 2013.
[5] Y. Chen et al, VLSI 2014. [6] F. Yaul et al, ISSCC 2016.

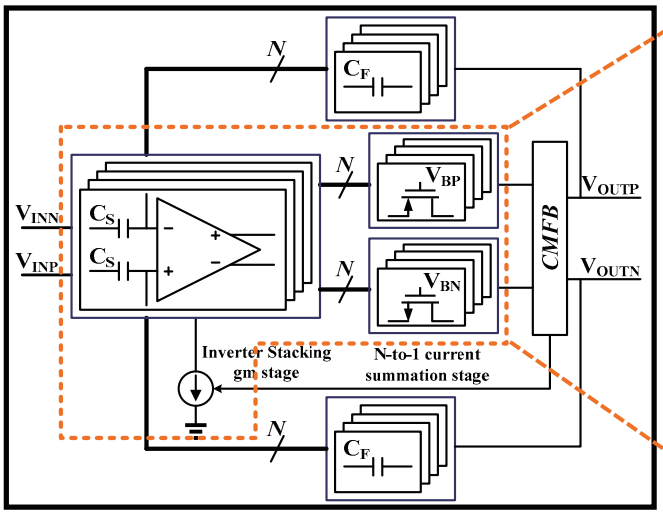

Fig. 1 Conceptual diagram of the proposed inverter-stacking amplifier.

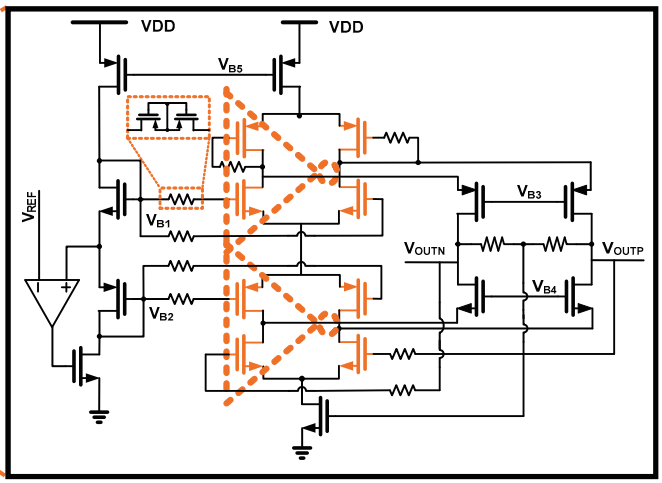

Fig. 2 Schematic of 2 inverter stacking amplifier

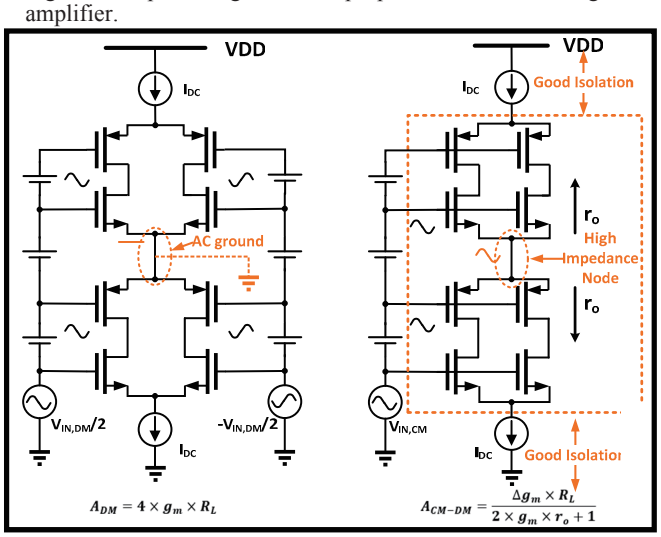

Fig. 3 Differential-mode and common-mode circuit analysis

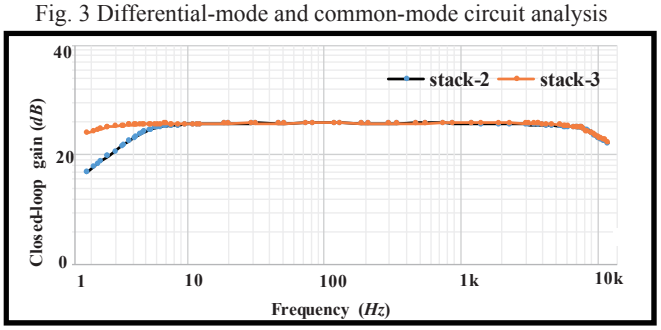

Fig. 5 Measured amplifier frequency response

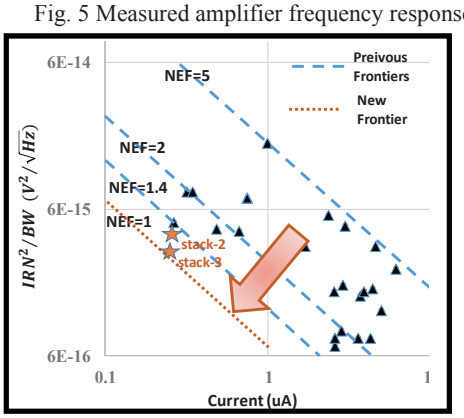

Fig. 7 Current-noise tradeoff, and NEF comparisons

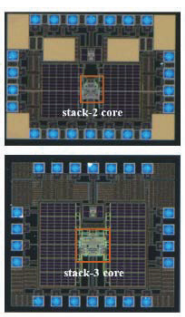

Fig. 8 Die photo of stack-2(top) and stack-3 (bottom) amplifiers

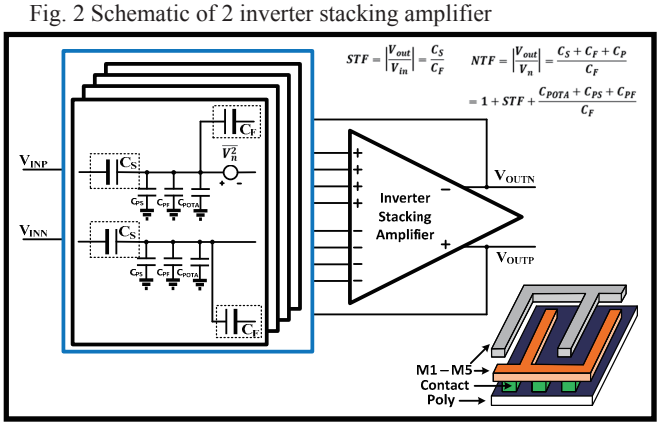

Fig. 4 Signal and noise transfer functions of the proposed closed-loop inverter stacking amplifier

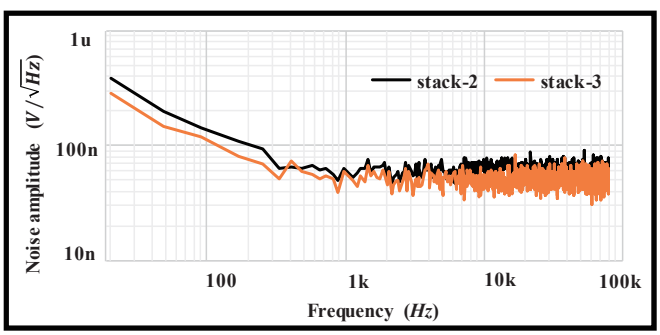

Fig. 6 Measured amplifier input referred noise PSD

	This work		[3] BioCAS 2015	[4] JSSC 2013	[5] VLSI 2014	[6] ISSCC 2016
	Stack-2	Stack-3				
Closed-loop	Y		Y	Y	N	Y
Process	0.18µm		0.18µm	0.13µm	0.18µm	0.18µm
Area(mm^2)	**0.01**	**0.02**	N/A	0.125	0.02	N/A
Gain(dB)	**25.4**	**25.6**	33	40	59.2	57.8
CMRR(dB)	**82**	**84**	>70	78	89	80
PSRR(dB)	**81**	**76**	>70	80	92	85
VDD(V)	**0.9**	**1.0**	0.3/0.6	1.5	1	0.2/0.8
Power(µW)	**0.23**	**0.25**	1.17	3.9	0.266	0.79
Bandwidth(Hz)	**10k**	**10k**	182	19.9k	804.3	670
IRN(μV_{rms})	**6.7**	**5.5**	0.34	3.7	1.54	0.94
NEF	**1.24**	**1.07**	1.74	1.64	1.38	2.1
PEF	**1.33**	**1.14**	1.41	4.03	1.9	1.6

Table I. Performance summary and comparison with latest works