DC-DC Converter Design

Vic Frederick

This article covers the operation, design aspects, and a methodology for a direct current to direct current (DC-DC) power electronic based on the notes from Dr. Hanson's Fundamentals of Power Electronics course and Dr. Flynn's Power Electronics Lab prioritized through my experiences in UT design teams and internships.

Power electronic are electronic circuits that process power as opposed to most other electronics that process information. The most well-known power electronics are:

Buck Converters

Boost Converters

Buck Boost Converters

Low Dropout Regulators

Isolated DC-DC Converters

Rectifiers

Inverters

Isolators

Coulomb Counters

Battery Changers

Motor Drives

Alternators

Power Management Integrated Circuits (PMIC)

This article will focus on the first electronic, but many of the principles covered here are generally applicable to the field. The reason for focusing on buck converters is that they are the mostly likely to have a discrete single board implementation with many factors left in the electronic designer's hands. Grid and high voltage electronics are also discrete, but their dangerous and critical operation requires more professionalism than this article assumes. As a side note, MPICs are unique in their ability to integrate many power electronic functions into a small form factor.
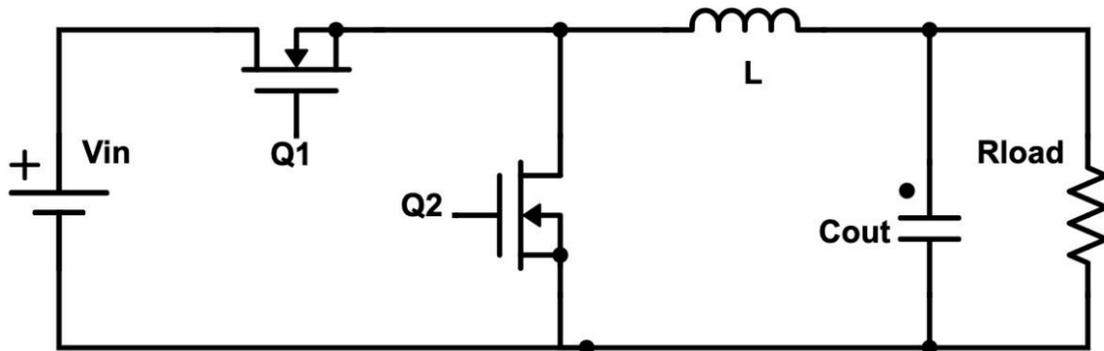
Buck Converters

Buck converters are the workhouse of the power electronic world. What most people need is a way to get a low voltage than what they have, and bucks balance efficiency and complexity to get that lower voltage.

Operation

Buck converters move the same power to a lower voltage and an appropriately higher current by turning the input on (Vin) and off (GND) with a transistor switch then filtering to regain a DC output with an LC filter. Ideally neither step consumes any power, so the output to input current ratio should inversely follow the output to input voltage ratio. The filter must be sized for the speed that the switch is being flipped called the switching frequency (fsw), and the proportion of switching time that the switch is connected to the input is called the duty cycle (D). This switching on and off of the input is called pulse width modulation (PWM) because the output is going to end up being a function of the width (D).
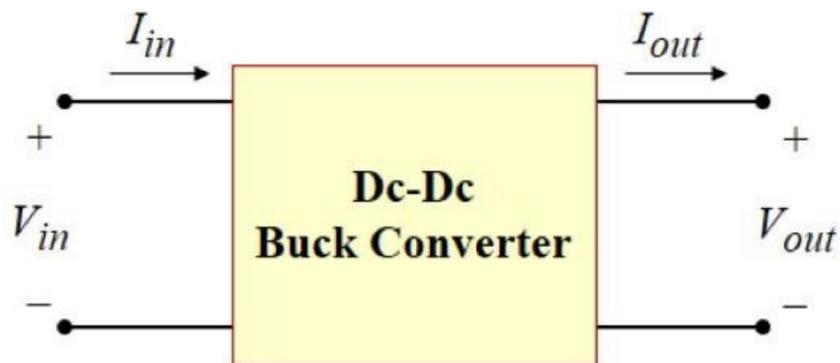
Port View of Buck Converter *Flynn Fall 2019*

Schematic View of Synchronous Buck Converter

$$Period = T_{sw} = \frac{1}{f_{sw}}$$
<div style="text-align:right">Equation 1</div>

$$Duty\ Cycle = D = \frac{T_{on}}{T_{sw}}$$
<div style="text-align:right">Equation 2</div>

To find the output voltage in terms of the duty cycle we can use the fact that the inductor is in periotic steady state meaning that the sum of the inductor voltages over the switching period is zero. The following equations are KVL for the outside loop when the top switch is closed for (DT) amount of time and the bottom is open and vice versa for (1-D)T time.

DT: $\qquad V_L = V_{in} - V_{out}$ $\hfill$ Equation 3

$(1-D)T$: $V_L = -V_{out}$ $\hfill$ Equation 4

Solving for (Vout) gives the approximate transfer function of the buck. The only assumption made is the fact that (Vout) is a constant across the two switching phases.

$$V_{out} = DV_{in}$$ $\hfill$ Equation 5

The peak-to-peak ripple of the inductor current can be found with this approximation as well. Faraday's law adopted to inductors Equation 6 can be rewritten at Equation 7 for ease of use. During the positive duty cycle (DT) current in the inductor will rise by Equation 8, and during the negative duty cycle (1-D)T the same change in current will occur with a negative sign.

$$V_L = L\frac{dI_L}{dt}$$ $\hfill$ Equation 6

$$\Delta I_L = \frac{V_L}{L}\Delta T$$ $\hfill$ Equation 7

$$\Delta I_L = \frac{V_{in} - V_{out}}{L}DT$$ $\hfill$ Equation 8

$$\Delta I_L = \frac{-V_{out}}{L}(1-D)T$$ $\hfill$ Equation 9

An output voltage ripple can be defined using the area under the positive capacitor current divided its capacitance. Using the periodic steady state analysis now on the capacitor, the sum of the currents through the capacitor over the period must be zero. None of the DC current through the inductor can flow though the capacitor. We assume that all the inductor ripple current travels through the capacitor due to its low impedance at the switching frequency compared to the load.
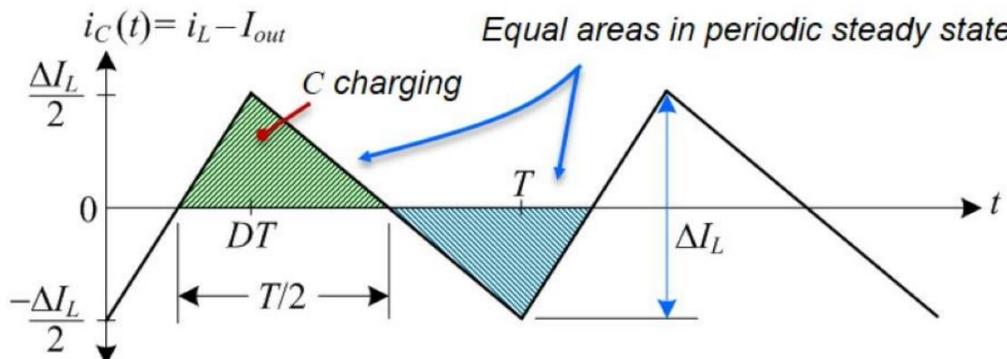
Output Capacitor Current *Flynn Fall 2019*

$$I_c = C\frac{dV_c}{dt}$$ $\hfill$ Equation 10

$$\Delta V_{out} = \frac{\Delta Q}{C} = \frac{\frac{1}{2}*\frac{T}{2}*\frac{\Delta I_L}{2}}{C} = \frac{\Delta I_L}{8C}T$$ $\hfill$ Equation 11

Design Aspects

Now that we have covered the basic operation of the buck converter, there is a laundry list of concerns and options when it comes to design. Here is what we want from a buck converter:

Tight Output Voltage Ripple: Most electronics we are powering cannot tolerate large supply changes at speeds we would like to switch at. Equation 11 represents the output voltage ripple added to the supply due to switching. Additional ripple is added by the equivalent series resistance (ESR) of the output capacitor noting that the voltage waveforms are 90 degrees out of phase.

$$\Delta V_{out_{with\ ESR}} = \Delta I_L \sqrt{\frac{T^2}{64C^2} + ESR^2}$$
\hfill Equation 12

Tight Load Regulation: Load regulation is the variation of the output voltage across a range of load currents. Most electronics draw different currents depending on what they are doing, but they will work best with a consistent supply voltage across their current needs. Load regulation is largely set by the precision of the feedback network.

High Efficiency: We want to process the power without losing much of it. Losses can lead to excess heat and significant battery life shortening. Equation 13 gives a measurable expression for what needs to be optimized, but (Vout), (Vin), and (Iout) are usually specified leaving (Iin) to be minimized to Equation 14.

$$Efficency: \ \eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}}$$
\hfill Equation 13

$$I_{in_{ideal}} = DI_{out}$$
\hfill Equation 14

Transient Settling Time: The transient time is given by the time it takes for the output voltage to settle within some tolerance of the desired output. The system wants to turn on as fast as possible to accomplish the task at hand, and nothing can run before it is smoothly powered.

Size: The volume and weight of a buck converter can severely limit what systems it goes into. All else equal, the smaller the solution means there are more problems it can solve. Smartphones will be a hard sell for discrete buck converters, but vehicles can have dozens. Every millimeter cubed saved can bring new customers and projects to your designs.

Thermals: In hot environments resistances get larger, capacitor dielectric permittivity get lower, inductor permeability shrinks, indicators more readily saturate, and capacitor breakdown voltages lower. Heat can shorten the life of many electronics. Reducing losses means reducing the heat produced by our buck converter.

Electromagnetic Interference (EMI): A switching power electronic is not only responsible for the waves it interjects back into the source but also the waves propagating into the air. In a radio since, switching frequencies are usually classified in the low frequency(30-300kHz) to medium frequency(300kHz-3MHz) spectrums, so long traces can unfortunately still be radiators.

Switching Scheme

The basic buck converter has two switching scheme options, asynchronous or synchronous.

Asynchronous Asynchronous uses a diode to make the negative duty cycle ground connection in the switching loop. This is usually more lossy as we will show, but it requires no gate driving. Some size benefits can be made with a diode solution when the losses are admissible. Current must remain positive in the inductor if systems dynamics are evaluated with continuous current in the inductor.
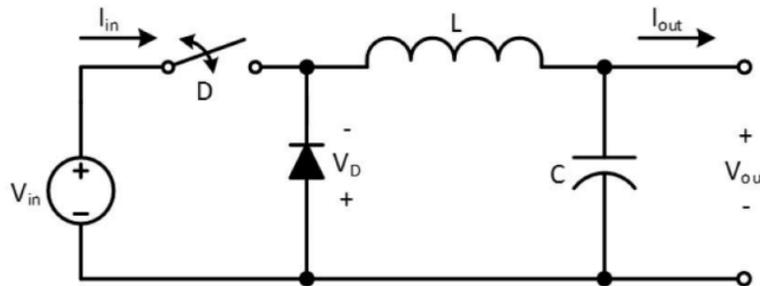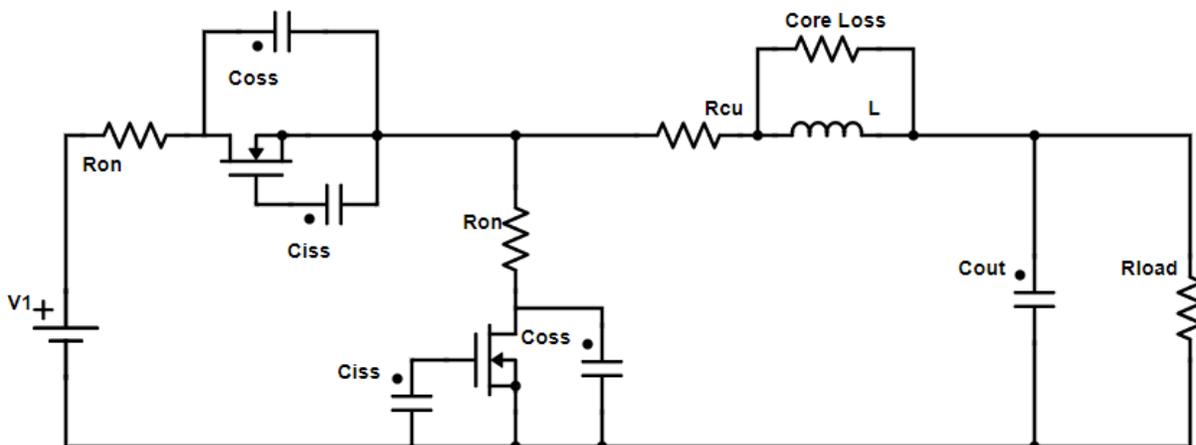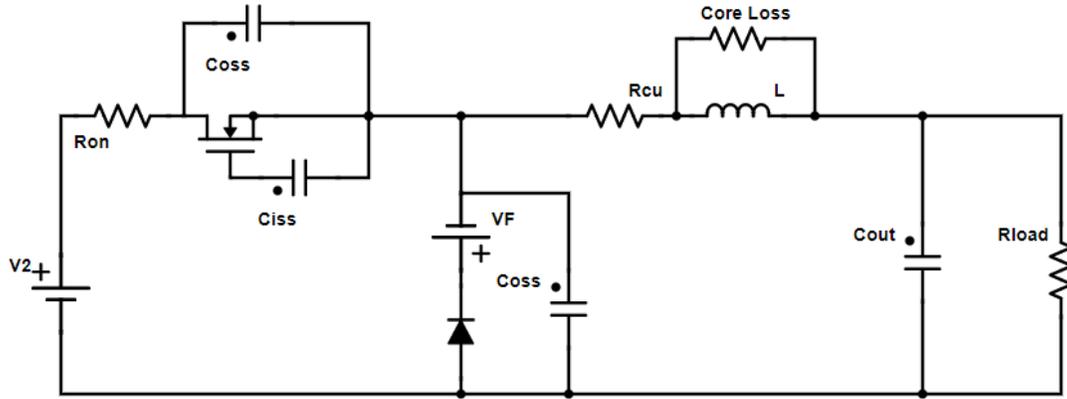

Asynchronous Buck Converter

Synchronous Synchronous switching with the use of another transistor can have lower losses, but requires some rise in complexity to drive the lower gate. Most discrete solutions can accomplish synchronous switching without adding additional components to the board, so it is usually the practical switching method.

Losses

Losses are the next most important design aspect after size. A flexible solution is above 90% efficient with compromises across large loads. The three main losses in power converters are conduction losses from resistance or voltage drop in the current path, switching losses from changing capacitances around the switching node, and core losses from the magnetic material operating at the switching frequency.

Synchronous Loss Sources Considered

Asynchronous Loss Sources Considered

Conduction losses include the on resistance of the transistors and the copper loss of the inductor winding. If the converter is Asynchronous than the bottom conduction loss is given by (P_D). RMS currents are used for all but the diode because the voltage across the diode is modeled as a constant forward voltage.

$$P_{on_{TOP}} = \frac{R_{on}I_{out}^2 V_{out}}{Vin}\left(1 + \frac{R_L^2}{3}\right)$$

Equation 15

$$P_{on_{BOTTOM}} = \frac{R_{on}I_{out}^2(V_{in}-V_{out})}{Vin}\left(1 + \frac{R_L^2}{3}\right)$$

Equation 16

$$P_{cu} = R_{cu}I_{out}^2\left(1 + \frac{R_L^2}{3}\right)$$

Equation 17

$$P_D = \frac{V_F I_{out}(V_{in}-V_{out})}{V_{in}}$$

Equation 18

Switching losses are based on the collapse of change when a capacitor across the switch is shorted by the switch closing. These capacitors include the capacitor from drain to source (Coss) called the switching loss itself and the capacitor from gate to source (Ciss – Crss) called the gating loss. When a capacitor is changed it holds the energy given in Equation 20. This energy is lost every time the capacitor is shorted by the switch. Additionally, it takes just as must energy to rechange the capacitor in the next cycle. With this energy being lost every switching event, power is just the energy lost time the events per second. There is a similar loss for series inductance for the switch opening, but these losses are usually minuscule. The bottom device is considered "Soft Switched" if the voltage is given time to naturally fall to zero before the switch is closed meaning that no change is waisted by shorting. Soft Switching is always achieved in the asynchronous case, but the time between the top switching opening to the bottom switch closing must be sufficient for the body diode of the bottom switch to ensure soft switching in the synchronous case. This time frame is called the dead time because no active switch is conducting to the switching node.

$$E_{cap} = \frac{1}{2}CV^2$$

Equation 20

$$P_{sw} = \frac{1}{2}C_{oss}V_{in}^2 f_{sw}$$

Equation 21

$$P_{gating} = C_{gs}V_g^2 f_{sw}$$

Equation 22

Core losses encompasses all the other losses that happen inside the magnetic material by operating it has high frequencies. The magnetic flux density (B) within the magnetic field loop has an AC component caused by the AC component of the current flowing through the coil. See Inductor Design section for more details.

$$P_{core} = P_V(f_{sw}, B_{ac})Displacement\ Volume_{core}$$
Equation 23

Thermals

While the circuit may not have the losses calculated above appear in the output current and voltage, they exist as heat within the individual contributors. Thermal design is all about moving the heat generated by losses away from its origin to the ambient environment. The temperature difference at a given location from ambient is a function of how well heat is transferred to ambient from that location. The temperatures of highest concern are at the IC die usually rated for 85 to 150C. Heat dissipation can be modeled as a circuit with a current source representing the device losses, resistors representing thermal resistance, and a voltage source representing ambient temperature above absolute zero. The temperature at the junction can be calculated with Equation 24.

Heat Transfer Circuit Model
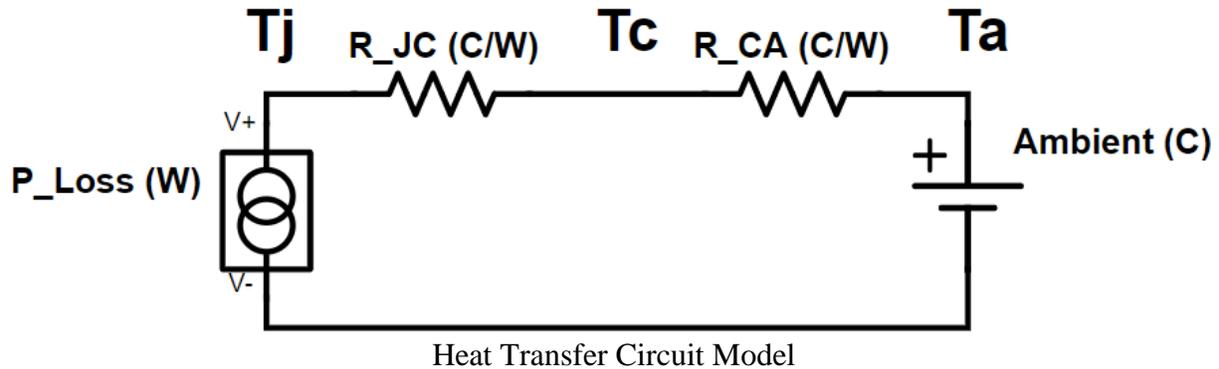
$$T_j = P_{loss}(R_{\theta jc} + R_{\theta ca}) + Ambient$$
Equation 24

The thermal resistances themselves can be calculated physically. Resistances between solids such as junction to case and case to PCB transfer heat through conduction with a length over area tradeoff much like electric conduction also featuring a thermal resistivity given by Equation 25. Transfer between a solid and a gas is accomplished through convection which relies on the area of contact and the gas conditions given by its Reynold number (hc) in Equation 26. Radiation emitting from a device can also transfer heat through a (T^4) relationship over an exposed area times the Boltzmann constant (k_B). The reflectivity or shininess of an exposed surface also effects how well it gives off radiation through an emissivity constant (ε) ranging from 0 to 1. Heatsinks can raise the surface area for confection and radiation transfers.

$$R_{\theta conduction} = \frac{\rho_\theta L}{A}$$
Equation 25

$$R_{\theta convection} = \frac{1}{h_c A}$$
Equation 26

$$Q_{radiation} = \varepsilon k_B A T^4$$
Equation 27

Printed Circuit Board Layout

Layout is implementing an idealized schematic, so the main goal of layout should be to stay as close to ideal as possible through the minimization of parasites. Traces have parasitic capacitance between all other metal. Traces will have lumped series resistance given by Equation 28, and parasitic inductance can be ballparked by Equation 29 and the following website: https://www.emisoftware.com/calculator/microstrip/

$$R_{trace} = \frac{\rho_{cu}L_{trace}}{W_{trace}H_{trace}}$$

Equation 28

$$L \approx \frac{\mu A}{d}$$

Equation 29

We want to minimize L in the switching loop, so the key is the make the (d) in Equation 29 be the height of the board or the light from one of the surfaces to the ground plane in a four-layer board. Another important loop is the gating loop. Placing the driver as close to the switching devices as possible is a general method. Estimating the parasitic inductance here can help determine the ringing we want to dampen at our transistors' gates as described in the Gate Driver selection.
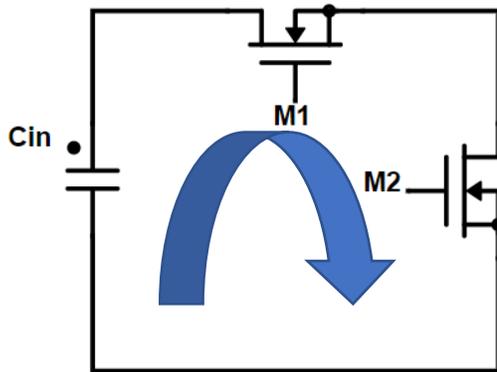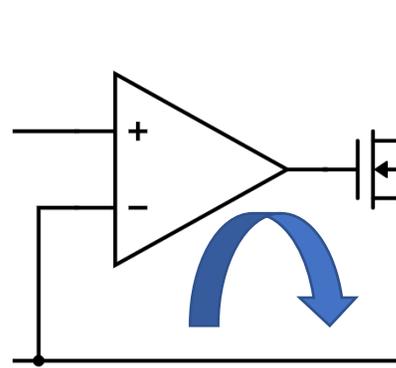
Switching Loop   Gating Loop

Layout Constants for 4 Layer FR4

$H_{1oz\,copper} = 35\mu m$

$H_{2oz\,copper} = 70\mu m$

$Min\ Feature\ Size = 0.3mm$

$Total\ board\ hight = 1.6mm$

$\varepsilon_{FR4} = 4$

$\rho_{Cu} = 1.68 * 10^{-8}\Omega m$

Transistor Selection

The transistors are the switching devices in the switch mode power supply name. Their on resistance and capacitances are key losses. Their package determines the largest thermal resistances on the board, and the package sets the length of the switching loop. Their gate voltage will also determine what class of PWM drivers can be used. The semiconductor market has produced a multitude of transistors all with different knobs turned in each of the above concerns to try to match the perfect application with the leading performance. Here is a short list of what devices are out there in the different Technologies:

Material	Manufacturers
Silicon (Si)	TI's NextFET
Gallium Nitride (GaN)	EPC, GaNSystems
Silicon Carbide (SiC)	Wolfspeed

Capacitor Selection

As shown in the operation, the output capacitor needs to handle the peak-to-peak inductor current while mitigating the voltage ripple at the output. Losses are usually low with ever shrinking equivalent series resistance (ESR) as the materials move towards Barium Titanate ceramics for small to medium capacitances and Aluminum polymers for large capacitances. Both technologies follow the trend toward lower voltages, so Aluminum Electrolytics still have their place with high voltage tolerances at the cost of size and lifetime. An invaluable tool in the industry is K-Sim from KEMET allowing the user to see how a given product will fair in our operating conditions: https://ksim3.kemet.com/

Gate Driver

To get the most out of a good switching device, it must be turned on and off quickly. Slow operation represents additional losses, lower effective duty ratio, and more switching harmonics. Gate drivers provide a low impedance path for current to quickly drain or source the gate charge needed to change the on state of the switch. This is the same as saying that the RC time constant is small as shown in the figure below using the Thevenin model of a direct versus driven gate. Another concern is referencing. The FET connecting the switching node to ground will always share the same ground as the gate driver, but the high side FET is referenced to the switching node which is moving between (Vin) and (GND) every switching event. The solution is to drive the top FET with a switch node referenced driver using a technique called bootstrapping. Bootstrapping makes a temporary supply for the top driver that becomes isolated from the rest of the gate driver once it is needed for the top switch. When it is not needed, the temporary source is replenished by the main driver supply.
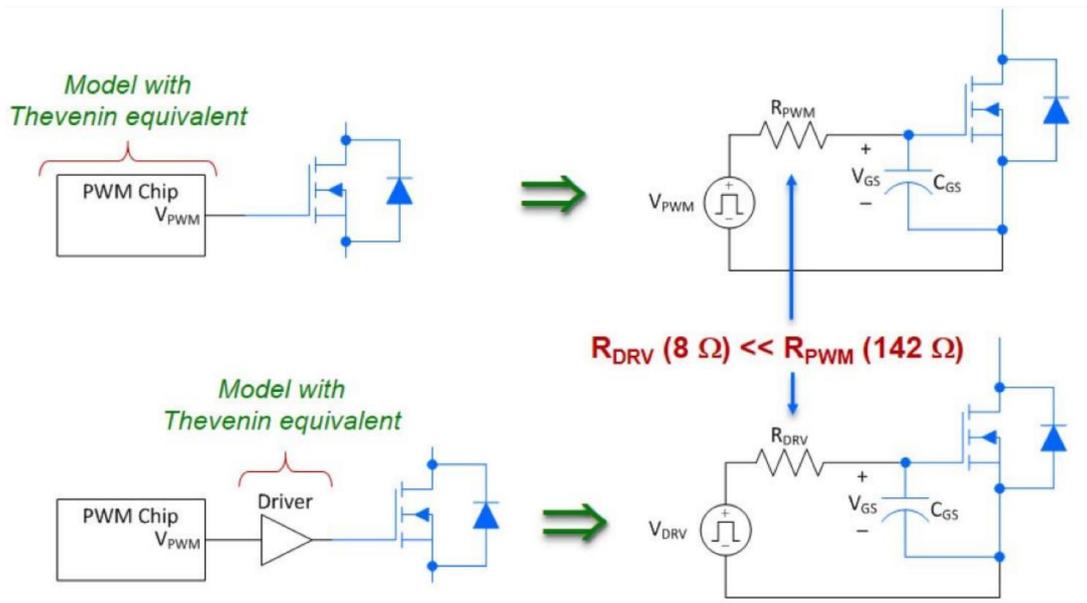
Direct vs. Driven FET Gate *Flynn Fall 2019*

Now that the FET can be switching quickly, we must ensure that the gate is unharmed during this fast operation. By removing the bulk of the impedance to the gate we have allowed the gate to source capacitance to possibly resonate with the inductance in our layout path for the switching loop. This can cause the gate voltage to overshoot the desired value and approach the breakdown voltage for the (Vgs) capacitor. A small amount of resistance can be reintroduced in series with the gate to ensure that the ringing at the gate is perfectly damped.

$$R_{series} = 2\sqrt{\frac{L}{C}} - R_g - R_{Driver_{MIN}}$$

Equation 30

Inductor Design

Inductors are passives that hold benefits for custom designs. Off the shelf potted inductors can be found at companies like CoilCraft using their power tool: https://www.coilcraft.com/en-us/tools/power-inductor-finder/#/search

A more practical inductor to make yourself is a gapped core inductor consisting of a core material, a geometry for that material, a gap with length (lg), and a coil to wrap around the core. With a high enough permeability, the core material will determine, unit volume core losses and saturating magnetic field density. Core loss is estimated using the empirical Steinmetz given by Equation 31 from a similar graph as the one given below for the core material 3F36 from FerroxCube. (Kf) is a constant with (α) and (β) as just the slope of the graph's log-log scale. While loss is determined by the changing field, saturation is avoided by keeping the peak (B) field under a reasonable tolerance of the rated maximum such as 75%.
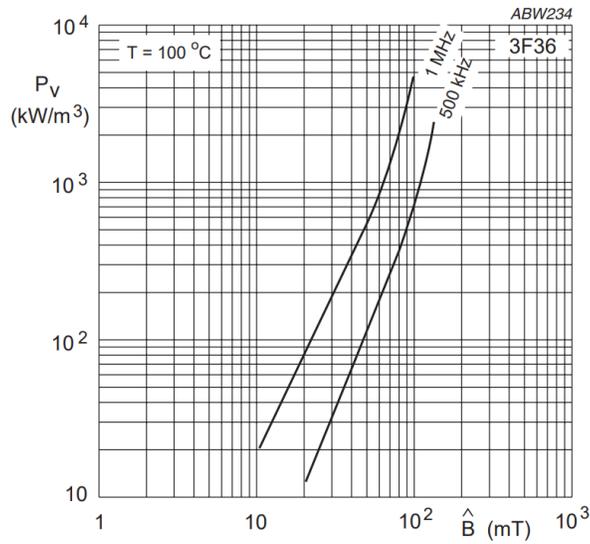
$$P_V = K_f B_{ac}^{\beta} f_{sw}^{\alpha}$$

Equation 31
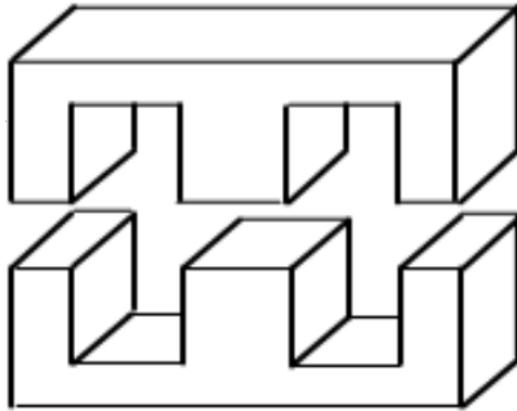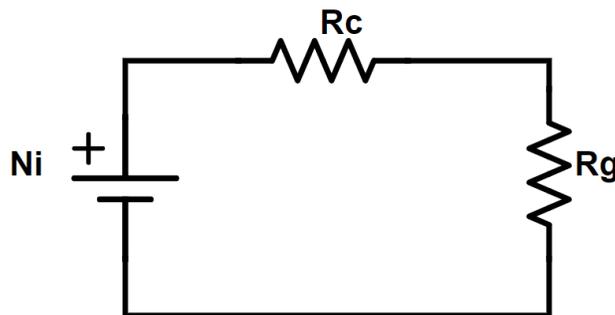
E Core   Wound E Core

Power Loss as a Function of Bac

Circuits can model the relationship between magnetic flux density and current just like electric circuits model current and voltage respectively. A magnetic material or gap will follow the analogy. Ohm's law can now be given for a quality called reluctance as opposed to resistance.

$$\mathcal{R} = \frac{l}{\mu A_{cross}}$$ Equation 32

Magnetic Circuit for a Gapped Core

The following two equations from this circuit model can be used to find (N) and (lg) for a selected geometry and material. Optimistically, you can fill half the space in the core ($A_{winging}$) with a long enough wire ($l_{winding}$) for the coil. The resistance for that winding is Equation 35.

$$B = \frac{\mu_g N I_L}{l_g}$$

<div align="right">Equation 33</div>

$$L = \frac{N^2}{\frac{l_g}{\mu_g A_C} + \frac{l_c}{\mu_c A_C}} \approx \frac{\mu_g N^2 A}{l_g}$$

<div align="right">Equation 34</div>

$$R_{cu} = \rho_{cu} \frac{2N l_{wingind}}{A_{wingind}}$$

<div align="right">Equation 35</div>

Small-Signal Modeling

A buck converter is a time dependent and roughly linear system, but we can make one assumption to find the LTI approximation. First, we need to write out the differential equation for both the state vectors, (I_L) and (V_c) for the positive and negative duty cycle. Then we can average the two phases together and separate each time varying term into its constant and varying pieces. Finally, assume that all varying terms multiplied by other varying term are insignificantly small. After that you can solve for (V_c) in terms of the small signal parameters representing each input variation's effect on the buck converter. The last step is to move everything over to the S-domain for classical controls design.

$$\phi_1: L\frac{dI_L}{dt} = V_{in} - V_{out} \qquad C\frac{dV_c}{dt} = I_L - \frac{V_C}{R} - I_O$$

<div align="right">Equation 36</div>

$$\phi_2: L\frac{dI_L}{dt} = -V_{out} \qquad C\frac{dV_c}{dt} = I_L - \frac{V_C}{R} - I_O$$

$$L\frac{dI_L}{dt} = D(V_{in} - V_{out}) + (1-D)(-V_{out}) = \boldsymbol{DV_{in} - V_{out}}$$

<div align="right">Equation 37</div>

$$C\frac{d\boldsymbol{V_c}}{dt} = \boldsymbol{I_L} - \frac{\boldsymbol{V_C}}{R} - \boldsymbol{I_O}$$

$$L\frac{d\widetilde{I_L}}{dt} = \boldsymbol{D}\widetilde{V_{in}} + \boldsymbol{V_{in}}\tilde{d} - \widetilde{V_{out}}$$

<div align="right">Equation 38</div>

$$C\frac{d\widetilde{V_C}}{dt} = \widetilde{I_L} - \frac{\widetilde{V_C}}{R} - \widetilde{I_O}$$

$$\frac{d^2\widetilde{V_C}}{dt^2} = \frac{\boldsymbol{D}}{LC}\widetilde{V_{in}} + \frac{\boldsymbol{V_{in}}}{LC}\tilde{d} - \frac{1}{C}\frac{d\widetilde{I_O}}{dt} - \frac{1}{RC}\frac{d\widetilde{V_C}}{dt} - \frac{1}{LC}\widetilde{V_C}$$
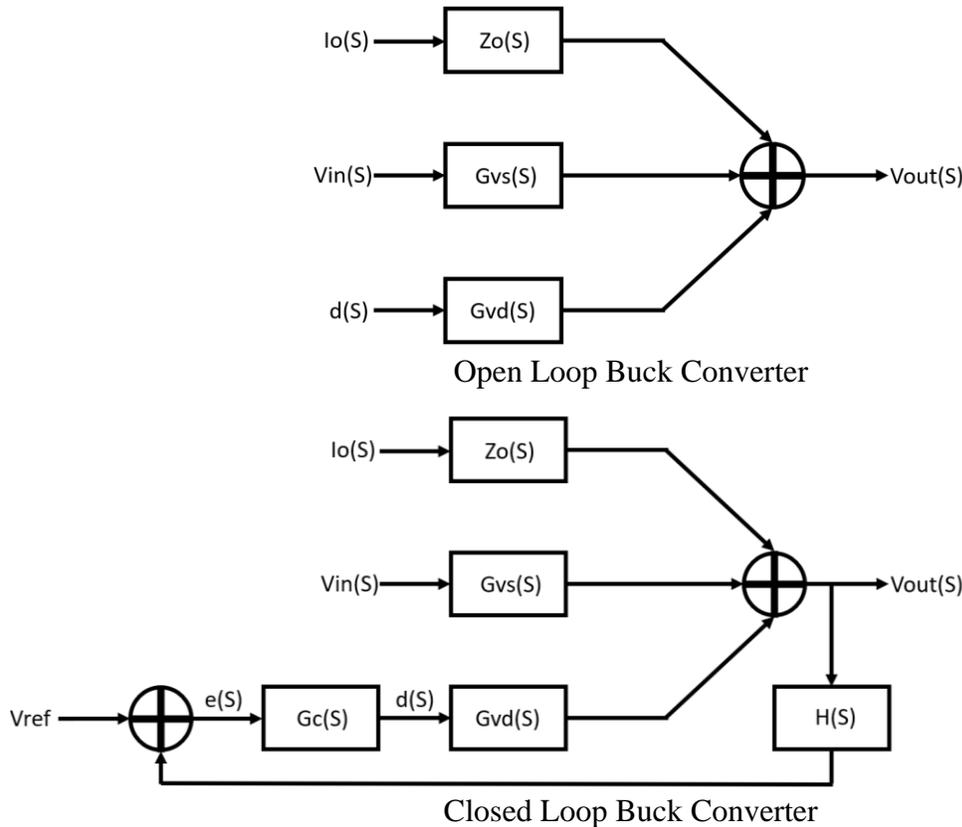
<div align="right">Equation 39</div>

$$\widetilde{V_C} = \frac{D/LC}{S^2 + \frac{1}{RC}S + \frac{1}{LC}}\widetilde{V_{in}} + \frac{V_{in}/LC}{S^2 + \frac{1}{RC}S + \frac{1}{LC}}\tilde{d} + \frac{-(1/C)S}{S^2 + \frac{1}{RC}S + \frac{1}{LC}}\widetilde{I_O}$$

<div align="right">Equation 40</div>

Each source of output variation is grouped into its own transfer term.

$$\widetilde{V_C} = G_{vs}\widetilde{V_{in}} + G_{vd}\tilde{d} + Z_o\widetilde{I_O}$$

<div align="right">Equation 41</div>

Control

The goal of control is to maintain the desired output voltage with known dynamic responses to each of the input variations found in the modeling above. The current open loop system is shown below. We want to close the duty cycle loop allowing the converter to self-regulate by changing the duty, so that no matter what happens to the output current or input voltage, the output voltage always mirrors a reference. The output is fed back with a scaling factor (H) then subtracted from the reference to create an error signal. (Gc) sets the dynamics of how that error signal changes the duty cycle feeding into (Gvd) to adjust the output accordingly.

Open Loop Buck Converter


Closed Loop Buck Converter

(Gvd) is a second order transfer, so an always stable (Gc) adds holes where the original system has poles to cancel them, and it has an integrator to force the gain to one as given by Equation 43. Phase is a constant -90 degrees. An additional pole can be added after the gain hits one to roll off the phase to a more ideal -120 degrees for a perfectly dampened control loop achieving the fastest settling output. Set (fc) to a tenth of (fsw) by changing (Kc) in the controller. This speed limit keeps the controller from trying to adjust the output during a single switching cycle.

$$T(S) = \frac{K_c\left(\frac{S}{\omega_{z1}}+1\right)\left(\frac{S}{\omega_{z2}}+1\right)}{S} * \frac{K_{ol}}{\left(\frac{S}{\omega_{p1}}+1\right)\left(\frac{S}{\omega_{p2}}+1\right)} = \frac{K_c K_{ol}}{S} \qquad \text{Equation 42}$$

$$2\pi f_c = \omega_c = K_c K_{ol} \qquad \text{Equation 43}$$

$$f_c \approx f_{sw}/10 \qquad \text{Equation 44}$$

New transfers can be defined for the closed loop system. The response to an input change is historically called audio-susceptibility (Acl), the output current response is now simply (Zcl), and (Vref) changes are processed by the command step.
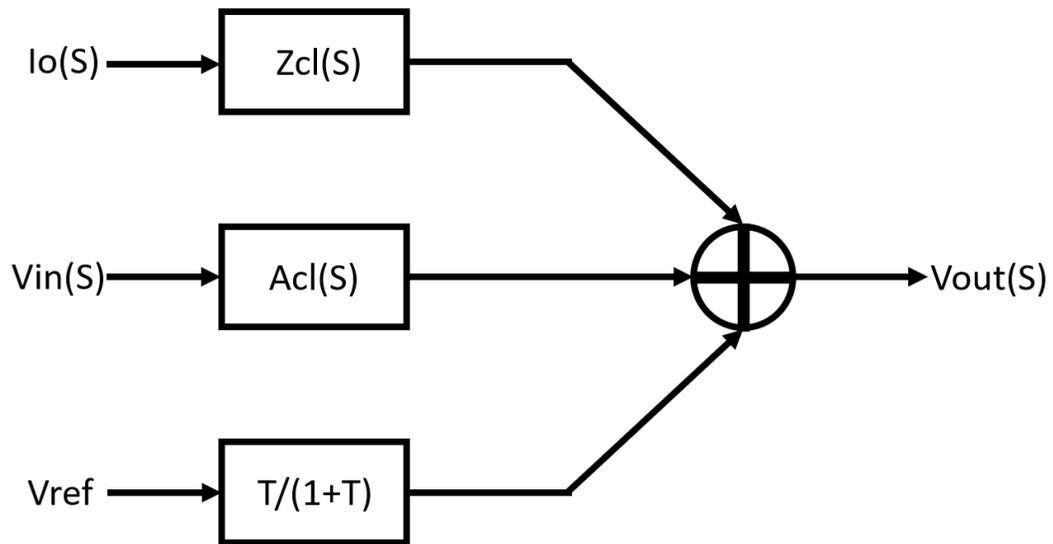
Closed loop Response to Output, Input, and Reference

$$Z_{CL} = \frac{Z_O}{1+T}$$ Equation 45

$$A_{CL} = \frac{G_{vs}}{1+T}$$ Equation 46