In this article we will go over the components, transfer functions, dynamics, and phase noise in Charge Pump Phase-Locked Loops (CPPLL) with materials from B. Razavi’s *RF Microelectronics* book and various papers. CPPLL are a subset of PLLs with a practical “all analog” implementation due to their locking over a large frequency range. The goal of a PLL is the synchronize the output oscillation to the input waveform scaled by a frequency and phase feedback factor. PLLs “Lock” or minimize the error between the input to output phase and the input to output frequency “Locking” both qualities. CPPLLs accomplish locking with the following blocks:

- Voltage Controlled Oscillator
- Phase/Frequency Detector
- Charge Pump
- Loop Filter
- Frequency Divider

**Voltage Controlled Oscillator (VCO)**

VCOs use an input voltage to control the frequency of an output. A change in phase can be accomplished by a variable frequency device using Equation 1. Looking at a periodic signal like Equation 2, if frequency can be changed by a voltage control signal Vcont, then the new waveform can be given as Equation 3. Vcont can be used to achieve any desired phase while the DC value of Vcont represents a frequency selection.

\[
\phi = \int f \, dt \quad \text{Equation 1}
\]

\[
V_{out} = V_o \cos(2\pi f_o t + \phi_o) \quad \text{Equation 2}
\]

\[
V_{out} = V_o \cos(2\pi f_o t + \int K_{VCO} V_{cont} \, dt) \quad \text{Equation 3}
\]
The two most common VCOs in integrated circuits are ring oscillators and LC oscillators. Rings take advantage of technology scaling in power and area, but they suffer from high phase noise, random frequency variability. LCs have much lower phase noise, but they require careful modeling of otherwise uncommon passives on chip, varactors and inductors.

**Phase/Frequency Detector (PFD)**

PFD determine which of two inputs has the slower frequency and/or lagging phase. An alternative approach is to detect just the phase difference, but this leads a static phase offset to establish the constant component of Vcont mentioned in the VCO section. The full range of the VCO also becomes the locking range with a phase and frequency detector as a phase only detector will eventually encounter a periodic phase difference preventing frequency locking.
Charge Pump (CP)
The above implementation of the PFD produces pulses as its output to represent the frequency commands to the VCO. The VCO would prefer to respond to a continuous signal, so the pulses are turned into a push or pull of current in or out of a capacitor storing Vcont. The discrete voltage pulses, Equation 4 occurring every reference cycle can be estimated by a continuous transfer function with the PFD, Equation 5 from the input phase difference to the control voltage.

\[
\Delta V = \frac{I_p \Delta T}{C_1} \quad \text{Equation 4}
\]

\[
\frac{V_{\text{cont}}}{\Delta \phi} = \frac{I_p}{2\pi C_1 s} \quad \text{Equation 5}
\]

Loop Filter (LF)
The LF suppresses the nonideal spurs or pulses from previous stages and provides a convenient location to design loop dynamics. The capacitor C\textsubscript{1} from the charge pump is the central component of the loop filter. The dynamic not set so far is the dampening of an otherwise second order system. Adding a resistor in series with C\textsubscript{1} gives us proportional to go along with our integral control of Vcont. A key nonideality of the PFD implementation from earlier is that the end of cycle reset signal turns on both push and pull currents for a few gate cycles (T\textsubscript{reset}). An imbalance in push and pull currents translates to a constant phase offset between the input and output of the PLL, Equation 6. An additional imperfection resulting from the reset phase is the skew (T\textsubscript{skew}) between the current pulses causes a jump on Vcont. By adding a smaller secondary capacitor, the peak-to-peak Vcont variation reduces to Equation 7. A fifth of C\textsubscript{1} can be added without significantly impacting loop dynamics. Equation 9 gives the transfer function for the PDF/CP pair.
\[ \Delta \phi_{\text{mismatch}} = 2\pi f_0 \frac{I_{\text{Up}} - I_{\text{Down}}}{I_{\text{Down}}} T_{\text{reset}} \]  \hspace{2cm} \text{Equation 6}

\[ V_{\text{cont skew \_ p-p}} = \frac{l_p}{C_1} T_{\text{skew}} \]  \hspace{2cm} \text{Equation 7}

\[ C_2 = 0.2C_1 \]  \hspace{2cm} \text{Equation 8}

\[ \frac{V_{\text{cont}}}{\Delta \phi} = \frac{l_p}{2\pi} \left( \frac{1}{C_1 S} + R_1 \right) \]  \hspace{2cm} \text{Equation 9}

**Frequency Divider**

Frequency Dividers translate the high frequency fast phase output for comparison to the low frequency slow phase reference. A key feature of PLLs is their ability to produce frequencies higher than their input. Dividers allow the PFD to behave as if the input and output are the same frequency. Dividers are implemented as one-bit counters that are greatly simplified by the lack of digits they must maintain. The simplest is a divide by two implemented with a single flip-flop. The inverting output is tied to the flip-flop’s input and the PLL output is used as the flip-flop’s clock. A cascade of small dividers is used to achieve large ratios.
Transfer Functions and Dynamics

Performance is set by dynamics and how noise in the system translates to the output phase. Closed loop CPPLLs can be modeled as damped 2\textsuperscript{nd} order systems. The undamped CP acts as an ideal integrator summing the PFD pulses, and the VCO turns that integration into frequency, the integration of phase. The dampening resistor in the loop filter pushes the closed-loop poles apart and sets the dynamics for a given bandwidth as shown by the equations below.

![CPPLL Linear Model Diagram]

**Loop Transfer**

\[
T(S) = \frac{I_p}{2\pi} \left( \frac{1}{C_1 S} + R_1 \right) \frac{K_{VCO}}{S} \frac{1}{M}
\]

Equation 10

**Closed Loop Transfer**

\[
H(S) = \frac{I_p}{2\pi} \left( \frac{1}{C_1 S} + R_1 \right) \frac{K_{VCO}}{S} \frac{1}{M} + 1 = \frac{I_p K_{VCO} R_1}{2\pi} \frac{1}{S^2} + \frac{I_p K_{VCO}}{2\pi C_1} + \frac{I_p K_{VCO}}{2\pi C_1} = M \frac{2\zeta \omega_n S + \omega_n^2}{S^2 + 2\zeta \omega_n S + \omega_n^2}
\]

Equation 11

**Loop Dynamics**

\[
\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi M C_1}}
\]

Equation 12

\[
\zeta = \frac{R_1}{2} \sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}}
\]

Equation 13

The dampening sets the distance between the two poles of the closed-loop transfer function.

\[
\omega_z = -\frac{\omega_n}{2\zeta}
\]

Equation 14

\[
\omega_{p1,2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n
\]

Equation 15

If \(\zeta = 1\) then the loop has 60\textdegree of phase margin and,

\[
\omega_z = -\frac{\omega_n}{2}
\]

Equation 16

\[
\omega_{p1} = \omega_{p2} - \omega_n
\]

Equation 17
The -3dB low-pass corner of the input phase noise is found by setting $|H(j\omega)|$ equal to $1/\sqrt{2}$.

$$\omega_{-3dB} = \omega_n\sqrt{1 + 2\zeta^2 \sqrt{(1 + 2\zeta^2)^2 + 1}}$$  \hspace{1cm} \text{Equation 18}

The open-loop unity bandwidth can be found by setting $|T(j\omega)|$ equal to 1.

$$\omega_u = \omega_n\sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}$$  \hspace{1cm} \text{Equation 19}

For $\zeta = 1$ this leaves,

$$\omega_{-3dB} = 2.5\omega_n$$  \hspace{1cm} \text{Equation 20}

$$\omega_u = 2.1\omega_n$$  \hspace{1cm} \text{Equation 21}

To ensure the continuous approximation for the phase detection-charge pump, $\omega_u$ should be chosen roughly one tenth of $\omega_{Ref}$.

\[
\begin{array}{c}
|H| \\
\hline
\hline
1 & 1 \\
\hline
0 & 0 \\
\hline
\end{array}
\]

\[\begin{array}{c}
\omega_n \quad \omega_n \quad \omega_n \sqrt{2}\omega_n \\
\hline
2 & \omega_n & \omega_n \sqrt{2}\omega_n \\
\hline
\end{array}\]

CPPLL Closed-Loop Transfer Function for $\zeta = 1$ and $M = 1$ \textit{Razavi}

\textbf{Noise Transfers}

While phase noise from the input is low-passed, phase noise originating from the VCO is high-passed, and voltage noise that modulates Vcont leading to phase noise is band-passed. Phase Noise from the divider has the equivalent transfer as the reference phase noise to the output.

$$\frac{\Phi_{Out}}{\Phi_{Ref}} = \frac{\Phi_{Out}}{\Phi_{Div}} = M\frac{2\zeta\omega_nS+\omega_n^2}{S^2+2\zeta\omega_nS+\omega_n^2} \sim LP$$  \hspace{1cm} \text{Equation 22}

$$\frac{\Phi_{Out}}{\Phi_{n,VCO}} = \frac{S^2}{S^2+2\zeta\omega_nS+\omega_n^2} \sim HP$$  \hspace{1cm} \text{Equation 23}

$$\frac{\Phi_{Out}}{\Phi_{n,Cont}} = \frac{K_{VCO}S}{S^2+2\zeta\omega_nS+\omega_n^2} \sim BP$$  \hspace{1cm} \text{Equation 24}
Phase Noise and Jitter

The previous section gave the speed and stability of the PLL, but a key performance metric is how “clean” the output frequency is when considering random and deterministic variations in phase/frequency. While deterministic variations are caused by supply ripple, charge pump ripple, and fractional division (in synthesizers), random variations are determined as phase noise in frequency domain and jitter in time domain.

Phase Noise Intuition

A waveform with variable phase has a different frequency. This can be seen by separating the phase into its constant and time varying component. The first-order time varying component produces a different frequency cosine. If the time varying phase is random than we would expect the frequency of the waveform to also be randomly higher or lower than its average as well.

\[ V_{out} = V_o \cos(2\pi f_o t + \phi(t) + \phi_{cont}) \]
\[ = V_o \cos(2\pi f_o t + \phi_{linear} t + \phi_{const}) \]
\[ = V_o \cos([2\pi f_o + \phi_{linear}] t + \phi_{const}) \]

Looking back at the VCO transfer function, Equation 3, if Vcont is a sinusoidal source than the output can be estimated by Equation 28 as the unmodulated carrier waveform with sidebands. The way we look at these sidebands is relative to the carrier, Equation 29. This shows that the sidebands get attenuated by one over their distance from the carrier, which is just the original frequency disturbance, \( \omega_m \).

\[ V_{out} = V_o \cos(2\pi f_o t + \int K_{VC} V_m \cos(\omega_m t) dt) \]
\[ V_{out} = V_o \cos(2\pi f_o t + \frac{K_{VCO} V_m}{\omega_m} \sin(\omega_m t)) \]
\[ V_{out} = V_o \cos(2\pi f_o t) + V_o \frac{K_{VCO} V_m}{2\omega_m} \{ \cos([\omega_o + \omega_m] t) + \cos([\omega_o - \omega_m] t) \} \]
\[ P_{SBC} = 20 \log \left( \frac{K_{VCO} V_m}{2\omega_m} \right) \]

Calculating Phase Noise

A general model of finding the output spectrum due to noise sources in an oscillator requires 6 steps:

1. Identify the uncorrelated noise sources, \( v_{n0} \)
2. Find their Impulse Sensitivity Functions, \( \Gamma(\omega_o t) \)
3. Find their cyclostationary noise, \( v_{n0} \alpha(t) \)
4. Find the maximum output swing, \( V_{out pp} \)
5. Using 1-4 calculate phase noise, \( S_{\phi n}(\omega) \)
6. Translate phase noise to the carrier voltage spectrum, \( S_{out}(\omega_o \pm \omega) \)
Electronic noise $v_{no}$ is converted to phase noise through a linear time-varying (LTV) process. The Impulse Sensitivity Function (ISF) $\Gamma(\omega_0 t)$ describes how a spontaneous and brief change in the waveform effects its phase. We can estimate the ISF using the derivative of the normalized waveform. In the LC figure above. The current impulse changes the voltage on the capacitor as the inductor is high impedance and the capacitor is low impedance for an infinitely fast pulse. The ISF will be zero when the current pulse does not change the voltage to current ratio in the system. This is when the capacitor is at its peak voltage. The maximum ISF will then happen when the capacitor has zero voltage across it. The effect of such a jump in voltage must be weighted by the maximum existing voltage $V_{out_{pp}}$ because the ISF is calculated for a normalized waveform.

Another effect to consider is the amount of noise being generated as a function of the output swing. Since sources like MOSFET channel thermal noise are dependent on the bias of the circuit, the noise contribution for a given point in the ISF must be considered as cyclostationary noise, the effective noise over the period. Equation 30 gives an expression for phase noise using the above considerations. The output spectrum mimics the phase spectrum centered at the carrier.

$$\phi_n = \int \left( \Gamma(\omega_0 \tau) \frac{v_{no} \alpha(\tau)}{V_{out_{pp}}} \right) d\tau$$  \hspace{1cm} \text{Equation 30}

**Cross Coupled Differential LC Oscillator Phase Noise**

LC oscillators are the low phase noise solution for VCOs. $1/f$ noise translation from the cross coupled pair can be avoided by keeping the devices in saturation. An additional $1/f$ contribution can be avoided by introducing a high impedance port at harmonics of the oscillation frequency. The latter eliminates the tail noise contribution as well.

$$S_{\phi_n} = \left( \frac{\sqrt{2}}{2} + 1 \right) \frac{2 \pi K T}{I_{SSV_0}} \left( \frac{f_0}{2Qf} \right)^2$$  \hspace{1cm} \text{Equation 31}

**N Stage Ring Oscillator Phase Noise**

Ring oscillators are the low area and fast characterization solution for VCOs. $1/f$ noise translation can be reduced by tuning NMOS to PMOS ratio. Equation 32 and 33 estimate $1/f^2$ and $1/f^3$ regions of phase noise.

$$S_{\phi_n,1/f^2} = \frac{1}{2I_B} \left( S_{thermal,NMOS} + S_{thermal,PMOS} \right) \left( \frac{f_0}{f} \right)^2$$  \hspace{1cm} \text{Equation 32}

$$S_{\phi_n,1/f^3} = \frac{1}{4NI_B^2} \left( S_{flicker,NMOS} + S_{flicker,PMOS} \right) \left( \frac{f_0}{f} \right)^2$$  \hspace{1cm} \text{Equation 33}
CPPLL Phase Noise
To analyze the output phase noise of a closed loop PLL, we must sum the contributions from each source of phase noise weighed by its appropriate transfer function squared. A noisy supply such as flicker in the integrated LDO can also translate to a significant phase noise. Equation 34 places the phase noise sources in their order of expected contribution from Equations 22-24. The shaping of the VCO phase is a primary function of the PLL with a sharper rejection in higher bandwidth loops. The reference contribution is scaled by the divider factor and reduced by lower bandwidth loops. The resistor in the loop filter can result in a higher peak phase noise at the closed loop 3dB bandwidth.

\[
\phi_n = \left| \frac{s^2}{s^2+2\zeta_\omega n s+\omega_n^2} \right|^2 \phi_{n,\text{VCO}}^2 + M^2 \left| \frac{2\zeta_\omega n s+\omega_n^2}{s^2+2\zeta_\omega n s+\omega_n^2} \right|^2 \phi_{n,\text{Ref}}^2 + \left| \frac{K_{\text{VCO}} s}{s^2+2\zeta_\omega n s+\omega_n^2} \right|^2 V_{n,R1}^2 \tag{34}
\]

Jitter
Random Jitter is the variation of the period due to phase noise. Parseval’s Theorem can relate the time and frequency uncertainty through Equation 35. The factor of $1/\omega_o$ gives the jitter in seconds rather than radians.

\[
J_{\text{rms}} = \frac{1}{\omega_o} \sqrt{\phi_n^2} = \frac{1}{\omega_o} \int S_{\phi_n}(f) \, df \tag{35}
\]

Jitter can also be defined from one cycle to the next as cycle-to-cycle jitter in Equation 36. $f$ in the equation represents the offset frequency that $S_{\phi_n}(f)$ is measured at. The random departure from the average period is given as the period jitter in Equation 37.

\[
J_{\text{CC,rms}} = \frac{1}{\omega_o} \sqrt{\frac{8\pi^2 f^2}{f_o} S_{\phi_n}(f)} \tag{36}
\]

\[
J_{\text{C,rms}} = \frac{J_{\text{CC,rms}}}{\sqrt{2}} \tag{37}
\]

Deterministic Jitter
Not all unwanted frequency variations are random. The deterministic changes in period can be attributed to voltage ripple from the switching power supply modulating the phase and charge pump current, or the PFD reset pulses. On chip LDOs supply PLLs in order to mitigate VDD noise and ripple. Additional PDF logic can be added to shorten the reset pulses. From the sidebands in Equation 29, the peak-to-peak deterministic jitter can be calculated using Equation 38.

\[
J_{\text{pk-pk}} = \frac{4}{\omega_o V_o} A_{\text{sideband}} \tag{38}
\]