Current Mirror Basics

Jin Gao

Fig. 1: Current Mirror

Concept

In analog IC design, current mirror structure is one of the most used concepts. It is commonly used to replicate current from one branch of the circuit to another, but it can also be used as a biasing network or as a “pseudo” current source. In Fig. 1, M1 and M2 are MOSFETs with the same area process, and \( V_{GS} \), \( I_{REF} \) is the current we are trying to mirror and \( I_{out} \) is the mirrored current. Since the gate of M1 and M2 are shorted, both MOSFETs experience the same \( V_{OV} \), \( V_{GS} - V_{TH} \). Operation of current mirrors is based on the governing equation of MOSFET current in saturation. Based on the \( I_{d, sat} \), one can see that the current is modeled by the square of overdrive voltage, \( V_{OV} = V_{GS} - V_{TH} \). The first-order operation of a current mirror can be realized as two MOSFETs with the same process and overdrive voltage, then the current flowing through the MOSFETs should be equivalent if they have the same width and length as shown in Eq. 3, assuming negligible channel length modulation. However, this may not always be the case in application. Some non-idealities such as process variation, \( V_{DS} \) difference, and \( V_{TH} \) mismatch may cause current mismatches.

**Governing Equations:**

**NMOS**

\[
I_{d, sat} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \quad \text{(eq. 1)}
\]

**PMOS**

\[
I_{d, sat} = \frac{1}{2} \mu C_{ox} \frac{W}{L} |V_{GS} - V_{TH}|^2 (1 + \lambda V_{DS}) \quad \text{(eq. 2)}
\]
\[
\frac{I_{\text{OUT}}}{I_{\text{REF}}} = \frac{\frac{1}{2} \mu C_{ox} W_2 (V_{GS} - V_{TH})^2}{\frac{1}{2} \mu C_{ox} W_1 (V_{GS} - V_{TH})^2} = \frac{w_2}{w_1} \quad \text{(eq.3)}
\]

**Mismatches**

Assume \( \beta = \mu C_{ox} \frac{W}{L} \)

\[
gm = \frac{2I_D}{V_{ov}}
\]

\[
\Delta I_{D,\beta} = \frac{\Delta \beta}{2} (V_{ov})^2 \quad \text{(eq.4)}
\]

\[
\Delta I_{D,vth} \approx -\Delta V_{TH} \beta V_{ov}^2 \quad \text{(eq.5)}
\]

\[
\frac{\Delta I_D}{I_D} \approx \frac{\Delta I_{D,\beta} + \Delta I_{D,vth}}{I_D} = \frac{\Delta \beta}{\beta} - \frac{gm}{I_D} \Delta V_{TH} \quad \text{(eq.6)}
\]

Mismatches in current mirror topology is referred to as the current difference between the reference current, \( I_{\text{REF}} \) and the output current, \( I_{\text{OUT}} \). The causes of current mismatches can be summarized into the following three categories: Process Variation, threshold voltage mismatches \( (V_{th}) \), and drain to source voltage difference \( (V_{DS}) \).

**Process Variations**

A common variation in the fabrication process is the mismatch in geometry of each MOSFETs. Due to the limitation of photolithography, the designed geometry may not be reflected on the actual etching on the wafer. The oxide thickness, width, and length of each MOSFET varies from die to die and wafer to wafer. This issue can be somewhat alleviated by good layout techniques to reduce local variation and by having larger device area. Hence, this is one of the many reasons why the process nodes for analog design are usually larger than that of digital circuits. Even though ways to reduce this variation are limited but it is still critical to understand where the mismatch originates. Mathematically, variation can be seen in Eq. 4 when \( \beta \) changes as it embodies all the physical parameters in the \( I_D \) square model.
Threshold Voltage Difference

Another source of current mismatch in current mirror is the threshold voltage difference, $V_{TH}$. A change in $V_{TH}$ directly impact how saturated the devices is. Eq. 5 shows that changes in $V_{TH}$ result in scaled change in $I_D$. This difference in threshold voltage is a result of body effect and non-idealities in doping concentration on the substrate and wells. In addition to intrinsic parameter, a variation in threshold voltage can also be realized as difference in effective $V_{GS}$. $V_{GS}$ may differ for each device with the presence of parasitic resistance along the interconnects.

\[
\nu'_t = 2\phi_0 + \frac{2\varepsilon_{Si}qN_A^2\phi_0}{C_{ox}} + \nu_{fb}
\]

where
\[
\phi_b = \frac{kT}{q} \ln \left( \frac{N_A}{N_f} \right)
\]

(Eq. 7)

Drain to Source voltage Difference

Ideally, $V_{DS}$ does not have an impact on device biasing point; however, due to channel length modulation. The drain current $I_{DS}$ varies with change in drain to source voltage across the device. As seen in Eq. 2 and the Fig. 3, the channel length modulation is reflected as the additional slope $\lambda$ after the device is in saturation. This phenomenon is observed often in short channel devices and becomes more obvious as the as channel length goes under 180nm.

Implementation and reducing the impact of mismatches

Some common techniques exist to reduce the impact of current mismatch in current mirror topologies, and they are not limited to the following examples.
Layout

One way to reduce mismatch in a same die is to place all the mirror devices in close proximity. Even though there may still be some variation between different die to die, this will reduce the local variation within the same die. For instance, in applications using current mirror scaling as discussed in the later section, the devices may lay in a common centroid pattern if the devices are sized differently.

![Simple Current Mirror](image)

**Fig. 4: Common Centroid Pattern**

Threshold Voltage

To reduce the impact of threshold voltage, the designer can choose a higher $V_{DS}$ voltage. As seen in the following figure, if the short channel effect is not pronounced, the variation in current may be limited. Reducing $g_{m/id}$ of that devices can lower the impact of $\Delta V_{TH}$ as shown in Eq. 6. Additionally, to reduce $g_{m/id}$, the overdrive voltage can be increased meaning bias the gate with greater potential in respect to the threshold voltage.
Fig. 5: $V_{DS}$ vs $I_{DS}$

**Drain to Source Voltage Variation**

To reduce the $V_{DS}$ variation, the designer can choose a longer length for the device. Depending on the process, the length can be chosen to be in the order of few microns or scaled of the minimum length. For details on how length can be approximated based on matching accuracy, please visit the statical variation section of reference [4]. Another technique is to implement a cascaded current mirror. By having a cascode, the $V_{DS}$ of Q2 will follow $V_{DS}$ of Q1, so the current mirror will significantly reduce the $V_{DS}$ difference between Q1 and Q2. Intuitively, if voltage at D2 were to increase causing an increase in the output current $I_O$, the $V_{GS}$ of Q4 will reduce limiting the current that Q2 is trying to increase. This way $I_O$ will be kept very close to the $I_{ref}$ in a small feedback loop. In addition, a cascoded device has high output impedance $\sim gm_{ro}ro^2$ making the mirror current acting more like an ideal current source. One downside of cascoded device is the voltage headroom. In order for Q4 and Q2 to be in saturation, the output voltage must be at least $2V_{GS} - V_{TH}$ or $2V_{DS,SAT} + V_{TH}$. As a rule of thumb in cascode mirrors, it is the best to size Q2 and Q1 as long channels.
Applications

Here are some examples of current mirror application:

*Scale $W_2/W_1$ to save power.*

In typical current mirror design, $W_2/W_1$ are not always 1:1. Since the gate voltage of diode-tied (Gate tied to drain) MOSFET is biased with $I_{REF}$, this will create a voltage level for the output branch to mirror and the ratio $W_2/W_1$ can be easily changed to save power. For example, if the required $I_{OUT}$ is 5 mA, instead of also driving the reference branch with $I_{REF} = 5$ mA, we can simply reduce $I_{REF}$ to 1 mA and change the $W_2/W_1$ ratio to 5:1 while keeping the length identical. This way $I_{OUT}$ is 5 mA with $I_{REF}$ only to be 1 mA to save power on the reference branch, and vice versa if you want a smaller $I_{OUT}$; however, as the ratio increases, the mismatch also increases. Typically a mirror ratio <10 is generally acceptable.
Fig. 7: Scaling Mirrored Current

*Distribute Mirror reference current to multiple output branches*

A single reference branch can also be used to mirror multiple branches as the circuit may need, and the mirrored branch can be used to mirror more branches; However, do note that the more you mirror, the greater the error may show in current matching.

Fig. 8: Current Mirror Distribution

*PMOS Current Mirror*

PMOS can also be used for mirroring. The only structure difference between PMOS mirroring and NMOS mirroring is the placement of $I_{REF}$ to source current or sink current. Both PMOS and NMOS can be used to mirror currents in the same topology as well depending on the application, shown in Fig.8. The implementation of $I_{REF}$ is not discussed in this document. There are many ways to implement $I_{REF}$, please refer to other documents for detail.
Fig. 9: PMOS Current Mirror
References


