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Chip-Package Interaction and Crackstop Study for Cu/Ultra low-k Interconnects

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Abstract. In this paper, the thermo-mechanical reliability of Cu/ultra low-k interconnects under chip to package interaction was investigated using finite element modeling and modified edge liftoff test (MELT). The crack propagation behavior in the low-k interconnect was simulated based on the crack tip opening displacement method (CTOD) and the maximum hoop stress criterion. In a six-level Cu/low-k interconnect model, the crack was found to grow from interconnect towards the Si substrate driven by shear stress and the calculated energy release rate (ERR) increases as crack grows. Structure reinforcement such as crackstops was demonstrated to be very effective in preserving the low-k interconnects integrity by reducing the crack driving force and increasing the fracture resistance if properly designed.

Keywords: Cu interconnects, reliability testing, crackstop, ultra low-k, chip package interaction.

INTRODUCTION

The exponential growth in device density requires continuous scaling of the interconnect structure for high-performance microprocessor chips. This leads to the implementation of new material, process and design for interconnect and packaging structures. The current effort of the semiconductor industry is focused on implementing ultra-low k (ULK) dielectric material with $k < 2.5$ into Cu interconnects to reduce the RC delay [1]. The weak mechanical properties of the ULK dielectrics and the increase in the interconnect level raise serious reliability concern for Cu/ultra low k interconnects. Interfacial delamination caused by chip-packaging interaction (CPI) is commonly observed in low k interconnects after die assembly into a flip-chip package [2,3]. A previous study revealed that the CPI-induced crack driving forces for interfacial delamination can increase substantially when the dielectric material is switched from fully dense low-k to ultra low-k materials as shown in Fig. 1 [4,5]. The effect was found to depend more on the elastic modulus, E, of the low-k material than the coefficient of thermal expansion (CTE).

In this paper, we extended the study of CPI to a 6 level Cu/low-k structure and calculated the crack propagation path using a CTOD method based on a maximum hoop stress criterion. Local crack stops were added into the model and their effect on crack propagation was studied. Finally, the fracture behavior of Cu/low-k interconnect was measured using the MELT test and the effect of crack stop structures was investigated. The reliability impact on ULK interconnects and their design rules for 45nm technology and beyond will be discussed.

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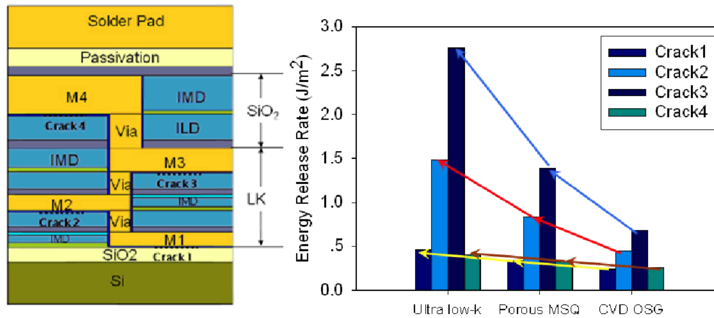

Fig. 1. ERR comparison between different low-k dielectrics under CPI [4]

SIMULATION

Sub-modeling technique

Multi-level sub-modeling technique was employed in this study in order to bridge the gap in feature size between the package and the chip [2-5]. We first developed a 2D FEA model based on a 3-level sub-modeling technique as shown in Fig.2. Level 1 is the package level for investigating the overall thermal deformation for the flip-chip package. Simulation results for this package level were verified with experimental results obtained from moiré interferometry. Level 2 is a sub-model with much finer meshes and focus on the critical solder bump region at the outermost chip corner. Level 3 contains detailed features for the interconnect structure with six metal levels. In this structure, the pitch and line dimensions in the first two metal levels (M1 and M2) are doubled in the third level (M3) while the fourth level (M4) is 1.5x the dimension of M3. This simulates approximately the hierarchical levels in real interconnect structures. Crack tip opening displacement method and the maximum hoop stress criterion were employed to study the crack propagation behavior in low-k interconnect. [6,7,8]

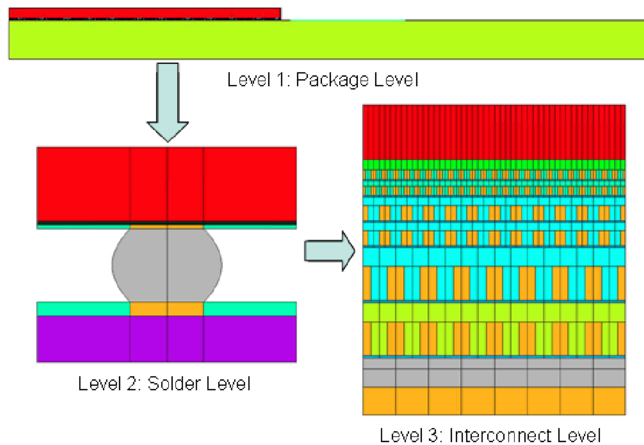

Fig. 2. Three sub-level interconnect model for crack propagation studies

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EXPERIMENT

Modified Edge Liftoff Test (m-ELT) was used to determine the effect of fracture toughness due to the implementation of crack-stop structures into low k interconnects. To prepare the specimen, a thick layer of epoxy was deposited on top of Si wafer and then cured for one hour at 177oC (Fig. 3). After curing, the sample was diced into 1 cm x 1 cm coupons. These diced specimens were placed in a cooling chamber where debonding can be observed upon cooling with liquid nitrogen. The temperature at which debonding occurred was recorded and the corresponding residual stress can be extrapolated using a calibrated residual stress vs. temperature curve. The strain energy release rate can be calculated by Eq. 1 [9,10], where σ_e is the residual stress in the epoxy coating layer; h is is the epoxy thickness and E and v are Yong's modulus and Poisson's ratio.

Fig. 3. Schematics of m-ELT sample

$$G_c = \frac{\sigma_e^2(T)\cdot h}{2\overline{E}_{film}}$$

$$\overline{E}_{film} = \frac{E_{film}}{1-\nu^2} \qquad \text{Eq. (1)}$$

RESULTS AND DISCUSSION

Crack Propagation and Crack Stop

An example of crack propagation in a real interconnect structure due to CPI is shown in Fig. 4. In general, the crack propagates along a path of maximum G/Γ, the ratio between the energy release rate and the fracture toughness [7]. Therefore, the crack propagation not only seeks a path with the largest energy release rate, but also favors a path with the lowest fracture toughness, either interfacial or cohesive. Depending on the local material combination and geometry, an interfacial crack may kink out of the interface, causing cohesive fracture of low-k materials. As shown in Fig.4, the crack propagated from the upper levels to the lower levels, eventually causing failure by die cracking [11]. Due to the complexity in the materials and structures, modeling of crack propagation in multilevel interconnects has not been well developed. In this paper, a 2D multi-level structure was used to study the crack propagation. The crack was assumed to initiate at an upper-level interface, which had been shown to have a higher energy release rate compared with that in a lower-level interface.

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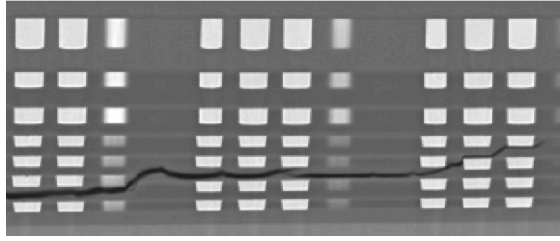
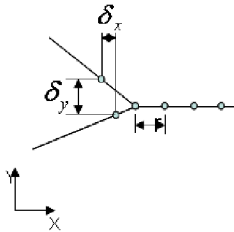


Fig. 4.Crack propagation in a multilevel interconnect

The CTOD method was employed to calculate the mode mixity at each crack tip as crack extended (Fig.5) and then the maximum hoop stress criteria was used to predict the crack propagation direction as shown in Eq. (2).



$$K_1 = \left[A\cos(\varepsilon \ln \boldsymbol{r}) + B\sin(\varepsilon \ln \boldsymbol{r})\right]/D$$

$$K_2 = \left[-A\sin(\varepsilon \ln \boldsymbol{r}) + B\cos(\varepsilon \ln \boldsymbol{r})\right]/D$$

$$A = \delta_y - 2\varepsilon\delta_x \quad B = \delta_x + 2\varepsilon\delta_y \quad D = \frac{8}{E^* \cosh(\pi\varepsilon)}\left(\frac{\boldsymbol{r}}{2\boldsymbol{\pi}}\right)^{1/2}$$

$$G = \frac{1}{E^* \cosh^2(\pi\varepsilon)}\left(K_1^2 + K_2^2\right)$$

Fig. 5. Crack Tip Opening Displacement Method (CTOD)

$$\sigma_{\theta\theta}(r,\theta) = \frac{\mathrm{Re}\left[Kr^{i\varepsilon}\right]}{\sqrt{2\pi r}}\cos^3\left(\frac{\theta}{2}\right) - \frac{\mathrm{Im}\left[Kr^{i\varepsilon}\right]}{\sqrt{2\pi r}}3\cos^2\left(\frac{\theta}{2}\right)\sin\left(\frac{\theta}{2}\right) \qquad \text{Eq. (2)}$$

$$\tan\left(\frac{\theta^*}{2}\right) = \frac{2\tan\psi}{1+\sqrt{1+8\tan^2\psi}}$$

The crack propagation path obtained by simulation was plotted in Fig. 6, propagating from the upper levels to the lower levels. The actual path may not be exactly as shown since it can be affected by process defects and material inhomogeneity in the low-k interconnects. Nevertheless, the overall crack behavior can still be deduced from the simulation. The result also demonstrated that as the crack propagates toward the lower levels and the total crack length increases, the energy release rate increases, indicating an unstable crack growth.

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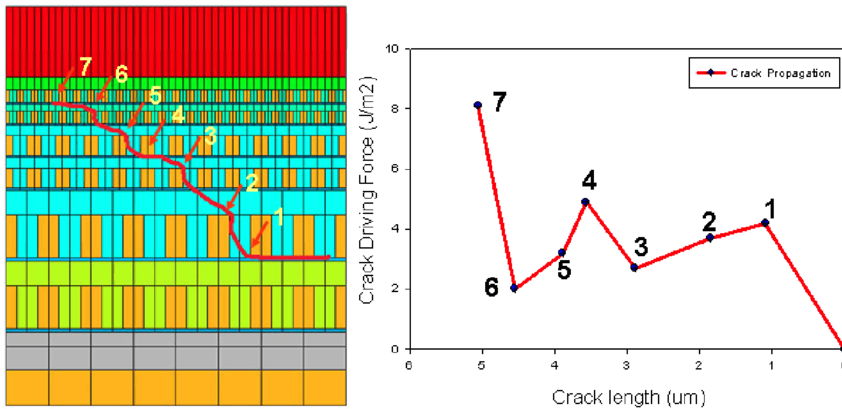

Fig. 6. ERR for crack propagation

A major challenge in packaging Si die is to prevent cracks propagating from the die edge to the active area of a chip during packaging process. One way to suppress crack propagation is to implement crack stop structures into the interconnects. The effect of crack stop structures was analyzed in this study. Dummy Cu barriers at via levels were added into Cu/low-k interconnect as local reinforcements. The simulation result showed that the crack driving force was suppressed by the crack stop structure as shown in Fig. 7. Meanwhile, our experiments revealed that the toughness of interconnects was increased due to the implementation of the crack stop structure, thus demonstrating its effectiveness in improving the mechanical reliability of low-k interconnect. The study also showed that the crack driving force increases with crack length. Therefore, the most effective way to use the crack-stop is to embed it very close to the crack initiation locations such as die edge or where fully dense low-k contacts with ultra low-k material.

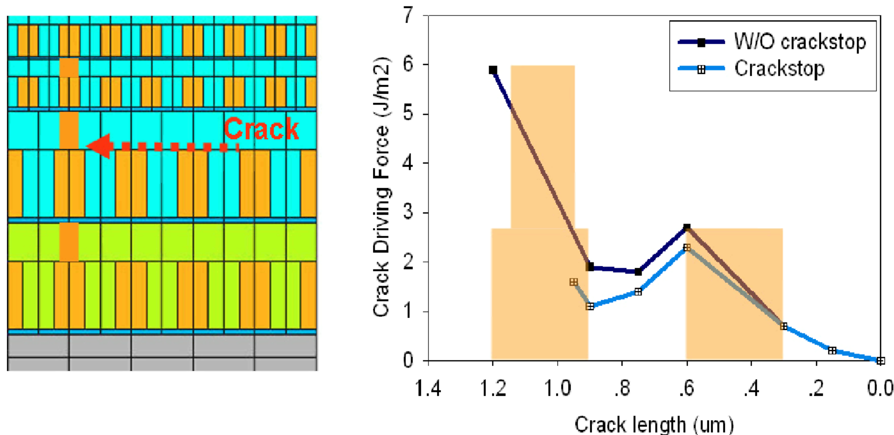

Fig. 7. Effect of crackstop structure on ERR

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FRACTURE TOUGHNESS MEASUREMENT

Several crack stop designs were tested using the m-ELT technique and the results were plotted in Fig. 8. Significant increase in the fracture resistance was observed for chips with crack stop structures to about 20 J/m2 as compared with chips without crack stop structures, usually about 1~4 J/m2 [12]. This demonstrated the effectiveness of the crack structure in preventing dicing cracks at the die edge from propagating into the active interconnect structure. Failure analysis of these samples yielded a crack propagation path from upper interconnect level to lower level as shown in Fig.9, which is consistent with our simulation results.

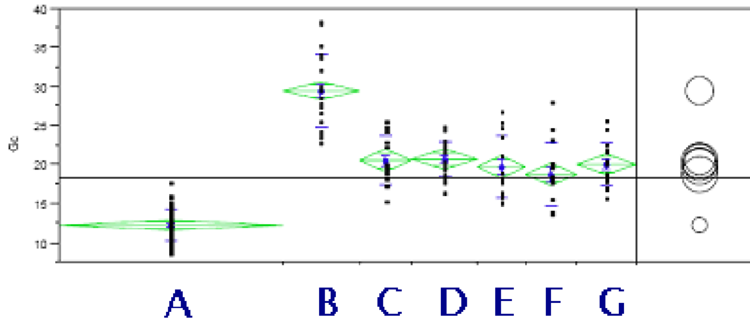

Fig. 8: Fracture toughness measurement of crackstop by MELT

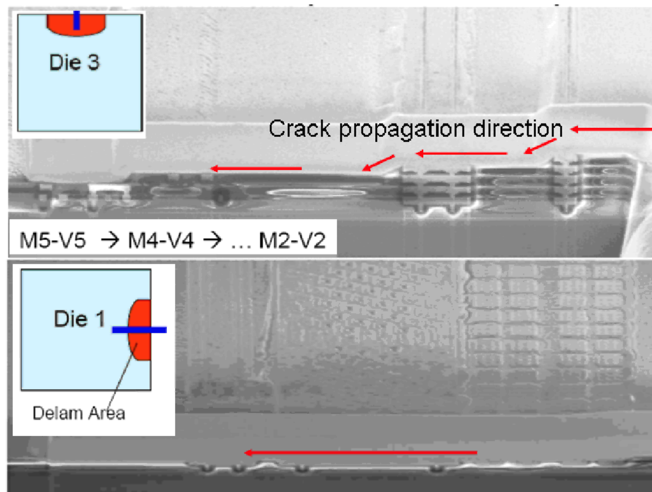

Fig. 9: Failure analysis of failed samples

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CONCLUSIONS

The impact of CPI on the mechanical reliability of Cu/Ultra low-k interconnects in a flip chip package was investigated using a multi-level sub-modeling method. Modeling showed that crack propagated from the upper-level interconnect towards Si substrate under CPI, which agrees well with our experimental observations. A decrease in the energy release rate was achieved by adding dummy Cu structure at the via level into the low-k interconnect. Meanwhile, m-ELT results revealed that the fracture toughness of the structure was increased by implementing crackstops. The study demonstrated proper design of the crackstop structure is critical in suppressing crack propagation and improving the mechanical reliability of Cu/ultra low-k interconnect.

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