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Thermomechanical Reliability Challenges For 3D Interconnects With Through-Silicon Vias

Suk-Kyu Ryu[a], Kuan-Hsun Lu[b], Xuefeng Zhang[b,c], Jay Im[b], Paul S. Ho[b] and Rui Huang[a]

[a]*Dept. of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712*
[b]*Microelectronics Research Center, University of Texas, Austin, TX 78712*
[c]*Advanced Micro Devices, 7171 Southwest Pkwy, Austin, TX 78735*

Abstract. Continual scaling of on-chip wiring structures has brought significant challenges for materials and processes beyond the 32 nm technology node in microelectronics. Recently three-dimensional (3-D) integration with through-silicon-vias (TSVs) has emerged as an effective solution to meet the future interconnect requirement. Among others, thermo-mechanical reliability is a key concern for the development of TSV structures used in die stacking as 3-D interconnects. This paper examines the effects of thermally induced stresses on interfacial reliability of TSV structures. First, three-dimensional distribution of the thermal stress near the TSV and the wafer surface is analyzed. Using a linear superposition method, a semi-analytic solution is developed for a simplified structure consisting of a single TSV embedded in a silicon (Si) wafer. The solution is verified for relatively thick wafers by comparing to numerical results from finite element analysis (FEA). The stress analysis suggests interfacial delamination as a potential failure mechanism for the TSV structure. An analytical solution is then obtained for the steady-state energy release rate as the upper bound for the interfacial fracture driving force, while the effect of crack length is evaluated numerically by FEA. With these results, the effects of the TSV dimensions (e.g., via diameter and wafer thickness) on the interfacial reliability are elucidated. Furthermore, the effects of via material properties are discussed.

Keywords: Through-Silicon via, thermal stress, interfacial delamination
PACS: 46.50.+a

INTRODUCTION

Continual scaling of microelectronic devices has brought serious challenges to the materials and processes of on-chip interconnect beyond the 32 nm technology node [1]. The 3-D integration presents an effective solution as a system approach, which has generated significant interests recently to develop 3-D interconnects [2-4]. A critical structural element in 3-D integration is the through-silicon via (TSV), which directly connects stacked structures die-to-die. The TSVs may assume various structural configurations such as fully filled TSV, annular TSV, TSV with 'nail head', and TSV with buffer layers (see Fig. 1). Use of TSVs in 3-D integration can effectively improve system performance and reduce manufacturing costs [5-7].

Due to the mismatch in the coefficients of thermal expansion (CTEs) of the via materials and Si, thermal stresses are ubiquitously induced during processing and thermal cycling of TSV structures, which can potentially degrade the performance of stress-sensitive devices around the TSVs [8, 9] or drive crack growth in 3-D

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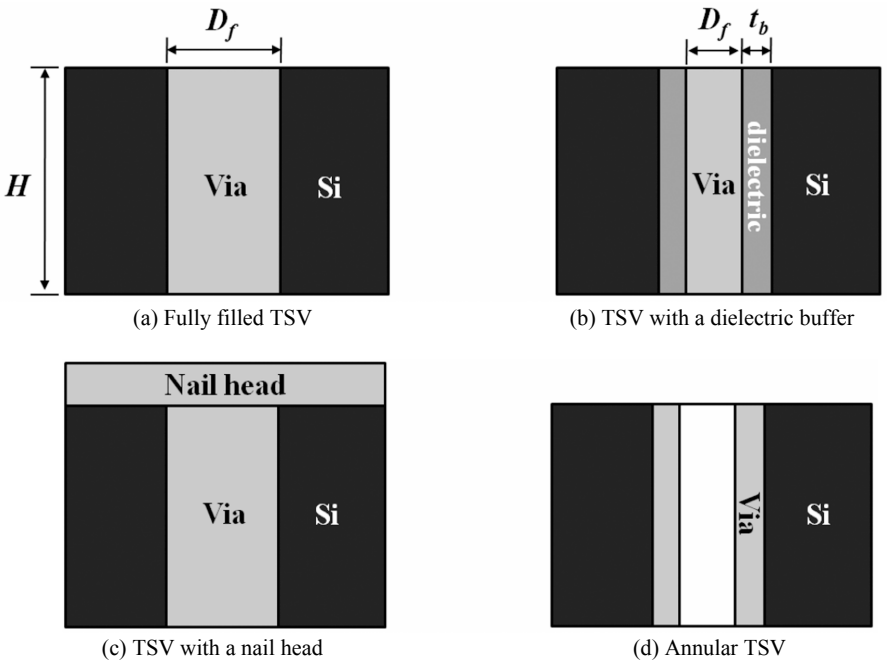
interconnects [9-13]. Therefore, the success of 3-D integration largely relies on the characteristics of thermo-mechanical stresses developed in the system and its impact on performance and reliability. Finite element methods have been used to numerically analyze the thermo-mechanical stresses in 3-D integrated structures [9-13], typically complicated by specific material processes and structural designs. To assess the themo-mechanical reliability of TSV structures, the driving forces for both cohesive and interfacial crack growth were calculated [12, 13]. In addition to these numerical studies, a simple analytical approach based on a 2-D model was used to analyze the thermomechanical interactions in TSV arrays [14]. However, the 2-D solution does not capture the 3-D nature of the stress field near the wafer surface around a TSV. Determination of the near-surface stresses is critical due to the fact that the active devices are usually located at the wafer surface.

In this paper, a semi-analytic 3-D solution is developed for an isolated TSV embedded in the silicon wafer (Fig. 1a), which compares closely with numerical results obtained by finite element analysis (FEA) for TSV structures with relatively thick wafers. We then focus on the interfacial reliability of TSV, for which an analytical solution is obtained for the steady-state energy release rate. Based on these results, the effects of the TSV materials and geometries on interfacial reliability are investigated.



(a) Fully filled TSV

(b) TSV with a dielectric buffer

(c) TSV with a nail head

(d) Annular TSV

FIGURE 1. Schematics of through-silicon vias (TSVs) in various structural forms.

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THREE-DIMENSIONAL STRESS ANALYSIS

Consider a single TSV embedded in an infinite Si wafer (Fig. 1a). The stress field induced by differential thermal expansion in the via and Si is three-dimensional in nature. As a prerequisite for the study of stress-related phenomena, we assume in the present study that all materials are isotropic and linearly elastic. Under the assumption of linear elasticity, the stress field in the TSV structure can be obtained by superposition of the two problems sketched in Fig. 2. In Problem A, the system is subjected to a thermal loading (ΔT) and a uniform stress (σ_z) on the surfaces of the via, so that the stress field is homogeneous in the via. To recover the traction-free boundary condition on the surfaces in the original problem, the normal stress on the surface is removed by superimposing Problem B, in which the via is subjected to a pressure of the same magnitude ($p = \sigma_z$) at both ends, but no thermal load. Problem A can be solved analytically, while an approximate solution to Problem B can be obtained semi-analytically. The same method was previously used to determine the stress field in fiber-reinforced intermetallic composites [15].

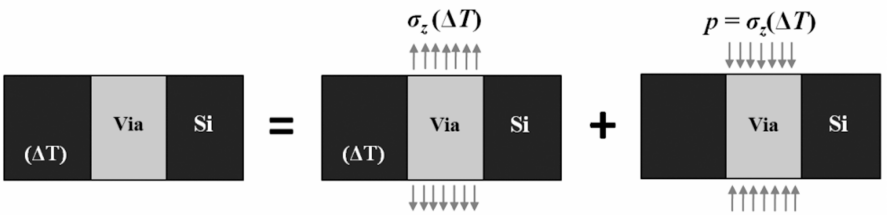

FIGURE 2. Illustration of the method of superposition to obtain the semi-analytical solution for the thermal stresses in a TSV structure: (a) the original problem; (b) Problem A; (c) Problem B.

The exact solution to Problem A in Fig. 2b is identical to the 2-D plane-strain solution to the classical Lame problem in elasticity [16]. The thermal stress in the via is uniform and tri-axial, with the following components:

$$\sigma_r^A = \sigma_\theta^A = \frac{-E_f \varepsilon_T}{1-2\nu_f + \dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}} \text{ and } \sigma_z^A = -E_f \varepsilon_T \left[\frac{1+\dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}}{1-2\nu_f + \dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}} \right] . \quad (1)$$

where σ_r, σ_θ, and σ_z are the radial, circumferential, and axial stresses, respectively, and $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$ is the thermal mismatch strain. The material properties, α, E, ν, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson's ratio, with the subscripts f and m for the via (fiber) and Si (matrix), respectively. In contrast, the stress field in Si ($r > D_f / 2$) is non-uniform and bi-axial:

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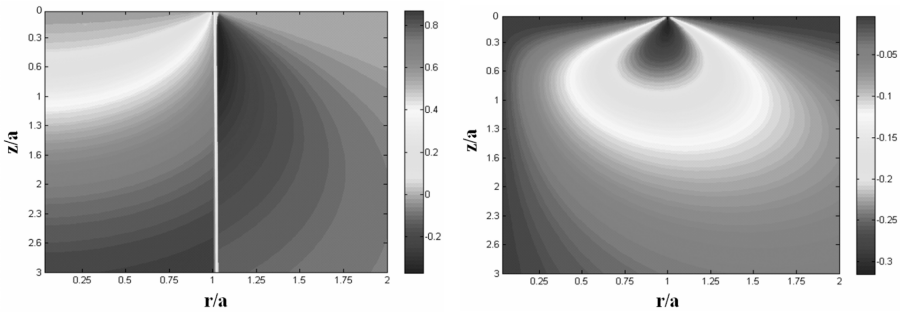
$$\sigma_r^A = -\sigma_\theta^A = \frac{-E_f \varepsilon_T}{1-2\nu_f + \dfrac{1+\nu_m}{1+\nu_f}\dfrac{E_f}{E_m}} \left(\frac{D_f}{2r}\right)^2, \tag{2}$$

where D_f is the diameter of the TSV and r is the radial coordinate measured from the center of the via. The stress field in Eqs. (1-2) can be simplified by neglecting the elastic mismatch between the via and Si, with $E_f = E_m = E$ and $\nu_f = \nu_m = \nu$ as given in the previous studies [13, 14].

The above 2-D solution does not satisfy the traction-free boundary condition on the surfaces in the original problem (Fig. 1a) because of the presence of the axial stress (σ_z^A) in the via. This is corrected by superimposing Problem B in Fig. 2, with a uniform axial stress of the same magnitude acting at both ends of the TSV in the opposite direction (i.e., $p = \sigma_z^A$). The stress field due to the surface pressure is typically localized near the ends of the via. Thus, the stress distribution in Eqs. (1-2) is an accurate solution far away from the ends of the TSV, especially for high aspect-ratio (height/diameter, or H/D_f) TSVs embedded in a thick wafer. However, the correction due to Problem B renders a very different stress distribution near the wafer surface around the TSV. For a relatively thin wafer, the stress in the entire via and its surrounding can be affected and thus different from the 2-D solution. In the following, we first develop a semi-analytical solution to Problem B for a thick wafer and then study the effect of wafer thickness numerically by FEA.

Focusing on the near-surface stress field for Problem B in Fig. 2, we consider a semi-infinite wafer subject to a uniform pressure on the surface over a circular area of diameter D_f. For simplicity, we neglect the elastic mismatch between the via and Si, so that $p = \sigma_z^A = -E\varepsilon_T/(1-\nu)$. Consequently, the solution can be obtained in an integral form based on the 3-D solution to the classical Boussinesq problem in elasticity [16, 17]. The stress field is axi-symmetric, varying with both r and z in the cylindrical coordinate with $z = 0$ at the surface.



(a) Axial stress (σ_z) (b) Shear stress (σ_{rz})

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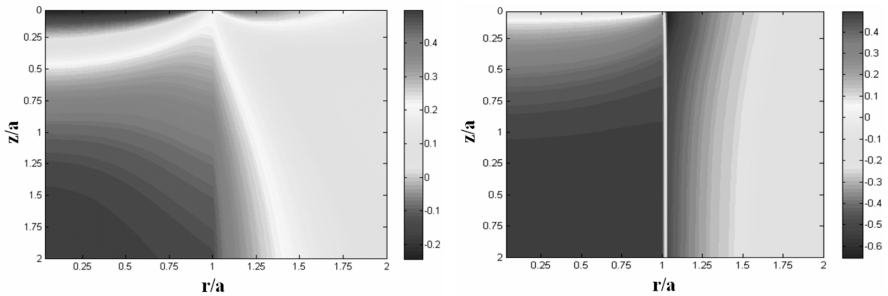

(c) Radial stress (σ_r) (d) Circumferential stress (σ_θ)

FIGURE 3. Near-surface stress distributions predicted by the semi-analytical solution. The stress magnitude is normalized by $p = -E\varepsilon_T/(1-\nu)$.

The near-surface stress distribution around the via is then obtained by adding the stress distributions for Problem B onto Eqs. (1-2) for both the via and the Si wafer, i.e., $\sigma_z = \sigma_z^A + \sigma_z^B$, etc. The contours of the overall stress distribution are plotted in Figure 3, where the stress magnitude is normalized by the pressure p. Figure 3a shows that the normal stress σ_z is zero on the surface ($z = 0$), as required by the traction-free boundary condition. The normal stress is non-uniform in the via and Si near the surface. Unlike the 2-D solution, the shear stress (σ_{zr}) is not zero near the end of the via (Fig. 3b). In fact, a concentration of the shear stress is predicted at the junction between the surface ($z = 0$) and via/Si interface ($r = D_f/2$), which can contribute to the driving force to cause interfacial delamination. The distributions of the radial stress (σ_r) and the circumferential stress (σ_θ) near the end of TSV (Figs. 3c and 3d) are also very different from the predictions by the 2-D solution. Depending on the sign of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$, the stresses can be either tensile or compressive. For example, if $\alpha_f > \alpha_m$, $p < 0$ for heating ($\Delta T > 0$) and $p > 0$ for cooling ($\Delta T < 0$). For the case of cooling, the radial stress is tensile along the via/Si interface, which can contribute to the driving force for interfacial delamination. The radial stress is also tensile in Si near the surface, which may cause circumferential cracking (C-cracks) of the Si. During heating, the circumferential stress is tensile in Si, which may cause radial cracks (R-cracks) in Si. For both heating and cooling, the presence of the shear stress (σ_{rz}) along the TSV/Si interface can induce interfacial failure by delamination.

To verify the semi-analytic solution, finite element analysis (FEA) is performed using the commercial package, ABAQUS (v6.8). Since the thickness of the Si wafer is one of the key design parameters for the TSV structure, the effect of wafer thickness on thermal stress distribution is examined by FEA models with two different thicknesses. The model structure is shown in Fig. 1a, with the TSV diameter $D_f = 30$ μm and the wafer thickness $H = 300$ μm and 60 μm. A negative thermal loading (cooling), $\Delta T = -250$ ºC, is assumed. The material properties are: $E_f = E_m = 110$ GPa, $v_f = v_m = 0.35$, and $\alpha_f = 17$ ppm/ºC and $\alpha_m = 2.3$ ppm/ºC. The model is an

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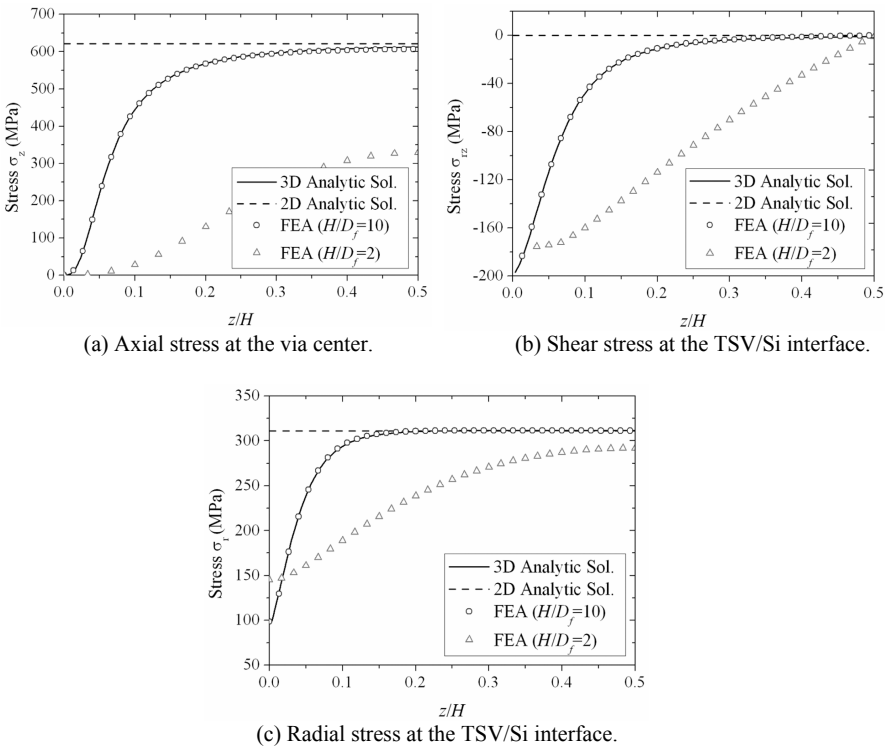
approximation to a Cu TSV in Si, neglecting the elastic mismatch between Cu and Si. In practice a thin barrier layer is typically needed between the Cu via and Si, which has minimal effects on the stress distribution and is thus ignored here.



(a) Axial stress at the via center.

(b) Shear stress at the TSV/Si interface.

(c) Radial stress at the TSV/Si interface.

FIGURE 4. Effect of wafer thickness on stress distributions ($D_f = 30$ μm and $\Delta T = -250$ ºC).

Figure 4 shows the FEA results, in comparison with the semi-analytical solution. First, the axial stress (σ_z) along the center line of the TSV (r = 0) shows a transition from zero stress at the surface (z = 0) to a tensile stress away from the surface (Fig. 4a). For the thick wafer ($H / D_f = 10$), the FEA result shows excellent agreement with the analytical solution, both approaching the 2-D solution (the dashed line) away from the surface. For the thin wafer ($H / D_f = 2$), however, the axial stress in the TSV is significantly lower, due to close proximity of the two free surfaces. The shear and radial stresses along the TSV/Si interface ($r = D_f / 2$) are shown in Figs. 4b and 4c, respectively. Again, the semi-analytical solution compares closely with the FEA results for the thick wafer. By symmetry, the shear stress is zero at the mid-plane of the wafer ($z / H = 0.5$). Based on an asymptotic analysis of the semi-analytical solution [17], the magnitude of the shear stress at the interface approaches a finite value ($\sigma_{rz} \to -p / \pi$) at the surface (z = 0). In between, the variation of the shear stress depends on the wafer thickness. Similarly, the radial stress (σ_r) at the interface

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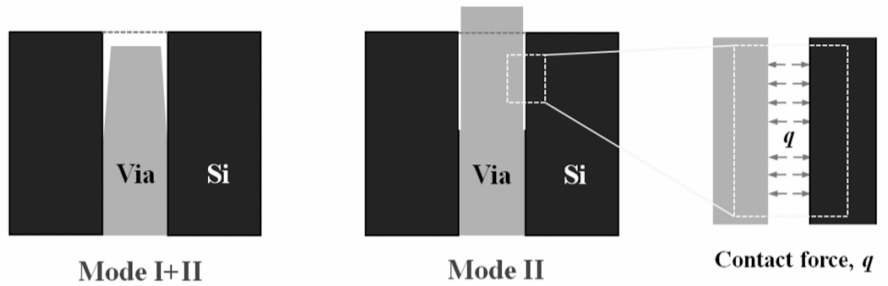
approaches a finite value ($\sigma_r \to (0.5-\nu)p$) at z = 0 and approaches the 2-D solution (the dashed line, $\sigma_r \to 0.5p$) far away from the surface. For the thinner wafer, the radial stress is slightly higher near the surface but is lower elsewhere.

It is seen from Fig. 4 that the 2-D plane-strain solution only predicts stresses far away from the wafer surface, while the semi-analytical 3-D solution is a good approximation everywhere for relatively thick wafers (e.g., $H/D_f > 10$). Neither solution is applicable for relatively thin wafers.

ANALYSIS OF INTERFACIAL DELAMINATION

The stress analysis in the previous section suggests a potential failure mechanism of the TSV structure due to interfacial delamination. Figure 5 depicts two modes of interfacial delamination for a fully-filled TSV structure. With a negative thermal load ($\Delta T < 0$), the radial stress along the via/Si interface is tensile (assuming $\alpha_f > \alpha_m$). Consequently, the interfacial delamination crack may grow in a mixed mode (peeling and shearing). With a positive thermal load ($\Delta T > 0$), however, the radial stress is compressive which does not contribute to the driving force for delamination. This results in an interfacial crack with a pure shearing mode (mode II). In this case, the two crack faces are in contact and may be subject to friction. For simplicity, we assume a frictionless contact in the present study. In the following, we first develop analytical solutions for the steady-state energy release rates of the interfacial crack, under both cooling and heating conditions. The analytical solutions are then compared to finite element analysis, which is extended to study the effects of crack length and wafer thickness on the fracture driving force.



(a) Cooling ($\Delta T < 0$) (b) Heating ($\Delta T > 0$)

FIGURE 5. Schematics of interfacial delamination of TSV under cooling and heating conditions.

For a TSV with a relatively high aspect ratio (H/D_f), the energy release rate for interfacial delamination reaches a steady state when the crack length is several times greater than the via diameter. Since the energy release rate is usually lower for shorter cracks, the steady-state value sets an upper bound for the fracture driving force, which may be used as the critical condition for conservative design of reliable TSV structures.

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Consider an infinitely long fiber (TSV) in an infinite matrix (Si wafer), with a semi-infinite, circumferential crack along the interface and subjected to a thermal load (ΔT). The steady-state energy release rate for the interfacial crack growth is obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. While the stress field near the crack front is complicated with singularity, it translates in a steady state as the crack front advances. Far ahead of the crack front, the stress field can be obtained analytically by solving the 2-D plane-strain problem (Problem A in Fig. 2). Far behind the crack front, since the TSV is debonded from Si, the stress is relaxed in both the via and Si. For the case of cooling ($\Delta T < 0$), the stress is zero in both TSV and Si. For heating ($\Delta T > 0$), however, the contact between the crack faces induces a stress field similar to Problem A, but the axial stress (σ_z) in the via is zero under the assumption of frictionless contact.

For the case of cooling, the steady-state energy release rate is obtained as [25]

$$G_{cooling}^{SS} = \frac{E_m \varepsilon_T^2 D_f}{4}\left(\frac{(1+v_f)(1+\alpha)}{(1-2v_f)(1-\alpha)+(1+\alpha)\dfrac{1+v_m}{1+v_f}}+\frac{1}{2}\frac{1+\alpha}{1-\alpha}\right), \qquad (3)$$

where $\alpha = \left(\overline{E}_f - \overline{E}_m\right)/\left(\overline{E}_f + \overline{E}_m\right)$ is the Dundur's parameter for elastic mismatch between the TSV and Si, with $\overline{E} = E/\left(1-\nu^2\right)$. If the elastic mismatch is neglected (i.e., $\alpha = 0$ and $\nu_f = \nu_m = \nu$), Eq. (3) is reduced to a simpler form:

$$G_{cooling}^{SS} = \frac{E\varepsilon_T^2 D_f}{4(1-\nu)}. \qquad (4)$$

Under the heating condition ($\Delta T > 0$), due to the contact of the crack faces (Fig. 5b), the stress state in the TSV far behind the crack front is equi-biaxial:

$$\sigma_r = \sigma_\theta = -\frac{E_f \varepsilon_T}{1-v_f+(1+v_m)\dfrac{E_f}{E_m}}. \qquad (5)$$

Correspondingly, the stress field in the matrix (Si) is

$$\sigma_r = -\sigma_\theta = -\frac{E_f \varepsilon_T}{1-v_f+(1+v_m)\dfrac{E_f}{E_m}}\frac{D_f^2}{4r^2}. \qquad (6)$$

Therefore, the steady-state energy release rate for heating is

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$$G_{heating}^{SS} = \frac{E_m \varepsilon_T^2 D_f}{4} \left[\begin{array}{c} \dfrac{(1+\alpha)(1+v_f)}{(1-\alpha)(1-2v_f)+(1+\alpha)\dfrac{1+v_m}{1+v_f}} + \dfrac{1}{2}\dfrac{1+\alpha}{1-\alpha} \\ -\dfrac{(1+\alpha)}{(1-v_f)(1-\alpha)+(1+v_m)(1+\alpha)} \end{array} \right]. \quad (7)$$

Again, a simpler result can be obtained by neglecting the elastic mismatch, namely

$$G_{heating}^{SS} = \frac{1+v}{8(1-v)} E \varepsilon_T^2 D_f . \quad (8)$$

We note the following from the analytical solutions. First, the steady-state energy release rate for interfacial delamination is linearly proportional to the TSV diameter, which may set an upper bound for the via diameter in order to avoid delamination. Second, the energy release rate is proportional to the square of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$. Thus the delamination driving force can be reduced by either using TSV materials with smaller thermal expansion mismatch ($\alpha_f - \alpha_m$) and/or by reducing the thermal loads (ΔT). Third, the energy release rate for interfacial delamination increases with the elastic modulus of the TSV material; however, the effect is less prominent than the effect of the thermal expansion mismatch. Finally, a comparison between Eq. (4) and (8) indicates that, with the same magnitude for the thermal load (ΔT), the driving force for interfacial delamination under cooling is about twice of that under heating. Furthermore, we note that the energy release rate should be compared to the adhesion energy (fracture toughness) of the interface in order to assess the interfacial reliability, as discussed later.

TABLE 1. Thermomechanical properties of the TSV materials used in the present study.

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's ratio
Si	2.3	130	0.28
Cu	17	110	0.35
Al	20	70	0.35
Ni	13	207	0.31
W	4.4	400	0.28
BCB	40	3.0	0.34

For a finite-sized TSV structure with a finite interfacial crack, the energy release rate depends on both the crack length and the wafer thickness. In Fig. 6 we show the energy release rate as a function of the crack length for different TSV diameters with a wafer thickness $H = 300\ \mu m$. The material properties for the via and the substrate are taken as those of Cu and Si in Table 1. A FEA model of the TSV structure is constructed, and the energy release rates are calculated by the method of J-integral in ABAQUS. As expected, the energy release rate increases with the crack length and approaches the steady-state solution when the crack length is about 2-3 times the via

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diameter. By comparing the energy release rate to the interfacial adhesion energy, i.e., $G(a_c) = \Gamma$, a critical crack length (a_c) may be determined, beyond which the delamination crack grows unstably. For a conservative design, one may require $G_{SS} \le \Gamma$ so that all cracks remain stable under the prescribed thermal loads.

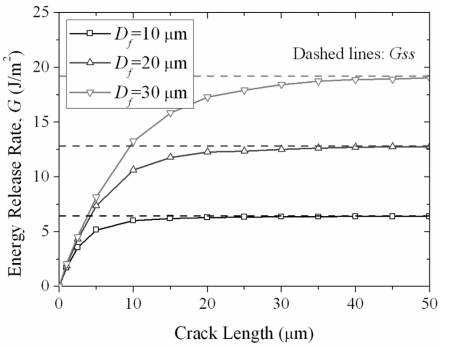

FIGURE 6. Effect of crack length on the energy release rate for interfacial delamination of TSVs (H = 300 μm and $\Delta T = -250$ °C).

To illustrate the effect of wafer thickness, Fig. 7 shows the energy release rate as a function of the crack length for different wafer thicknesses, with the same via diameter and thermal load. For a relatively thin wafer, the energy release rate for interfacial delamination reaches a maximum and then decreases as the crack length increases, approaching the wafer surface on the other side. The maximum energy release rate decreases as the wafer thickness decreases. Therefore, the interfacial reliability of TSVs may be improved by using thinner wafers, although other effects such as wafer handling and Si cracking may limit the use of thin wafers.

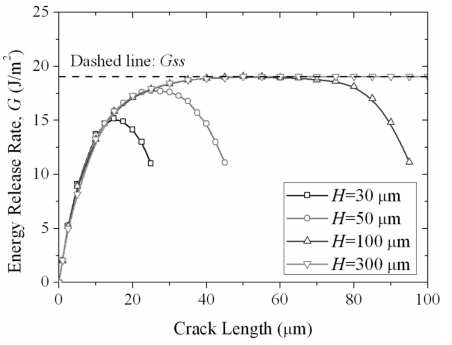

FIGURE 7. Effect of wafer thickness on the energy release rate for interfacial delamination of TSVs ($D_f = 30$ μm and $\Delta T = -250$ °C).

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EFFECTS OF TSV MATERIALS

Several other metals including aluminum (Al), nickel (Ni), and tungsten (W) have been considered to replace Cu as alternative materials for TSVs. The effect of materials on interfacial fracture driving force for the fully filled TSVs is evaluated using the thermomechanical properties listed in Table I. The steady-state energy release rates for the four TSV materials are compared in Fig. 8 under both cooling ($\Delta T = -250\,^{\circ}\mathrm{C}$) and heating ($\Delta T = 250\,^{\circ}\mathrm{C}$) conditions, with the same TSV diameter of 30 microns. Compared to Cu, Al has a lower Young's modulus but a larger mismatch in CTE with Si. Consequently, the driving force for interfacial delamination is higher for Al under the same thermal load. In contrast, Ni has a higher Young's modulus than Cu but a lower thermal mismatch, resulting in a lower driving force for delamination. Despite the highest Young's modulus, W has a very small CTE mismatch with Si, and thus the delamination driving force is significantly lower than that for the Cu TSV. This renders W a particularly attractive material for TSV applications from the interfacial reliability perspective.

For each TSV material, the energy release rate has to be compared with the interfacial adhesion energy, i.e., $G(a_c) = \Gamma$, to determine a critical crack length (a_c), beyond which the delamination crack grows unstably. The interfacial adhesion varies with the TSV material and may be enhanced by using thin adhesive barrier layers between the TSV and Si [18]. Energy dissipation due to friction may also increase the total fracture energy, especially for the case of heating. In addition, plastic deformation of the TSV metals has not been considered in the present study. Plastic yielding could partly relax the thermal stress in the via and the Si, thus reducing the fracture driving force. Moreover, the energy dissipation during plastic deformation could contribute to the overall fracture energy [19]. Therefore, the interfacial reliability may be improved by plasticity in the via. However, plastic deformation is irrecoverable and could lead to other reliability issues such as dislocations, stress voiding and fatigue. Further studies are required to understand the effect of plasticity on thermomechanical reliability of TSVs.

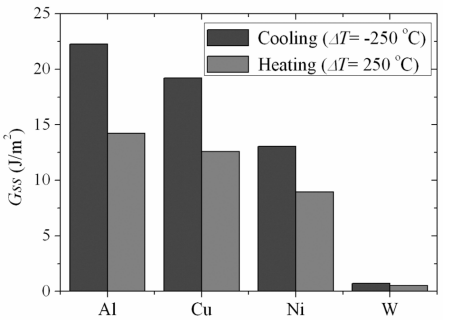

FIGURE 8. Comparison of the steady-state energy release rates for interfacial delamination in TSV structures using different via materials ($D_f = 30\,\mu\mathrm{m}$).

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EFFECTS OF DIELECTRIC BUFFER LAYERS

The present study has considered a much simplified structure with a single TSV embedded in Si. In practice, a thin barrier layer and/or a dielectric buffer layer may be needed between the TSV and Si. For example, to fabricate Cu TSVs, a dielectric or a nitride barrier layer is typically deposited on the via sidewall before Cu electroplating. The dielectric layer, which is often made of silicon dioxide with 1~2 μm thickness, provides insulation of the TSV from the silicon substrate. Similar to the Cu damascene interconnects, the barrier layer is usually made of metallic materials such as Ti, Ta, and their respective nitrides, TiN and TaN, with a thickness less than 0.1 μm [20-22]. The relatively thin barrier layer has little effect on the thermal stresses and the interfacial fracture driving force, but it may play an important role by enhancing the interfacial adhesion [18]. On the other hand, the much thicker dielectric buffer layer could serve as a stress buffer to reduce the thermal expansion mismatch between the TSV and Si, thus reducing the thermal stress and the fracture driving force. For this purpose, polymeric materials such as Parylene and BCB (Benzocyclobutene) have been used recently to replace the oxide layer [23, 24]. By using a 2~5 μm thick polymer buffer layer, the thermal stress in the TSV structure can be considerably reduced [13], and the electrical performance can be improved by reducing the capacitive coupling [24].

SUMMARY

In the present study, the characteristics of thermal stresses in a TSV structure are analyzed by a semi-analytical approach and FEA calculations. It is emphasized that the three-dimensional near-surface stress distributions are dramatically different from the analytical solution based on a simple two-dimensional model. The energy release rate for interfacial delamination of TSV is evaluated under both cooling and heating conditions, with an analytical solution under the steady-state condition and numerical solutions by FEA models. Based on these results, the effects of the TSV dimensions (e.g., via diameter and wafer thickness) on the interfacial reliability are elucidated. Furthermore, the effects of via material properties and dielectric buffer layers are discussed. Together, the potential of materials and structure optimization for improving TSV reliability is envisaged as the key for the development of 3D interconnects.

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