AIP Applied Physics Letters

Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique

Suk-Kyu Ryu, Tengfei Jiang, Kuan H. Lu, Jay Im, Ho-Young Son et al.

Citation: Appl. Phys. Lett. **100**, 041901 (2012); doi: 10.1063/1.3678020
View online: http://dx.doi.org/10.1063/1.3678020
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i4
Published by the American Institute of Physics.

Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique

Suk-Kyu Ryu,[1] Tengfei Jiang,[2] Kuan H. Lu,[2] Jay Im,[2] Ho-Young Son,[3] Kwang-Yoo Byun,[3] Rui Huang,[1] and Paul S. Ho[2,a)]
[1]*Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, Texas 78712, USA*
[2]*Microelectronics Research Center and Texas Materials Institute, University of Texas, Austin, Texas 78712, USA*
[3]*Hynix Semiconductor Inc., Icheon-City, Gyeonggi-do, South Korea*

(Received 27 September 2011; accepted 27 December 2011; published online 23 January 2012)

Through-silicon via is a critical element for three-dimensional (3D) integration of devices in multilevel stack structures. Thermally induced stresses in through-silicon vias (TSVs) have raised serious concerns over mechanical and electrical reliability in 3D technology. An experimental technique is presented to characterize thermal stresses in TSVs during thermal cycling based on curvature measurements of bending beam specimens. Focused ion beam and electron backscattering diffraction analyses reveal significant grain growth in copper vias, which is correlated with stress relaxation during the first cycle. Finite element analysis is performed to determine the stress distribution and the effect of localized plasticity and to account for TSV extrusion observed during annealing. © *2012 American Institute of Physics*. [doi:10.1063/1.3678020]

Three-dimensional (3D) integration with through-silicon vias (TSVs) has emerged as an effective solution to overcome the wiring limit imposed on device density and performance.[1,2] However, thermal expansion mismatch between copper (Cu) TSVs and silicon (Si) can induce thermal stresses sufficient to cause cracking or interfacial delamination in the TSV structures.[3–6] Moreover, the stresses in Si may degrade the electrical performance of active devices or components placed near the TSVs.[7] It is thus important to understand the characteristics of the thermal stresses as well as the potential impacts on mechanical and electrical reliability of 3D integration. Recently, Raman spectroscopy has been applied to measure thermal stresses in Si near Cu TSVs.[8,9] The technique, however, yields only a certain combination of the near-surface stress components in Si and does not measure the stresses in the metal vias directly. Experimental methods to measure thermal stresses in TSVs and to validate numerical models are urgently needed. In this Letter, we present a bending beam technique that can be used to experimentally characterize thermal stresses in TSVs.

The bending beam (BB) technique is similar to the wafer curvature method for characterizing stresses in thin films.[10–12] Typically, Stoney's formula is used to determine the average stress in a thin film based on the measurement of wafer curvature. The method has been extended to periodic line structures.[13] For the TSV structures, the bending beam technique allows measurement of the curvature and average stress during thermal cycling, based on which the elastic and plastic behavior can be deduced. However, unlike thin films, the classical Stoney's formula does not apply for the TSV structures to directly convert substrate curvature into stresses. In the present study, finite element analysis (FEA) was performed to determine the stress distribution and to examine the effect of plasticity.

The BB specimen consisted of periodic arrays of blind Cu vias with 10 μm diameter and 55 μm depth, as shown schematically in Fig. 1. The pitch distances are 50 μm and 40 μm in the longitudinal and transverse directions, respectively. As received, the top surface of Si was covered with an oxide layer of 0.8 μm thick. An oxide barrier layer of about 0.4 μm thick was deposited at the via/Si interface. The specimen used for measurement was 5 mm wide, 50 mm long, and 700 μm thick. The TSV arrays were arranged in parallel patches along the center line of the specimen ($\sim$300 μm wide for each patch).

During sample preparation, an initial curvature was developed due to process induced residual stresses. To evaluate thermal stresses in the Cu vias during thermal cycling, two specimens were used, one of which served as the reference with the Cu vias etched off using nitric acid. Both specimens were heated to 200 °C with a heating rate of 2 °C/min,

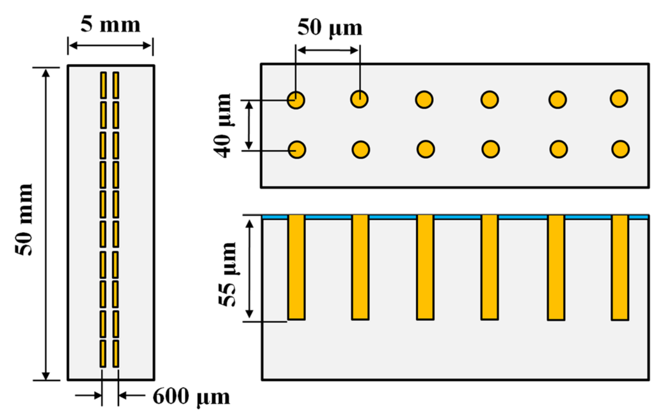

FIG. 1. (Color online) Illustration of the TSV specimen for bending beam tests.

a)Author to whom correspondence should be addressed. Electronic mail: paulho@mail.utexas.edu.

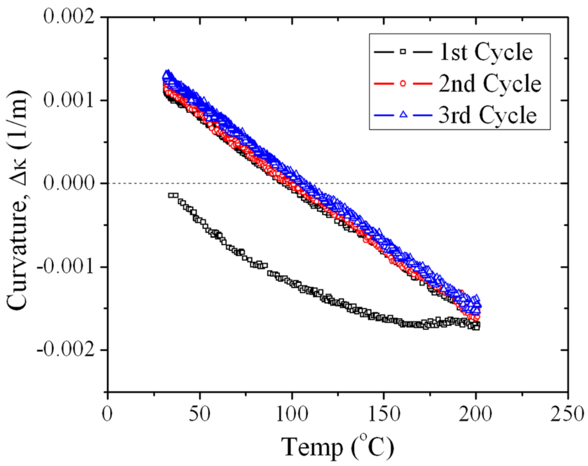

FIG. 2. (Color online) Measurement of curvature difference between a TSV specimen and a reference specimen during thermal cycling.

followed by cooling back to the room temperature. The curvature was measured by a scanning laser method. The curvature difference between the two specimens is attributed to the thermal stress in the Cu vias, as plotted in Fig. 2. During the first cycle, the curvature decreases nonlinearly as the temperature increases, suggesting an average compressive stress in the Cu vias and inelastic deformation possibly due to evolution of grain structures and/or plastic deformation. During subsequent cycles, however, the curvature-temperature relation is nearly linear with negligible hysteresis, indicating predominantly elastic behavior. This behavior is in sharp contrast with wafer curvature measurements of Cu thin films, which is typically nonlinear with a hysteresis loop due to plasticity.[11] The difference can be partly attributed to the triaxial stress states in the Cu vias. Unlike the biaxial stress in Cu films, the triaxial stress gives rise to a relatively low effective shear stress required for plastic deformation. Moreover, the effects of geometry and confinement may also play roles in suppressing plasticity in the Cu vias.[14]

As shown in Fig. 2, the curvature difference between the specimen with TSVs and the reference specimen without TSVs becomes zero at around 100 °C, which is consistent with the annealing temperature after electroplating of Cu to fill the TSV structures. It may thus be assumed that the stresses in the Cu vias are largely relaxed at around 100 °C during annealing. The temperature 100 °C is then used as the reference temperature for calculating thermal stresses in the TSV structures by finite element analysis.

Next, the oxide layer on the surface of the TSV specimen was mechanically polished off. The specimen was then subject to four thermal cycles, as shown in Fig. 3. In the first two cycles, the specimen was heated to 200 °C, and the behavior is similar to Fig. 2 for the specimen with the surface oxide layer. During the third and fourth thermal cycles, the specimen was heated to 350 °C. As the specimen was heated beyond 200 °C in the third cycle, the curvature-temperature relation becomes nonlinear, indicating inelastic stress relaxation at higher temperatures. The mechanism of such stress relaxation is not fully understood. In Cu thin films, inelastic deformation at high temperatures is often attributed to dislocation plasticity and diffusional creep.[10,11] However, plastic deformation in the Cu vias is found to be highly localized by the finite element analysis (Fig. 5), which has negligible effect on the overall curvature of the specimen. On the other hand, we observed significant grain growth almost everywhere in the Cu vias as shown in the focused ion beam (FIB) images in Fig. 3. The grain growth process can significantly reduce the thermal stress in the vias and thus the curvature. Similar behavior has also been observed for thin films.[12,15] Subsequently, in the fourth cycle, the curvature-temperature again becomes nearly linear between the room temperature and 350 °C, suggesting that the grain structure has been stabilized up to 350 °C. Further increasing the temperature would expect to result in more grain growth and stress relaxation.

In addition to the FIB images in Fig. 3, the grain size and orientation in the Cu vias were quantitatively analyzed by electron backscattering diffraction (EBSD). The average grain size for the specimen before thermal cycling was 0.71 μm. After thermal cycling to 350 °C, the grain size grew to 1.18 μm, which is about 60% larger. From the EBSD, no preferred grain orientation was observed, which has been also reported by others.[16] Furthermore, a large number of twin boundaries were observed with a characteristic 60° misorientation angle across the boundaries. The presence of these twin boundaries may play an important role in the mechanical behavior of the Cu vias, especially for the mechanisms of dislocation plasticity and grain boundary diffusion.

After subjected to the thermal cycling, the TSV specimen was cross-sectioned for scanning electron microscope (SEM) imaging. As shown in Fig. 4, extrusion of Cu vias is evident. In a previous study, we simulated TSV pop-up by assuming elastic deformation of the vias along with interfacial delamination based on a cohesive zone model.[17] In the present study, however, no evidence of interfacial

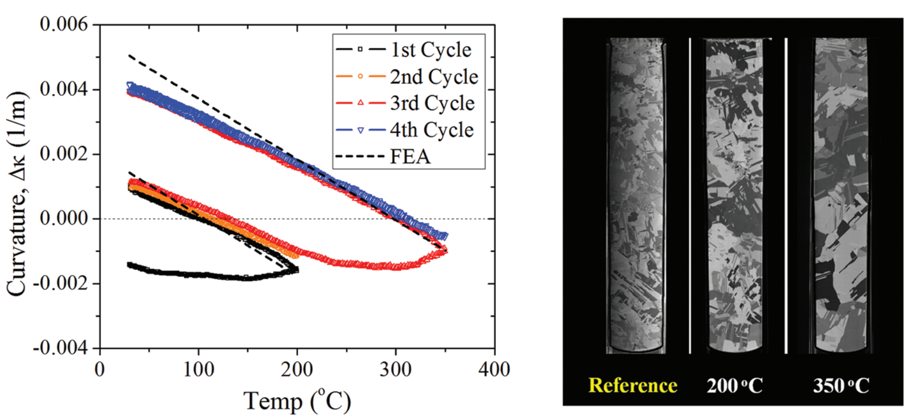

FIG. 3. (Color) Left: Curvature measurement of a TSV specimen with the surface oxide polished off. Right: FIB images showing the grain structures in the Cu vias before and after thermal cycling.

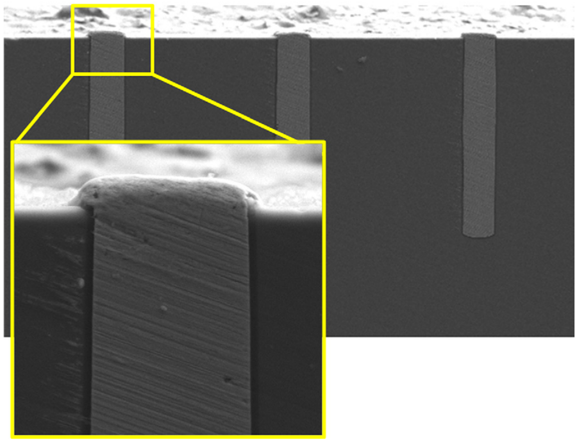

FIG. 4. (Color online) SEM images showing TSV extrusion after thermal cycling.

TABLE I. Thermomechanical properties used in finite element analysis.

Material	CTE (ppm/°C)	Young's modulus (GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
Oxide	0.55	72	0.16

delamination was observed. On the other hand, it is found that localized plastic deformation in the Cu vias (Fig. 5) could be responsible for the observed via extrusion.

The curvature measurements in the bending beam tests may be converted to volume average stresses in the TSVs, similar to the wafer curvature tests for periodic line structures.[13] However, the specimens used in the present study contained TSVs only in a narrow region along the center line, for which the volume average approach becomes less effective. Instead, finite element analysis was performed to determine the deformation and stress distribution in the TSV specimen. First, we assume all the materials to be linear elastic, with the properties listed in Table I. As shown in Fig. 5 (left panel), the specimen bends non-uniformly due to mismatch in thermal expansion. An average curvature is determined along the center line of the specimen, and the rate of curvature change, $\Delta\kappa/\Delta T$, is calculated for comparison with the bending beam results. As shown in Fig. 3, the measured curvature change is nearly linear with respect to the temperature during cooling in all cycles as well as during heating in the second and fourth cycles; the measured rate of curvature change is approximately -1.47×10^{-5} $m^{-1}/°C$. The FEA calculated rate of curvature change is -1.88×10^{-5} $m^{-1}/°C$, plotted as the dashed lines in Fig. 3, which is in fair agreement with the BB measurements considering the process variability of the TSV structures.

As discussed above, the inelastic behavior during heating in the first and third cycles (Fig. 3) could be a result of plastic deformation and grain growth in the Cu vias. The plastic yield strength of electroplated Cu films was measured to be around 250 MPa.[18] Assuming an elastic-plastic behavior for the Cu vias with the yield strength of 250 MPa, we calculated the deformation and stress distribution in the Cu vias, as shown in Fig. 5 (right panel). It is noted that the von Mises stress as the effective shear stress for plastic deformation is non-uniform in the Cu vias, which reaches the yield strength only in a small region near the junction between the via/Si interface and the upper surface. As a result, the plastic deformation in the Cu vias is highly localized, in contrast to Cu thin films where the stress is nearly uniform and plastic deformation occurs over the entire film volume. While the localized plastic deformation is sufficient to cause via extrusion, it has negligible effect on the overall curvature of the specimen. Therefore, the nonlinear curvature-temperature behavior is mainly due to grain growth induced stress relaxation, although plastic deformation with work hardening may also be possible. The grain growth could lead to lower yield strength of the Cu vias by the Hall-Petch effect, which in turn leads to more extensive plastic deformation and Cu extrusion. Thus it is important to stabilize the grain structures of the Cu vias before subsequent processes in order to minimize via extrusion. This may be achieved by high-temperature annealing as observed in the FIB images.

Based on this observation, an annealing process is suggested to prevent via extrusion. With a high annealing temperature (~400 °C), followed by a one-time chemical-mechanical planarization (CMP) process to remove the extruded Cu, TSV extrusion can be eliminated in the subsequent processes below the annealing temperature. This can simplify the fabrication processes of TSVs and significantly reduce the manufacturing cost.

In summary, we present results from bending beam tests of TSV specimens containing periodic arrays of blind Cu vias. Based on the measurements of curvature change under thermal cycling, the characteristics of thermal stresses in the TSVs are elucidated. Significant grain growth in the Cu vias was observed by FIB and EBSD analyses. It is found that local plastic deformation in Cu may lead to via extrusion, while stress relaxation due to grain growth is significant

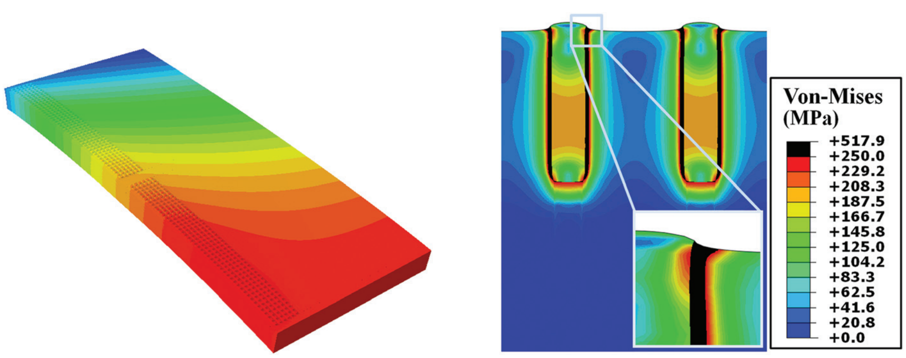

FIG. 5. (Color) FEA results with a thermal load $\Delta T = 200$ °C. Left: bending of the TSV specimen (quarter model); Right: plastic deformation and stress distribution.

during the first cycle and a subsequent cycle to a higher temperature. A process of high temperature annealing is suggested to stabilize the grain structures in the Cu vias to minimize via extrusion.

The authors gratefully acknowledge financial support of this work by Semiconductor Research Corporation. We are also grateful to Minsuk Suh at Hynix for providing the TSV specimens.

[1]L. W. Schaper, S. L. Burkett, S. Spiesshoefer, G. V. Vangara, Z. Rahman, and S. Polamreddy, IEEE Trans. Adv. Packag. **28**, 356 (2005).
[2]J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, R. Sirdeshmukh, E. J. Sprogis *et al.*, IBM J. Res. Dev. **52**, 553 (2008).
[3]N. Ranganathan, K. Prasad, N. Balasubramanian, and K. L. Pey, J. Micromech. Microeng. **18**, 075018 (2008).
[4]C. S. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. C. Chai, IEEE Trans. Adv. Packag. **32**, 720 (2009).
[5]K. H. Lu, S. K. Ryu, Q. Zhao, X. Zhang, J. Im, R. Huang, and P. S. Ho, in *Proceedings of Electronic Components and Technology Conference, Las Vegas, NV* (IEEE, New York, 2010), pp. 40–45.
[6]S. K. Ryu, K. H. Lu, X. Zhang, J. H. Im, P. S. Ho, and R. Huang, IEEE Trans. Device Mater. Reliab. **11**, 35 (2011).
[7]S. Thompson, G. Sun, Y. Choi, and T. Nishida, IEEE Trans. Electron Devices **53**, 1010 (2006).
[8]C. McDonough, J. Capulong, B. Backes, P. Singh, L. Smith, W. Wang, and R. E. Geer, SEMATECH Workshop on Stress Management for 3D ICs, Burlingame, CA, 2010.
[9]Y. Yang, G. Katti, R. Labie, Y. Travaly, B. Verlinden, and I. De Wolf, in *Proceedings of the IEEE International Interconnect Technology Conference, Burlingame, CA* (IEEE, New York, 2010).
[10]R. P. Vinci, E. M. Zielinski, and J. C. Bravman, Thin Solid Films **262**, 142 (1995).
[11]D. Gan, P. S. Ho, R. Huang, J. Leu, J. Maiz, and T. Scherban, J. Appl. Phys. **97**, 103531 (2005).
[12]D. C. Miller, C. F. Herrmann, H. J. Maier, S. M. George, C. R. Stoldt, and K. Gall, Thin Solid Films **515**, 3208 (2007).
[13]Y. L. Shen, S. Suresh, and I. A. Blech, J. Appl. Phys. **80**, 1388 (1996).
[14]M. D. Uchic, D. M. Dimiduk, J. N. Florando, and W. D. Nix, Science **305**, 986 (2004).
[15]J. M. E. Harper, C. Cabral, P. C. Andricacos, L. Gignac, I. C. Noyan, K. P. Rodbell, and C. K. Hu, J. Appl. Phys. **86**, 2516 (1999).
[16]M. Krause, F. Altmann, C. Schmidt, M. Petzold, D. Malta, and D. Temple, in *Proceedings of the Electronic Components and Technology Conference, Lake Buena Vista, FL* (IEEE, New York, 2011), pp. 1452–1458.
[17]S. K. Ryu, K. Lu, J. Im, R. Huang, and P. Ho, AIP Conf. Proc. **1378**, 153 (2011).
[18]Y. Xiang, X. Chen, and J. J. Vlassak, Mater. Res. Soc. Symp. Proc. **695**, 189 (2002).