Mechanical Stability of Air-gap Interconnects

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Abstract

Implementation of air-gaps in the trench dielectric levels has been demonstrated as a potential effective solution to further reduction of the capacitance coupling in the Cu/low-k interconnects.[1-4] In this paper, the critical issue of mechanical stability in such air-gap interconnect structures during thermal processing and under chip packaging interaction (CPI) is investigated using 3D multilevel finite element analysis (FEA) models.

Introduction

Implementation of air-gaps in the trench dielectric levels has been demonstrated as a potential effective solution for dielectric scaling beyond 32nm with an achievable dielectric constant below 2.0.[1-4] However, air-gap interconnect confronts serious challenges concerning its structural integrity and mechanical stability. Bridging low-k cap (or hard mask) was observed to collapse over wide gaps during thermal decomposition of the gap-forming material.[2,4] Crack initiation in keyhole-shaped gaps [5] formed by etch-back and nonconformal refill schemes can also be a potential reliability concern. As packaging assembly exerts additional stresses to the fragile interconnect structures, chip packaging interaction (CPI) has been recognized as a serious reliability issue for air-gap structures. In this paper, we analyzed the mechanical stability issues of air-gap interconnect structures during thermal processing and subsequent packaging assembly using 3D multilevel finite element analysis (FEA) models.

Structural and Mechanical Stability of as-Processed Air-gap Interconnects

A 3D five-level finite element model was developed to simulate process-induced stresses in an air-gap interconnect (see Figure 1). To catch the representative features, FSG was used in the first two metal levels and the global level. Air-gaps were implemented in levels three and four.

With varying line widths and dielectric materials, only slight reduction of the stress levels was observed in Cu wires as a result of air-gap implementation. This is not unexpected, as Cu wires are primarily confined by the silicon substrate. The introduction of air-gaps only further weakens the already weak confinement of Cu wires by the interlevel dielectrics. These results indicate that air-gap implementa-

tion will not impact on stress-related Cu reliability issues and will thus help focus our attention on the mechanical issues in the mechanically weak low-k dielectrics and relevant interfaces.

We first investigated the stability of the thin suspended dielectric layer after air-gap formation. This suspended dielectric layer can either be the perforated Cu cap in the etch-back approach or the

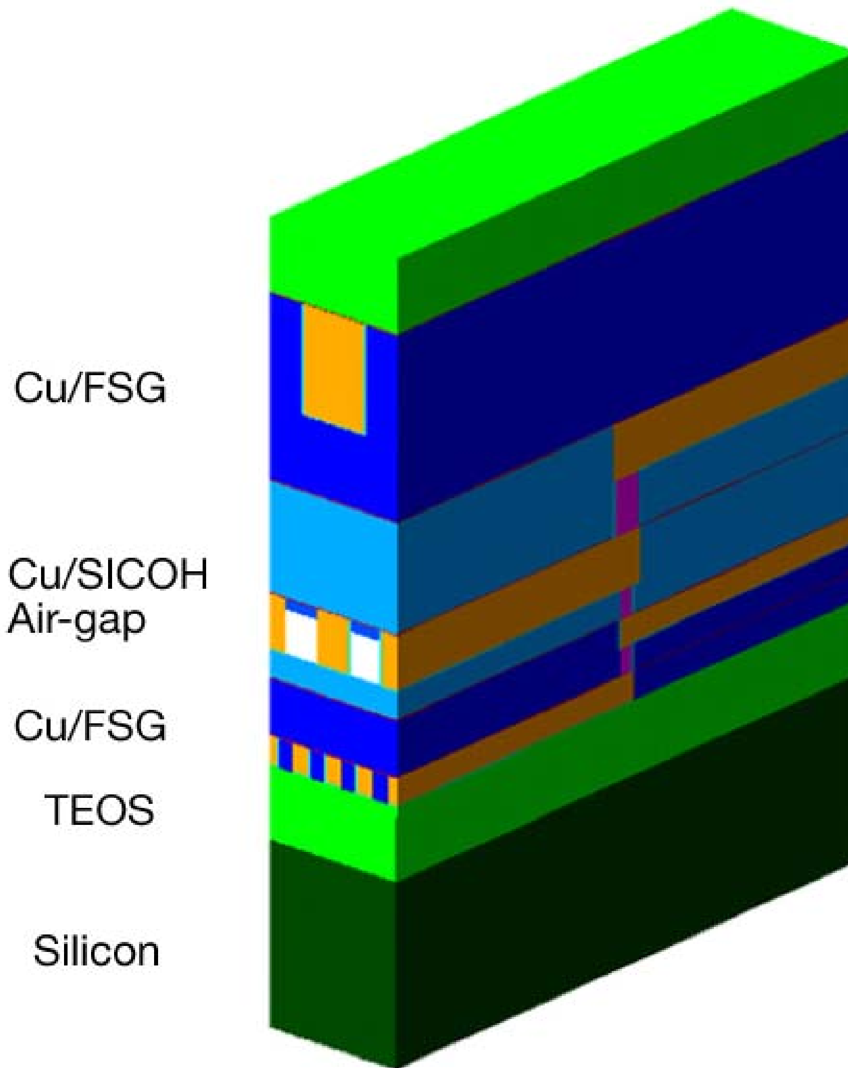


Figure 1. 3D Multilevel FEA Model

low-k cap (or hard mask) in the sacrificial removal approach. High stress level in this layer can cause its buckling under compression or channel cracking under tension.[6] Air-gap formation underneath is expected to result in reduced elastic constraint, which may further aggravate the cracking driving force.[7] Because the cap thickness is only a fraction of the thickness of the upper level ILD, and the cracking driving force is proportional to the film thickness, our study was first directed to the channel cracking of the ILD overlayer.

On a simplified 3D air-gap structure (see Figure 2), process-induced stresses and the energy release rate (ERR) for crack growth were calculated by following a typical process flow and using a virtual crack closure technique (VCCT).[8] The ERR for crack growth in the overlayer was found to increase with the air-gap width. This can be attributed to reduced constraints from the underlying layers. However, the ERR value was not affected much due to an increase of air-gap volume percentage (from 50 percent to 80 percent), a reduction of the modulus of the via level dielectric (from FSG to SiCOH) and changes of the Cu cap thickness (5/10/20nm). Up to a gap width of 2 μm, the ERR values are well below the typical cohesive strength of ULK's (G_C>5GPa). This pleasant surprise can be attributed to the additional constraints provided by the adjacent supporting Cu wires.

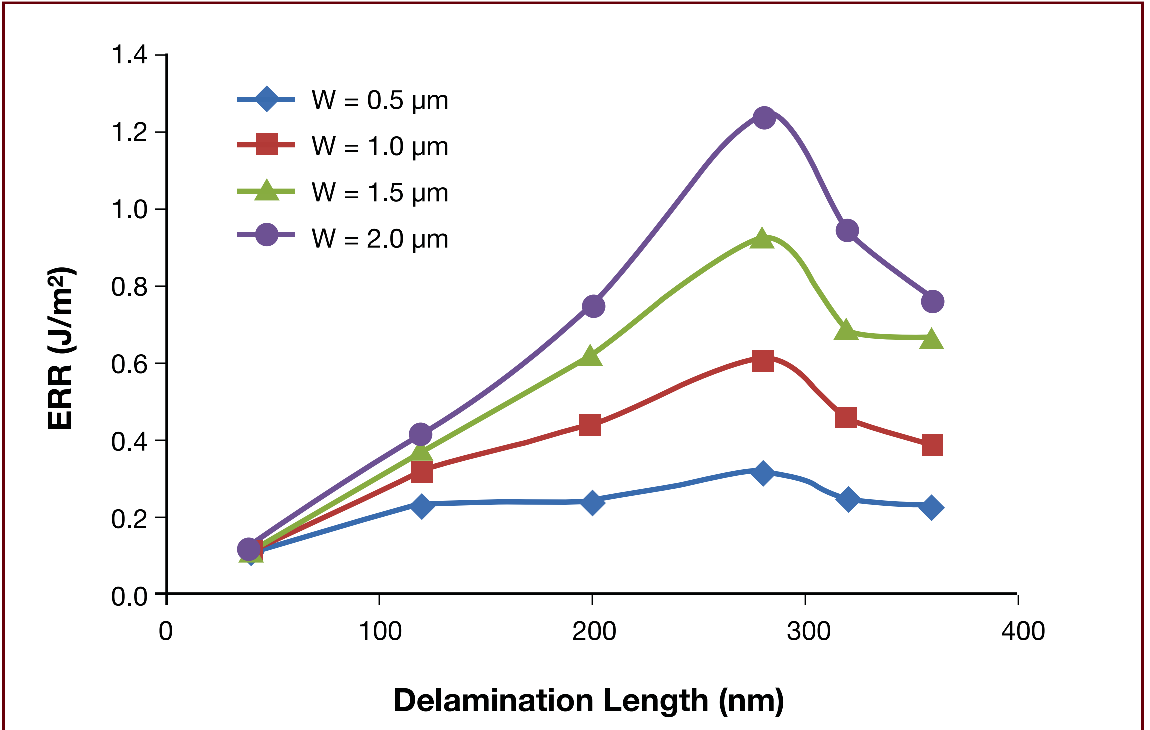
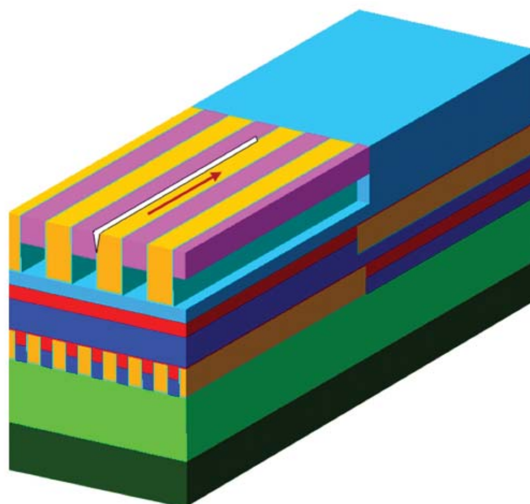
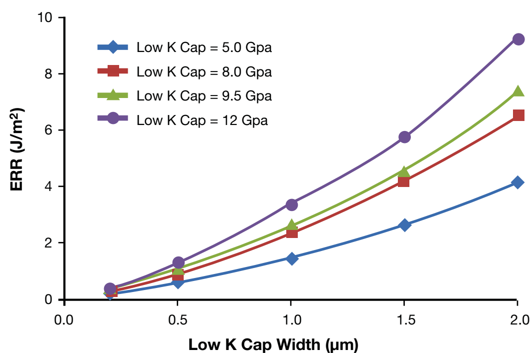


Figure 2. 3D Simplified Air-gap Model: Channel Cracking

In the sacrificial removal approach, the low-k cap (or hard mask) was observed to delaminate from the barrier and collapse during gap formation.[4] Using a similar simplified air-gap structure (see Figure 3a) and VCCT, we calculated the delamination driving force. The delamination ERR increases dramatically as the gap width increases. The ERR increases by an order of magnitude as the gap width increases from 0.2 μm to 2 μm. Even at a gap width of 1.5 μm, the potential cracking driving force has reached such a level that the low-k cap material and cap thickness must be carefully determined to prevent its collapse during processing (see Figure 3b).

Additional external stress load can be very problematic. This may well occur during the CMP process. A uniformly distributed load was added to pull the low-k cap toward the air gap, representing a possible down-





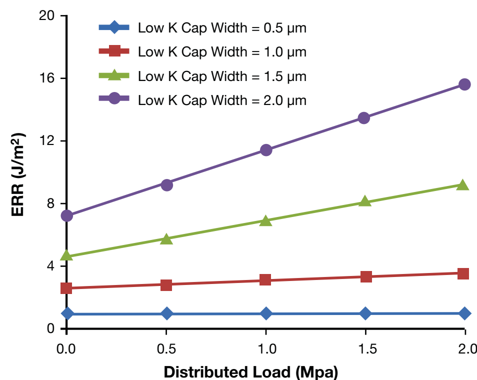
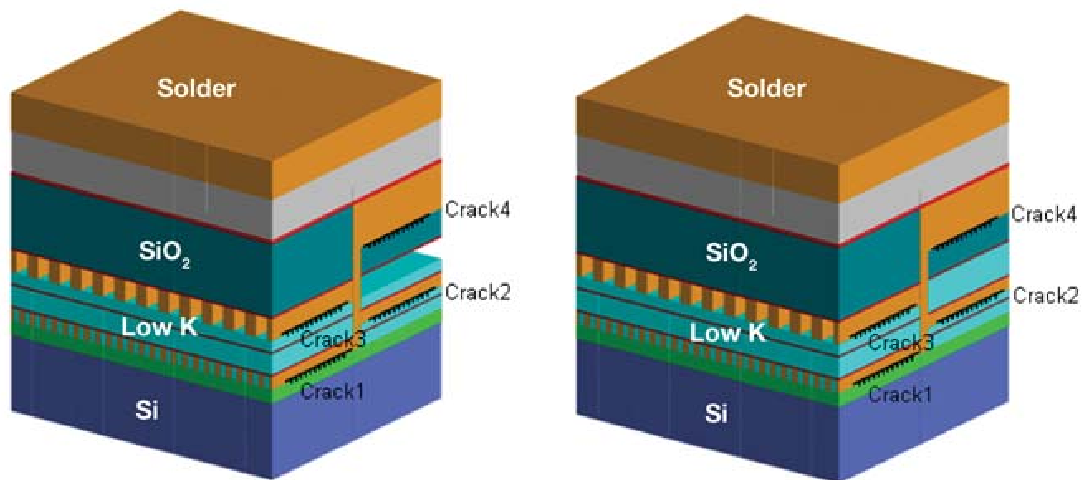


Figure 3. 3D Simplified Air-gap Model: Delamination



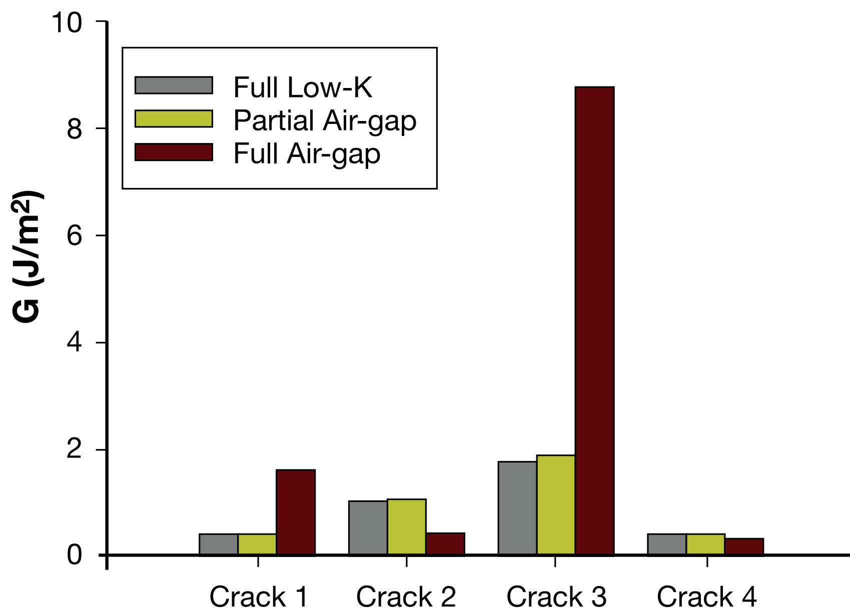


Figure 4. CPI Results

ward force either due to the decomposition of the sacrificial layer or CMP downforce. The ERR increases as the intensity of the distributed load increases, but the rate of increase depends on the gap width. For a gap width of 1.5 to 2 μm, the ERR can increase 2-3x, thus significantly increasing the delamination risk (see Figure 3b).

Impact of Chip-Packaging Interaction

Packaging is where the interconnect structure as a whole is subjected to significant external stresses. Take plastic flip-chip packages for example; the highest thermal load occurs during die attach before underfilling. The CPI effect for air-gap structures was investigated for Pb-free solders with a reflow temperature of 250°C. The substrate in the package was organic and with a die size of 8x8 mm^2. On a slightly different 3D finite element model, multilevel submodeling technique and the VCCT are used for calculation of the crack driving force at relevant interfaces under the outermost solder ball.[8,9] ERRs were calculated for horizontal cracks placed at each metal level at the most crack-prone interfaces between the etch stop/passivation (ESL) and the low-k dielectric or the air-gap. Each crack is 0.1 μm wide and 2 μm long, extending in the wiring direction as shown in Figure 4.

In a full low-k integration scheme, the ERR is highest for crack 3 at the M3 interface due to the elastic mismatch between SiO_2 and the low-k layer. The effect of air-gap implementation was first examined for an across-level full air-gap structure where air gaps replace all the intermetal dielectrics (IMD) across M3. This led to a dramatic increase of about 5x in the ERR for crack 3. It should be noted that the value of ERR depends on the size of the crack used in the calculation. Since only one crack size was used, the result from this calculation can provide only a qualitative guideline to evaluate the mechanical stability of the air-gap structures. As the crack propagates, the ERR will further increase. Nevertheless, such a large increase in the ERR should be considered as a serious stability risk. For this reason, we compared those ERR values with the ERRs obtained for a partial air-gap structure where only the dielectrics between dense metal lines is replaced by air gaps as in the case of selective gap formation. This resulted in significant reduction of the ERRs. The results again confirm that the air-gap dimension is a critical parameter in controlling the mechanical stability subjected to chip-packaging interaction. Air-gap-specific design is essential to implement a robust air-gap interconnect structure, especially for schemes using across-level gap-forming IMD material.

Conclusion

Our investigation of the mechanical stability issues associated with air-gap formation has found that the structural integrity issues are not as insurmountable as they initially appeared. With proper design changes and material selection, these issues can be managed. However, the biggest challenge comes from the external stresses during processing and packaging. The size of the air gaps must be limited. Selective air-gap formation to control the gap dimension appears to be inevitable.

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