Thermo-Mechanical Reliability of 3-D ICs containing Through Silicon Vias

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Abstract

In 3-D interconnect structures, process-induced thermal stresses around through-silicon-vias (TSVs) raise serious reliability issues such as Si cracking and performance degradation of devices. In this study, the thermo-mechanical reliability of 3-D interconnect was investigated using finite element analysis (FEA) combined with analytical methods. FEA simulation demonstrated that the thermal stresses in silicon decrease as a function of distance from an isolated TSV and increase with the TSV diameter. Additional simulation suggested that hybrid TSV structures can significantly reduce the thermal stresses. An analytical stress solution was introduced to deduce the stress distribution around an isolated TSV, which was further developed to deduce the stress interaction in TSV arrays based on linear superposition of the analytical solution. We calculated the crack driving force in TSV lines under a thermal load. The effects of TSV diameter, pitch size, and the line configuration on crack driving force were investigated.

Introduction

With continuing device scaling, traditional wiring design imposes significant challenges on the device performance, power dissipation, and packaging form factor. This has recently generated great interests in developing 3-D integration [1,2]. While the current effort has been focused on the design and processing development, the reliability challenges due to 3-D integration cannot be overlooked. Specifically, the incorporation of intra-stratum TSVs brings significant impacts to the thermo-mechanical reliability of 3-D interconnects. Due to the thermal expansion mismatch between constituent materials, the fabrication of TSVs can induce thermal stresses to degrade the performance of stress-sensitive devices. It has been reported that 100 MPa of stress can change more than 7% of carrier mobility in MOSFET devices [3]. In addition, the thermal stresses can drive cracks in silicon substrates to cause device failure [4]. Various approaches were taken in the past to address these reliability issues. For example, FEA was performed to determine the stresses developed during the manufacturing process [5,6], and various via filling designs [7,8] were proposed to minimize the thermal stresses generated by the TSVs.

In this study, we calculate first the thermal stress of single TSV with various structural configurations. FEA simulation and analytic calculation are used to characterize the stress distribution around an isolated copper TSV embedded in silicon matrix. Then the methodology will be extended to analyze the stress interaction in TSV arrays. Based on the stress characteristics of single TSV, we are able to examine the constructive/destructive stress interaction between TSVs. Finally, the crack driving force induced by the thermal stresses around TSVs is evaluated with the objective to identify important factors to control the crack driving force in TSV interconnects and to develop design rules to improve the reliability of TSV structures.

FEA Stress Simulation of Copper TSVs

To study the thermal stress distribution of an isolated copper TSV, three TSV structures were first investigated by FEA simulation, including a. full copper filling, b. annular copper filling, and c. full copper filling with a polymer liner between copper and silicon. The cross-sections of these three structures are depicted in Figure 1. A rotationally symmetric FEA model was created for these structures. The process-induced thermal stresses were calculated by an element-birth-and-death technique following the manufacturing steps. Table 1 lists the simplified process steps for the FEA simulation:

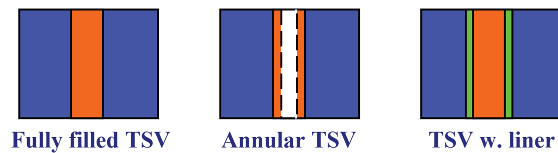

FIGURE 1. Cross-section of TSV structures

TABLE 1. Simplified process steps for FEA simulation

Process Step	Description	Temperature (^{o}C)
1	TEOS deposition	400
2	Ti barrier layer deposition	375
3	Cu electroplating	25
4	Annealing	200
5	Cooling	25

After simulating the manufacturing processes of TSVs, the residual thermal stress on the surface of silicon substrate was examined. Figure 2 shows the radial stress distribution around fully filled TSVs of different via radii. We found that the stress in silicon generally decreases with distance from the fully filled copper TSV but increases with the TSV radius. The thermal stress around a smaller TSV decays much faster away from the via edge, so the area of keep-away-zone for stress sensitive devices becomes also smaller. For instance, if the tolerable residual stress is 100MPa, the keep-away distance from a TSV with 5μm and 15μm radius is 5.5μm and 17μm from the via edge, respectively. The simulation results suggest that scaling down the TSV radius is very beneficial to reduce the thermal stress as well as the area of keep-away-zone.

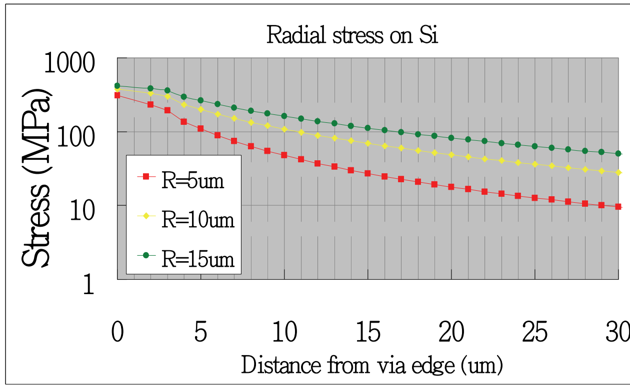

FIGURE 2. Thermal stress around fully filled TSVs

The thermal stresses induced by 10μm radius TSVs with different structures are compared in Figure 3. The thermal stress on the silicon surface is reduced with a thinner copper filling in the annular TSV structure. The stress in silicon can be further reduced by introducing a soft polymer liner, such as benzocyclobutene (BCB), at the side wall between the copper and the silicon substrate. The results show that the annular structure and a compliant side wall can reduce the process-induced thermal stresses.

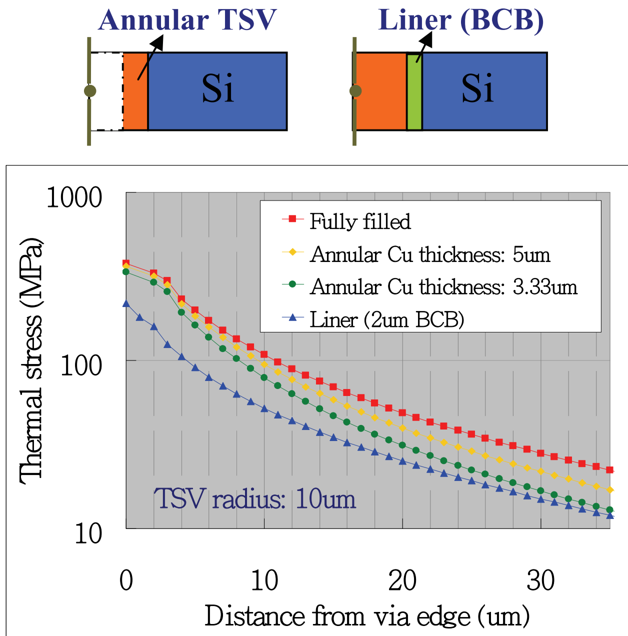

FIGURE 3. Thermal stress around TSVs with various structures

In 3-D ICs, groups of TSVs are usually incorporated in array configurations. The thermal stress interaction in the space between TSVs is of interest to us. To investigate the thermal stress distribution in a TSV array, we set up another 3-D FEA model containing a two-by-two copper TSV array. The process-induced stresses were calculated following the same manufacturing steps as the previous single via analysis, and the residual stresses on the die surface were extracted afterwards. The von Mises stress and normal stress (σ_x) distribution are plotted in Figure 4(a) and 4(b), respectively, in arbitrary units. In both cases, stresses are intensified along the *x*- and *y*- directions but suppressed along the diagonal directions. The major difference between Figure 4(a) and 4(b) is the stress distribution characteristic. In a Cartesian coordinate system, the distribution of von Mises stress around an isolated TSV is axially symmetric, just like the radial stress distribution in a cylindrical coordinate system. In an infinite square TSV array, the distribution of von Mises stress is of four-fold rotational symmetry due to the stress interaction between adjacent TSVs. On the other hand, the normal stress distribution is of two-fold rotational symmetry with tensile stress concentrated on one axis and compressive stress concentrated on the other axis. According to the stress analysis, the keep-away-zone may not be axially symmetric around each TSV due to the stress interaction between TSVs. The keep-away-zone around each TSV can be of two- or four-fold symmetry depending on the piezoresistance characteristics of the stress-sensitive devices.

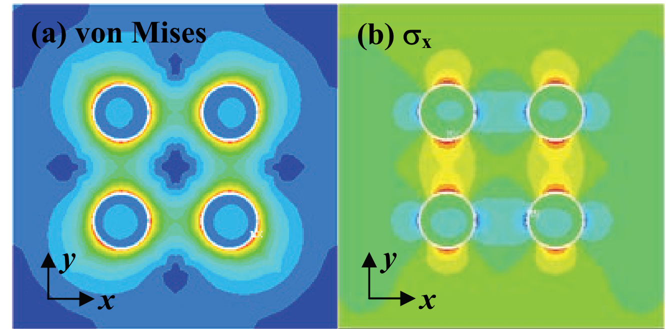

FIGURE 4. FEA simulation of a 2x2 TSV array

Analytical Plane Strain Approximation

For better understanding of the thermal stress characteristic of TSVs, we introduced a 2-D plane-strain analytical solution, known as Lamé stress solution [9], to evaluate the thermal stresses around an isolated TSV. Consider an infinitely long TSV embedded in an infinite matrix. The stress field in the matrix induced by a differential thermal load can be expressed as:

$$\sigma^m{}_{rr} = -\sigma^m{}_{\theta\theta} = -\frac{B\Delta\alpha\Delta T}{2}\left(\frac{R}{r}\right)^2 \quad (1)$$
$$\sigma^m{}_{zz} = \sigma^m{}_{rz} = \sigma^m{}_{\theta z} = \sigma^m{}_{r\theta} = 0$$

where *m*, *B*, $\Delta\alpha$, ΔT, *R*, and *r* signify the matrix, biaxial modulus, mismatch in coefficient of thermal expansion (CTE), differential thermal load, radius of TSV, and the distance away from the center of TSV. The elastic mismatch between TSV and the silicon matrix is neglected for simplicity. Equation 1 clearly reveals the radial-distance dependence of the thermal stresses around an isolated TSV.

The thermal stress increases with square of the TSV radius and decreases with square of the distance away from the TSV. Figure 5 re-plots the FEA results of thermal stress distribution (in Figure 3) as a function of normalized distance, *r/R*, around fully filled TSVs with different via radii. The stress distributions are almost the same with respect to the normalized distance for all TSV sizes. The slope of three curves in this log-log plot is close to -2, as expected from the analytical solution, Equation 1. It suggests the 2-D plane-strain solution can provide a reasonable approximation to characterize the thermal stress of TSVs.

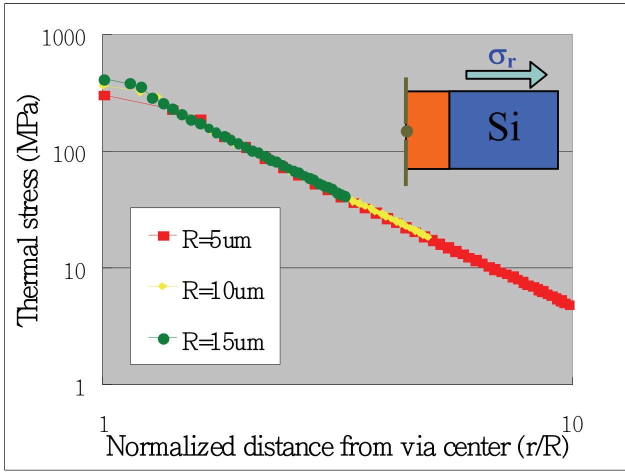

FIGURE 5. Thermal stress around fully filled Cu TSVs

Microelectronic devices are always manufactured in rectangular configurations. Therefore it is reasonable to examine the thermal stress distribution in a Cartesian coordinate system. After the coordinate transformation, Equation 1 can be rewritten as:

$$\sigma^m{}_{xx} = -\sigma^m{}_{yy} = -\frac{R^2 B\Delta\alpha\Delta T(x^2 - y^2)}{2(x^2 + y^2)^2}$$
$$\sigma^m{}_{xy} = -\frac{R^2 B\Delta\alpha\Delta Txy}{(x^2 + y^2)^2} \qquad (2)$$
$$\sigma^m{}_{zz} = \sigma^m{}_{yz} = \sigma^m{}_{zx} = 0$$

where the TSV is located at the origin. Figure 6 shows the calculated normal and shear stress distribution around an isolated, 10μm radius copper TSV in a Cartesian coordinate system, under a -175°C of thermal load. It is seen that tensile and compressive stresses are concentrated along mutually perpendicular directions around the TSV. The stress distribution exhibits similar two-fold rotational symmetry as shown previously in Figure 4(b).

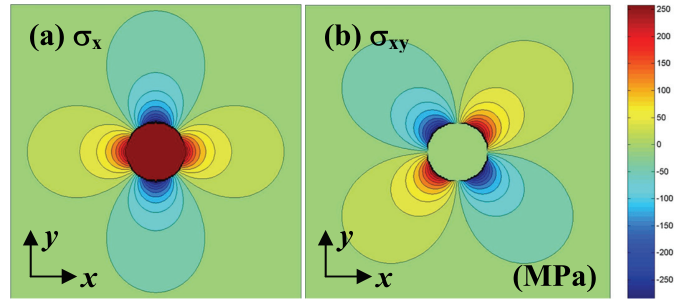

FIGURE 6. Thermal stress approximation around single TSV

In 3-D integration, the interaction of the stress field between the TSVs has to be taken into account in assessing the keep-away-zone. The stress interaction coming from adjacent TSVs were deduced using a linear superposition of the analytical solution. Figure 7 shows the stress interaction between two TSVs in a Cartesian coordinate system. When two TSVs are aligned along the *y*- direction, the normal stress is intensified and the shear stress is suppressed in the space between TSVs, as shown in Figure 7(a) and 7(b). In contrast, the normal stress is suppressed and the shear stress is intensified while two TSVs are aligned in the diagonal direction, as shown in Figure 7(c) and 7(d). It suggests that the stress interaction between TSVs is directional dependent, and the TSV arrays can be arranged accordingly to minimize the thermal stresses.

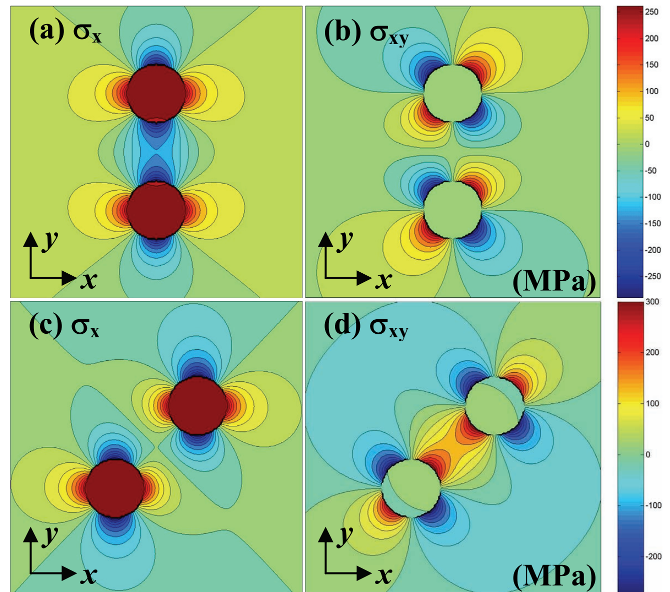

FIGURE 7. Thermal stress interaction between two TSVs

It is interesting to note that there exist stress-free points in the space between two TSVs as a result of destructive stress interaction. Figure 8 shows the von Mises stress distribution surrounding two TSVs under a -175°C of thermal load. Provided that two TSVs are located at the diagonal corners of a square, the other two corners of the square come out as stress-free points. According to Equation 1, the radial stress

from one TSV is canceled by the hoop stress from the other TSV at stress-free points, and all other stress components are also zero. The stress-free points exist regardless of the array orientation, as illustrated in Figure 8(a) and 8(b). Similar stress characteristics can be found in a rectangular TSV array. In Figure 4(a), the low stress trough in the center region of the array is formed by the stress cancellation of the nearby TSV pairs.

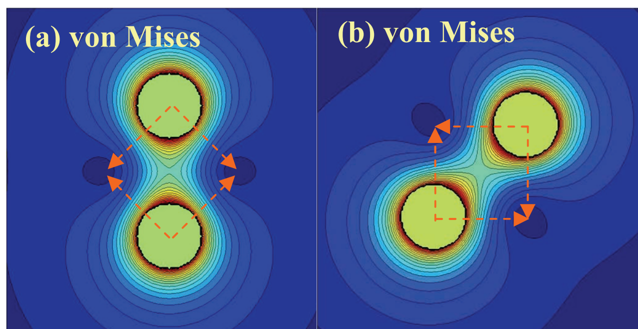

FIGURE 8. Stress-free points between two TSVs

The thermal stress distribution depends on the TSV array configuration, and the keep-away-zone design can be optimized by properly rearranging the array while retaining the same TSV density. The analytical plane strain approximation provides a fast and easy way to evaluate TSV array design from the thermo-mechanical perspective. Following is a simplified example. Assuming the channel directions of MOSFET devices are manufactured along the axial directions and only sensitive to normal stresses in silicon. The normal stresses of two TSV arrays under a -175°C of thermal load were calculated by the plane strain solution and plotted in Figure 9. These two TSV arrays have the same TSV density but different array orientation. Provided that the tolerable normal stress is within ±100 MPa, the TSV array configuration in Figure 9(b) yields a smaller area of keep-away-zone, outlined by rectangles, compared with that in Figure 9(a).

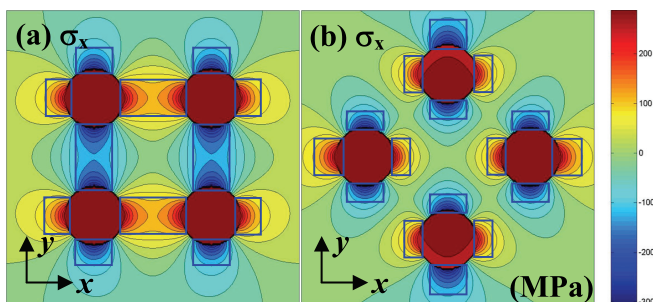

FIGURE 9. Normal stress distribution in two TSV arrays

Thermal Stress Induced Crack Driving Force

Thermal annealing is an important and inevitable process step in 3-D integration. During annealing, copper TSVs expand more than the silicon matrix. Therefore, tensile hoop stress as well as crack driving force builds up in the silicon matrix. An analogous fracture behavior, matrix cracking in intermetallic composites, has been well studied by Lu et al. [9]. We applied similar approaches to investigate the thermal stress induced crack driving force in TSV interconnects.

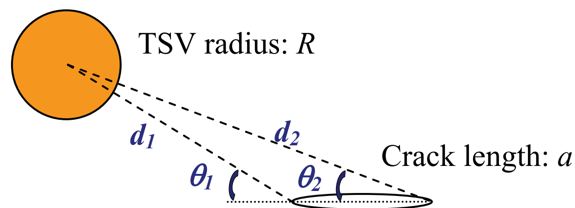

FIGURE 10. Scheme for stress intensity factor calculation

Figure 10 illustrates a through crack along with a TSV in an infinite plane. Under a differential thermal load, the mode I stress intensity factor, K_I, induced by the thermal expansion mismatch of an isolated TSV can be expressed by [9,10]:

$$K_I = R^2 B \Delta\alpha \Delta T \sqrt{\frac{\pi a}{8 d_1 d_2^{\,3}}} \cos\left(\frac{\theta_1}{2} + \frac{3\theta_2}{2}\right) \quad (3)$$

where d_1, d_2, θ_1 and θ_2 are defined in Figure 10. In a TSV array, the stress intensity factor is the linear superposition of K_I contributed by each TSV. In this study, the stress intensity factor on a radial crack was calculated for TSV lines under a +175 °C of thermal load, and TSV lines with various via radii R and pitch sizes L were compared. The cracking direction was aligned with the direction of TSV line for simplicity.

A straight line as well as a zigzag line is depicted in Figure 11 for crack driving force calculation. The TSV density along the line is the same for both arrangements; however, zigzag lines possess an extra angular term in Equation 3 while the angular term vanishes for straight lines in calculation. Consequently, zigzag TSV lines are expected to yield a lower crack driving force in comparison with straight TSV lines.

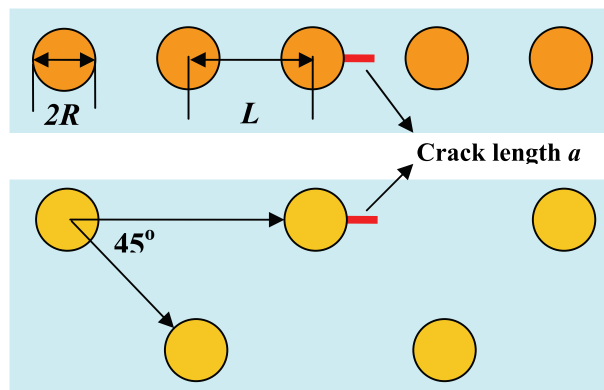

FIGURE 11. Straight and zigzag TSV lines

The effects of TSV diameter and pitch size were investigated in the straight line configuration [Figure 12]. It is shown that K_I increases monotonically with normalized crack length *a/R*, and rises significantly with the via radius. On the contrary, K_I decreases with increasing pitch size. If the pitch size approaches infinity, K_I will converge toward that induced by a single TSV, which is plotted in dash lines in Figure 12.

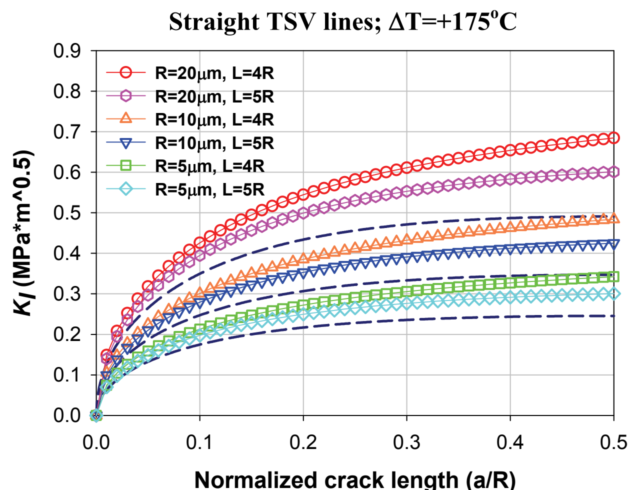

FIGURE 12. Stress intensity factor in straight TSV lines

The comparison between straight TSV lines and zigzag TSV lines is plotted in Figure 13. Given the same TSV line density and via radius, zigzag lines yield a lower stress intensity factor on the radial crack emanating from the center via. The K_I values induced by single TSV were plotted in dash lines again, and there is only minimum difference between single TSV and the zigzag structure. The result suggests the zigzag structure effectively suppresses the crack driving force and improve the thermo-mechanical reliability.

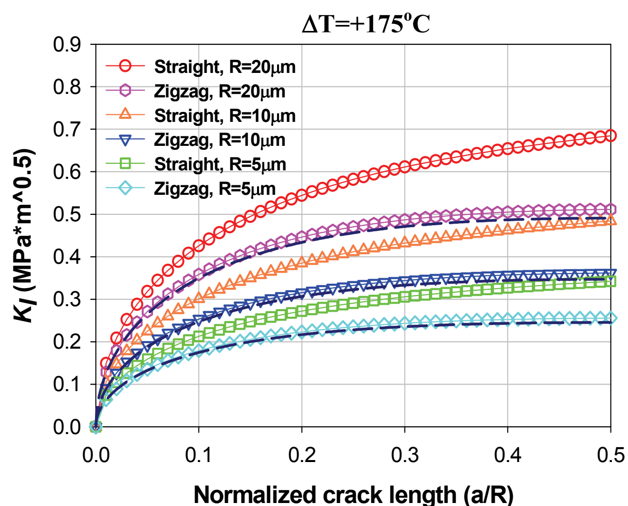

FIGURE 13. Straight vs. zigzag TSV lines

Conclusions

The thermo-mechanical characteristics of TSV interconnect was studied by FEA modeling and analytical methods. The distance-to-radius ratio was identified as an important parameter to determine the thermal stress level around an isolated TSV. According to FEA simulation, significant stress reduction can be achieved by introducing hybrid TSV structures. The thermal stress interaction due to proximity of TSVs was developed by the linear superposition of 2-D plane strain approximation. The stress interaction is directional dependent, and the area of keep-away-zone can be optimized by rearranging TSV array configurations. The driving force for radial crack growth in silicon matrix increases mainly with the TSV radius but decreases with the distance between TSVs. Rearranging TSV arrays can suppress the crack driving force and improve the thermo-mechanical reliability of the TSV interconnects.

References

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