The other stress function $\psi(\zeta)$ can be derived directly by analytic continuation along the traction-free boundary of the unit circle as

$$\psi(\zeta) = -\overline{\varphi(1/\bar{\zeta})} - \frac{\overline{\omega(1/\bar{\zeta})}}{\omega'(\zeta)}\varphi'(\zeta) \qquad (28)$$

or can be obtained from the Cauchy integral of the conjugate form of (19).

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Thermal Stress in 3-D Packaging

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Overview

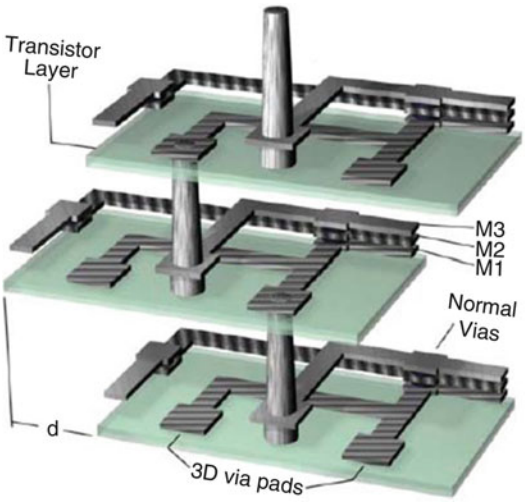
The thermal stresses in the 3-D packaging originate from the large mismatch in the coefficients of thermal expansion (CTEs) between the materials used in the 3-D structures. Especially, the CTE mismatch between the through-silicon via (TSV), which is an essential component in 3-D packaging, and the Si matrix is the main cause of structural failures in the 3-D packaging. The characteristics of the thermal stress are complex

and three dimensional (3-D) in nature. Depending on the TSV design, material, and processing conditions, the thermal stresses can lead to a variety of failure modes during fabrication, testing, and service of the 3-D structures. Understanding the characteristics of the thermal stresses is important for improving the design and reliability of 3-D packages.

This entry aims at providing a basic understanding of the characteristics of the thermal stresses and the thermomechanical reliability issues of the 3-D structures containing TSVs. First, the background of 3-D integration and packaging is introduced. Next, the thermomechanical reliability issues caused by the thermal stresses are reviewed, which highlights the importance of thermal stresses in 3-D packaging. Then, the characteristics of the thermal stresses in TSV structures are discussed based on both analytical and numerical approaches. This is followed by the discussion of the effects of anisotropic mechanical properties of Si and Cu plasticity on the thermal stresses. In the end, various experimental techniques for stress measurement are reviewed.

3-D Integration

Over the past decades, the microelectronics industry has been driven by Moore's law to continuously scale down device dimensions and increase circuit speed [1]. In recent years, the industry has encountered major technology barriers in scaling, such as the interconnect delay, also known as the resistive-capacitive (RC) delay [2]. In addition, there is an increasing demand to minimize the dimension of electronic packages, particularly for consumer electronic products such as mobile devices. To overcome such difficulties, a potential solution has been proposed at the packaging level, which is the implementation of three-dimensional (3-D) integration. Comparing to the conventional 2-D integrated structure, where long edge wiring is used, in the 3-D integration, two or more chips are stacked vertically and connected by through-silicon vias (TSVs), as illustrated in Fig. 1 [3]. For the TSV structures,



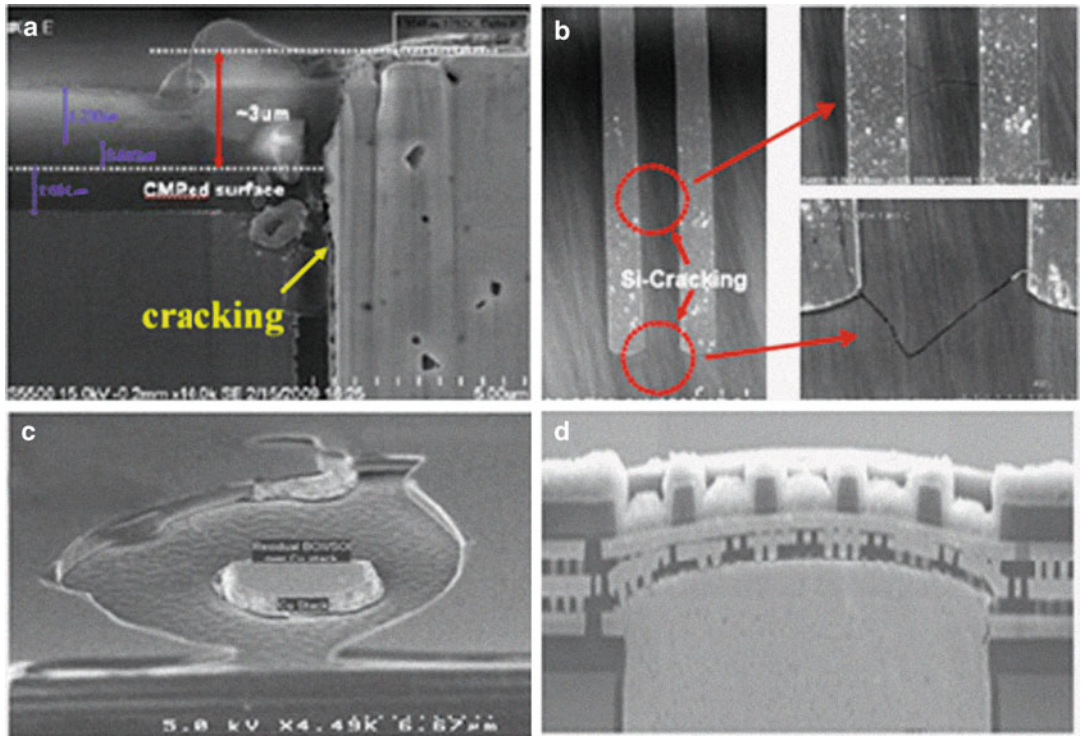
Thermal Stress in 3-D Packaging, Fig. 1 Illustration of 3-D integration with TSVs [3]

Cu is widely used because Cu is compatible with the conventional FEOL and BEOL processes and has appropriate properties.

The 3-D integration approach offers many advantages, such as improved electrical performance and reduced power consumption. Furthermore, 3-D integration allows higher device density and smaller packaging size, which eventually would lead to reduced manufacturing cost [4]. Therefore, 3-D integration presents an effective solution to overcome the wiring limit imposed on chip performance, density, and power consumption beyond the current technology [5, 6].

Thermomechanical Reliability of 3-D ICs

While 3-D integration with TSVs offers a promising solution for future technology nodes, serious thermomechanical reliability concerns have been raised, largely due to the CTE mismatch between the Cu vias and the Si wafer ($\alpha_{Cu} = 17$ ppm/C and $\alpha_{Si} = 2.3$ ppm/C). During fabrication of the TSV structure, which usually involves processes at various temperatures, thermal stresses are ubiquitously generated [7]. The thermal stresses can cause serious reliability issues in the integrated structure. For example, interfacial failure of the TSV (Fig. 2a) and



Thermal Stress in 3-D Packaging, Fig. 2 Thermomechanical issues in TSV structures (Source: Samsung [8]): (**a**) Interfacial delamination; (**b**) silicon cracking; (**c**, **d**) Via extrusion (Pop-up)

cracking in Si near the bottom of TSVs (Fig. 2b) have been observed [8]. Extrusion of Cu vias (via pop-up) is often observed in the TSV structures undergoing high temperature excursion, as shown in Fig. 2c. The via extrusion can be accompanied by interfacial delamination and can push up the upper dielectric layers, causing structural failure, as shown in Fig. 2d. The effects of Cu plasticity could also play an important role in via extrusion and need to be considered in studying the thermal stresses in TSV structures. In addition, the thermal stress can cause mobility degradation of carriers in Si surrounding the TSVs, therefore affecting performance of nearby devices. To prevent device performance degradation, a keep-out zone (KOZ) may be defined around the TSVs, which requires the analysis of thermal stresses near the surface where the electronic devices are located [9]. For successful implementation of TSVs in 3-D integration, it is essential to understand the characteristics of the thermal stresses and their impacts on thermomechanical reliability.

Analysis of Thermal Stresses

To study the thermal stresses in TSV structures, analytical and numerical approaches have been used. As a numerical approach, finite element methods (FEM) have been used to analyze the thermal stresses in 3-D integrated structures, and specific materials, processing, and structural designs can be taken into consideration [10–12]. Analytically, a simple approach based on a 2-D plane strain analysis has been used to analyze the thermal stresses. The classic Lame solution is extended to give the stress components in the via as in the following [13]:

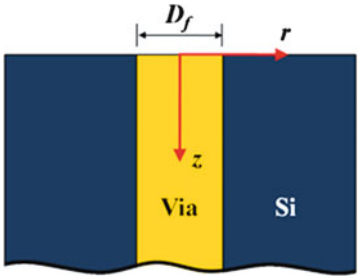
$$\sigma_r = \sigma_\theta = \frac{-E_f \varepsilon_T}{1 - 2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}} \tag{1}$$

$$\sigma_z = -E_f \varepsilon_T \left[\frac{1 + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}}{1 - 2\nu_f + \frac{1+\nu_m}{1+\nu_f}\frac{E_f}{E_m}} \right] \tag{2}$$

where σ_r, σ_θ, and σ_z are the radial, circumferential, and axial stresses, respectively, and $\varepsilon_T = (\alpha_f - \alpha_m)\,\Delta T$ is the mismatch strain due to the thermal load ΔT. The material properties, α, E, v, are the coefficient of thermal expansion (CTE), Young's modulus, and Poisson ratio, with the subscripts f and m for the Cu via (fiber) and Si (matrix), respectively. The stress in the via is uniform and triaxial. On the other hand, the corresponding stress field in Si ($r > D_f/2$) is nonuniform and biaxial:

$$\sigma_r = -\sigma_\theta = \frac{-E_f \varepsilon_T}{1 - 2v_f + \frac{1+v_m}{1+v_f}\frac{E_f}{E_m}} \left(\frac{D_f}{2r}\right)^2 \quad (3)$$

where D_f is the diameter of the TSV and r is the radial coordinate measured from the center of the via (Fig. 3).



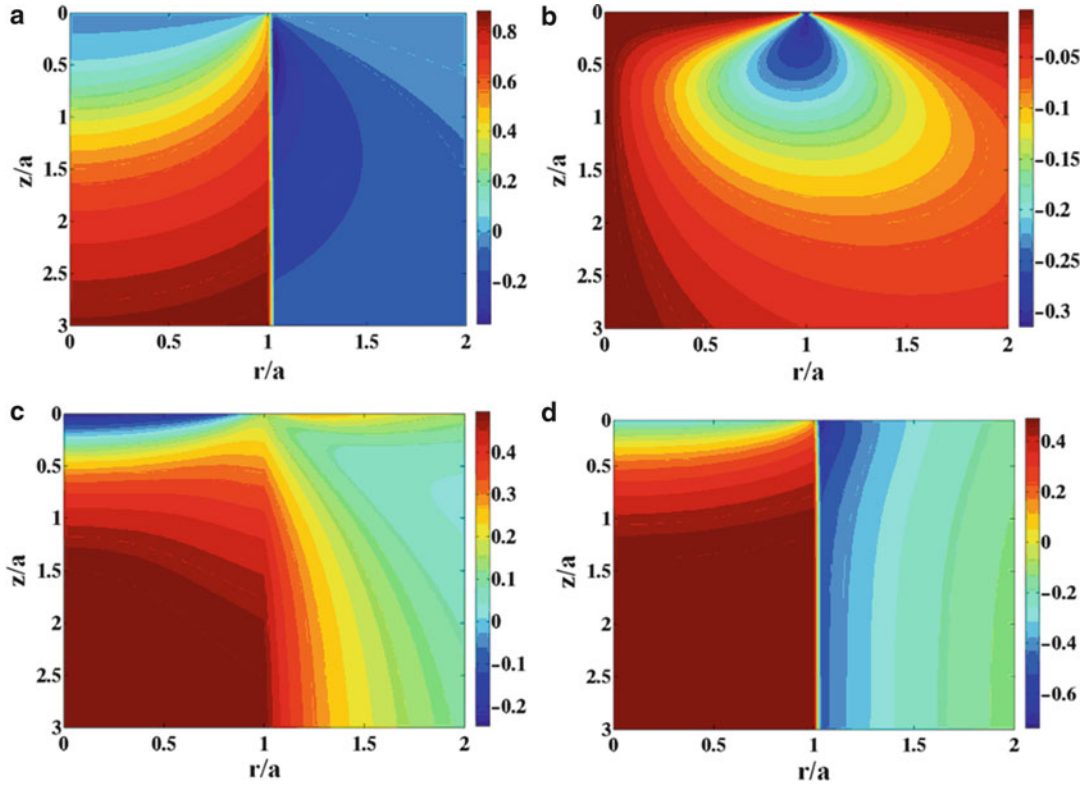
Thermal Stress in 3-D Packaging, Fig. 3 A simplified TSV structure

The 2-D solution has been employed in studying the interaction of thermal stresses in TSV arrays. However, the 2-D solution does not capture the 3-D nature of the stress field near the wafer surface around a TSV. Determination of the 3-D near-surface stress distribution is critical as the active devices are usually located near the wafer surface. For this purpose, a semi-analytic 3-D solution has been developed for an isolated TSV embedded in the silicon wafer [13]. Due to limited space, the mathematical derivation and final solutions for the 3-D near-surface stresses are not presented here. Instead, the results are presented graphically in Fig. 4, showing the distribution of the stress components. Fig. 4a shows that the normal stress σ_z is zero on the surface ($z = 0$), as required by the traction-free boundary condition. Unlike the 2-D solution, the stress in the via is nonuniform near the surface. Moreover, a concentration of the shear stress (σ_{zr}) is predicted at the junction between the surface ($z = 0$) and via/Si interface ($r = D_f/2$), which may contribute to the driving force for interfacial delamination. The distributions of the radial stress (σ_r) and the circumferential stress (σ_θ) near the end of the TSV (Fig. 4c and d) are also distinct from the predictions by the 2-D solution. Depending on the sign of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$, the stresses can be either tensile or compressive. For example, if $\alpha_f > \alpha_m$, $p < 0$ for heating ($\Delta T > 0$) and $p > 0$ for cooling ($\Delta T < 0$), where $p = -E\varepsilon_T/(1 - v)$. For the case of cooling ($\Delta T < 0$), the radial stress is tensile along the via/Si interface, which can contribute to the driving force for interfacial delamination. The radial stress is also tensile in Si near the surface, which may cause circumferential cracking (C-cracks) of the Si. During heating ($\Delta T > 0$), the circumferential stress is tensile in Si, which may cause radial cracks (R-cracks) in Si. For both heating and cooling, the presence of the shear stress (σ_{rz}) along the TSV/Si interface can cause interfacial failure by delamination.

Figure 5 compares the 3-D semi-analytic solution with the 2-D plane solution and numerical results by FEA. The axial stress (σ_z) along the center line of the TSV ($r = 0$) shows the transition from zero stress at the surface ($z = 0$) to a tensile stress away from the surface (Fig. 5a). For a thick wafer ($H/D_f = 10$), the FEA result shows good agreement with the 3-D analytical solution, both approaching the 2-D solution (the dashed line) away from the surface. For a thin wafer ($H/D_f = 2$), however, the axial stress in the TSV is significantly lower due to the close proximity of the two free surfaces. Similar results for the shear and radial stresses along the TSV/Si interface ($r = D_f/2$) are shown in Fig. 5b and c, respectively.

Effect of Cu Plasticity

The fabrication of TSV structures typically requires processing at high temperatures. Depending on the fabrication process, the Cu

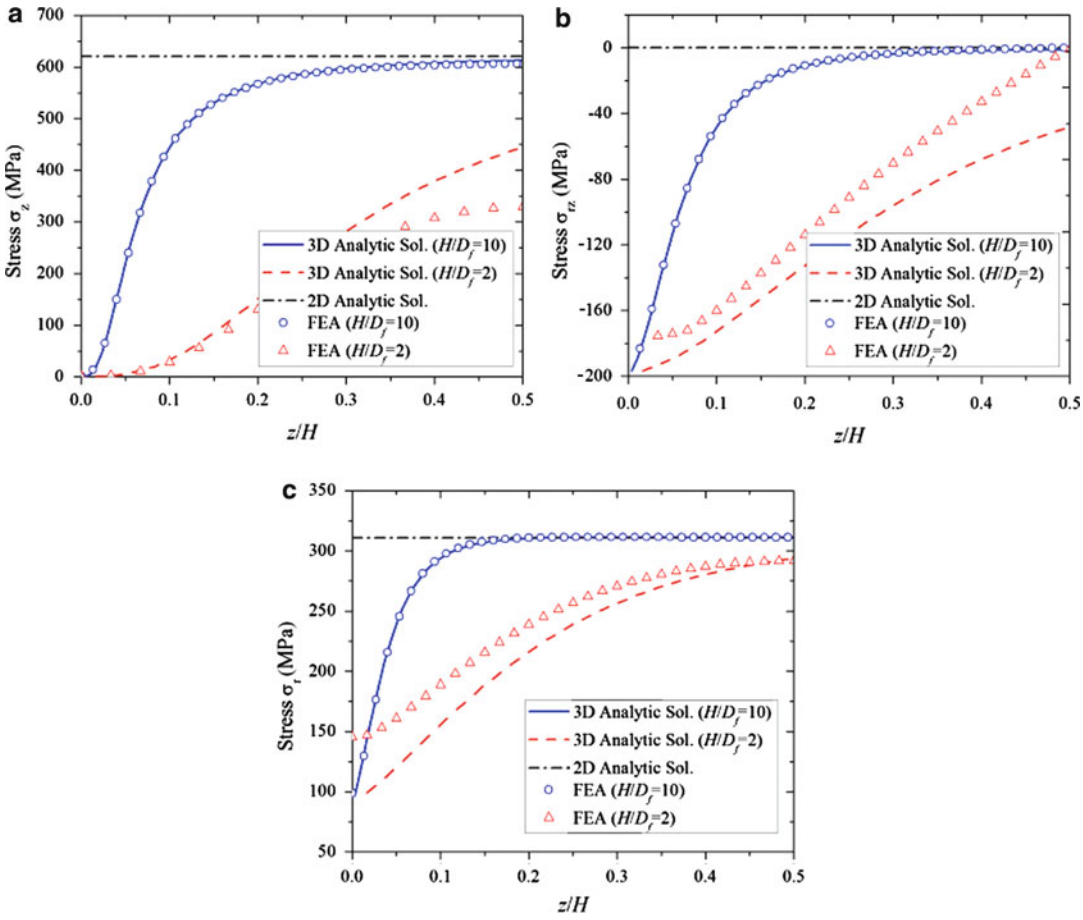


Thermal Stress in 3-D Packaging, Fig. 4 Near-surface stress distributions predicted by the semi-analytical solution. The stress magnitudes are normalized by $p = -E\varepsilon_T/(1-\nu)$, and the radial and depth coordinates (r and z) are normalized by the via radius $a = D_f/2$: (**a**) out-of plane stress (σ_z); (**b**) shear stress (σ_{rz}); (**c**) radial stress (σ_r); (**d**) circumferential stress (σ_θ)

via could experience plasticity when subjected to a positive or a negative thermal load. For example, after Cu plating, the TSV structures need to be heat up to temperatures as high as 400 °C for the deposition of additional passivation layers (TEOS or SiN). During such processes, the TSVs undergo positive thermal loads that are large enough to cause plasticity in the via. Plasticity could also develop in the via during cooling process if stress relaxation occurs at the high temperatures. The plasticity effects could significantly change the stress behavior and thus impact the thermomechanical reliability for TSV structures.

The effects of plasticity on thermal stresses in TSV structures are investigated for both positive and negative thermal loads using finite element analysis. The classical metal plasticity model is adopted for the via material, with rate-independent perfect plasticity and a von Mises yield surface for associated plastic flow [14]. In general, the rate-independent model is used to simulate metals deformed at relatively low temperatures (less than half of the material's melting point) and modest strain rates (of order 0.01–10/s).

In the metal plasticity model, a yield surface is defined as the limit of the elastic response. Inside the yield surface, the stress–strain behavior is linear elastic. During plastic flow, the stress state remains on the yield surface with no strain hardening and the plastic strain evolves by the associated flow rule. The von Mises stress or equivalent shear stress (σ_{eq}) is used for the yield criterion, which is defined as



Thermal Stress in 3-D Packaging, Fig. 5 Effect of wafer thickness on stress distributions ($D_f = 30\mu m$ and $\Delta T = -250°C$): (**a**) Axial stress at the via center ($r = 0$); (**b**) Shear stress at the TSV/Si interface ($r = D_f/2$); (**c**) Radial stress at the TSV/Si interface ($r = D_f/2$)

$$\sigma_{eq} = \sqrt{\frac{3}{2} s_{ij} s_{ij}} \tag{4}$$

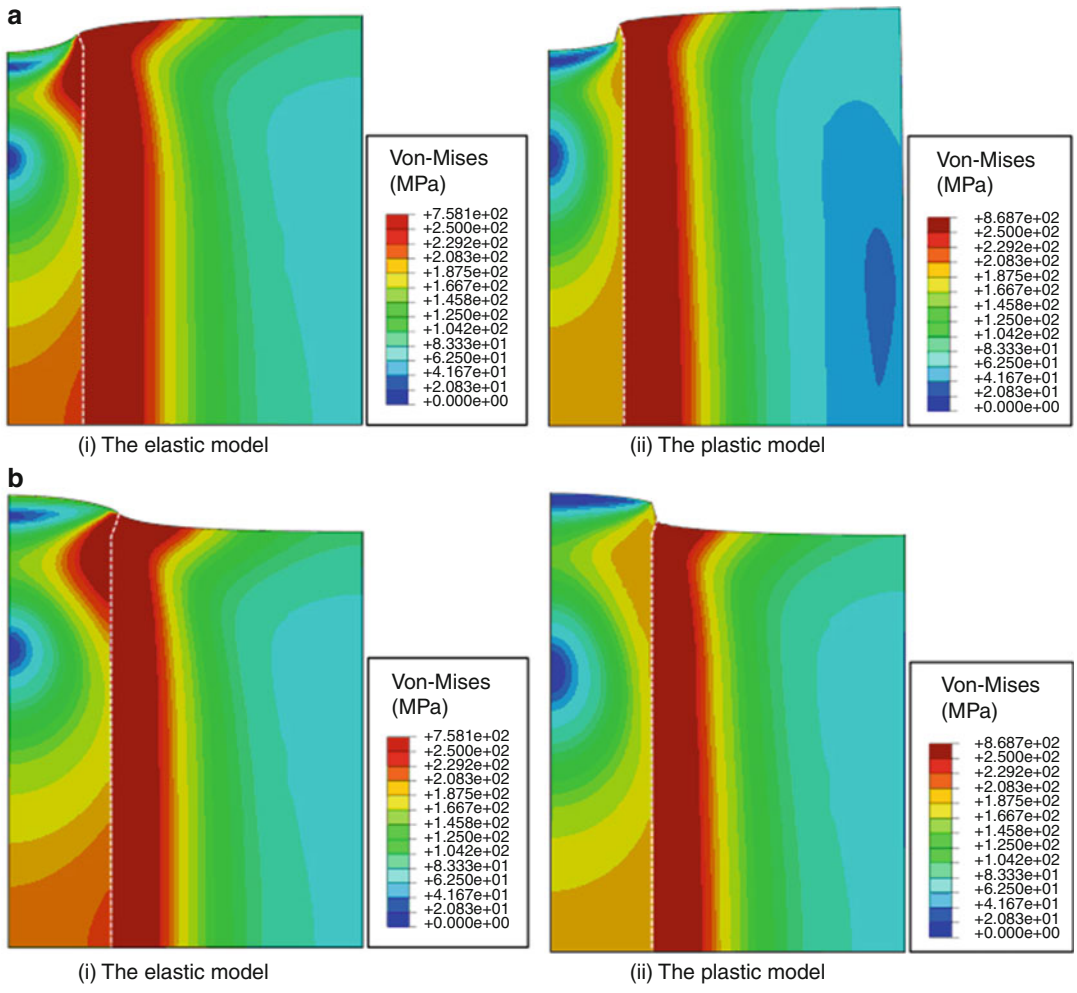
where $s_{ij} = \sigma_{ij} - \frac{1}{3}\sigma_{kk}\delta_{ij}$. Correspondingly, the equivalent plastic strain (ε_{eq}) is used to represent the effective plastic deformation, namely,

$$\varepsilon_{eq} = \sqrt{\frac{3}{2} e_{ij} e_{ij}} \tag{5}$$

where $e_{ij} = \varepsilon_{ij} - \frac{1}{3}\varepsilon_{kk}\delta_{ij}$

Figure 6 shows a comparison of the deformation and the von-Mises stresses from FEA calculations using the elastic model and the plastic model. In the calculations, a TSV structure with $D_f = 30$ μm is considered with thermal loads of $\Delta T = \pm 250$ °C. In the plastic model, the yield strength of the Cu via is taken to be $\sigma_y = 200$ MPa based on previous studies for electroplated Cu films with similar grain sizes [15–17]. As shown, the maximum von-Mises stress in the via for the elastic model exceeds the yield strength. In the plastic model, due to plastic yielding of the via material, the maximum von-Mises stress in the via equals the yield strength. It is noted that the plastic deformation is largely confined to a small volume near the junction between the via/Si interface and the wafer surface.

Due to the limited amount of plastic deformation, the stress distributions in Si around the

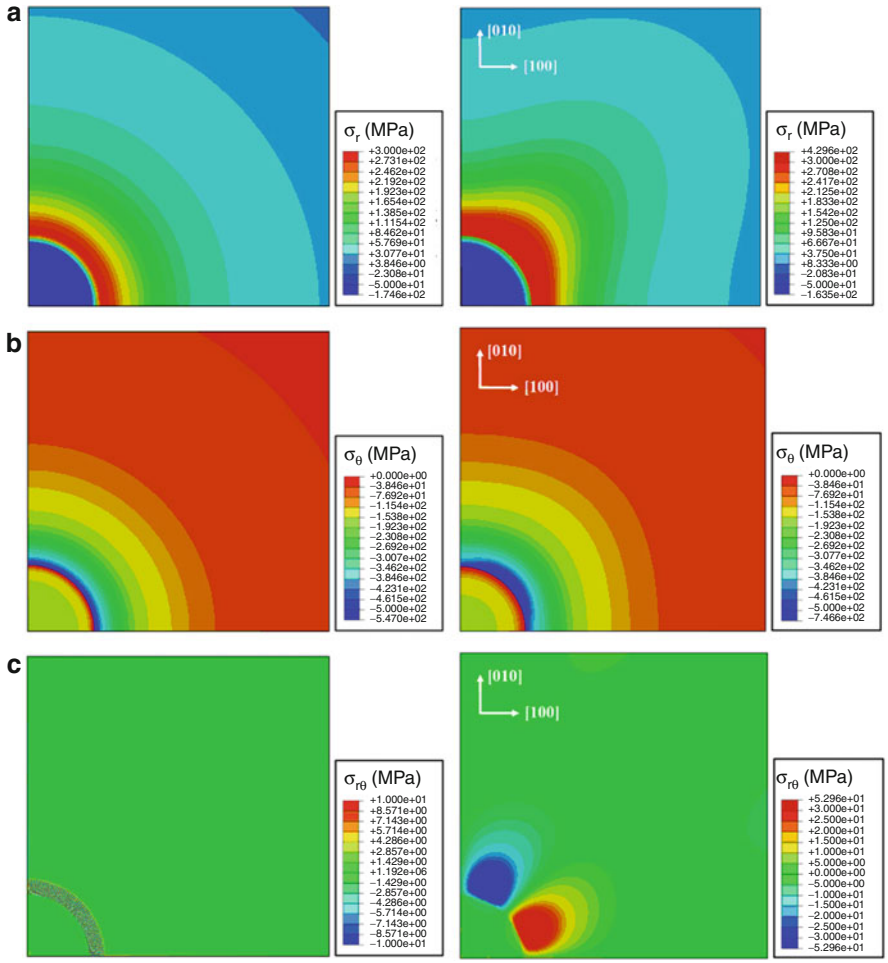


Thermal Stress in 3-D Packaging, Fig. 6 Comparison of stress distribution and deformation between an elastic and a plastic model with different thermal loads ($D_f = 30\mu m$): (**a**) Cooling with $\Delta T = -250$ °C; (**b**) Heating with $\Delta T = 250$ °C

via are similar in both models. However, the overall deformation obtained by the plastic model is considerably different from the elastic model, especially at the locations near the wafer surface. Under the negative thermal load ($\Delta T = -250^{o}$C), the via surface in the elastic model is deformed to a smooth concaved shape (Fig. 6a). In contrast, the via surface in the plastic model sinks in abruptly near the interface due to local plastic yielding. With a positive thermal load ($\Delta T = 250\ ^{o}$C), Fig. 6b shows that via extrusion is enhanced by the local plastic deformation in the via. The phenomenon of via extrusion has been observed as a common failure mode for TSV structures.

Effect of Elastic Anisotropy of Si

Silicon is an anisotropic material. The orientation of Si wafer is very important for the study of stress characteristics and the impact of stresses on reliability. With FEA, the effect of elastic anisotropy of Si is discussed here. Specifically, the (001) Si wafer, which is the most common



Thermal Stress in 3-D Packaging, Fig. 7 Effect of anisotropic elasticity on stress distributions ($D_f = 30\mu m$ and $\Delta T = -250°C$): (**a**) Radial stress, σ_r for isotropic Si (*left*) and (001) Si (*right*); (**b**) Circumferential stress, σ_θ for isotropic Si (*left*) and (001) Si (*right*); (**c**) Shear stress, $\sigma_{r\theta}$ for isotropic Si (*left*) and (001) Si (*right*)

type, is considered. The stiffness matrix of the (001) Si wafer is [18]

$$C_{(001)} = \begin{bmatrix} 166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\ 64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 0 & 79.8 \end{bmatrix} \text{GPa}$$

Figure 7 shows the near-surface distribution of thermal stresses around a TSV, comparing the results from the anisotropic model with an isotropic model with $E = 130$ GPa and $\nu = 0.28$ for Si. In both models, Cu is treated as an isotropic elastic material with $E = 110$ GPa and $\nu = 0.35$. The result from the isotropic model is axisymmetric, with concentric circular contours for both the radial and circumferential stresses. By symmetry, the in-plane shear stress ($\sigma_{r\theta}$) in Fig. 7c is zero everywhere in the isotropic model. However, when the anisotropic elastic property of Si is considered, the stress distribution in the (001) Si is no longer axisymmetric. Instead, it exhibits a fourfold symmetry, reflecting the cubic structure of the Si crystal. In addition, the in-plane shear stresses are not zero near the via.

Measurements of Thermal Stresses

Several experimental techniques, including the μ-Raman spectroscopy, the wafer curvature technique, X-ray diffraction, and the nanoindentation method, have been employed to measure the thermal stresses and characterize the material behaviors in the 3-D structures. Each of the measurement techniques has its own strength and limitations, which are briefly reviewed in this section. These techniques can also be combined to provide a more comprehensive understanding of the thermal stresses in 3-D structures with TSVs.

Raman spectroscopy is a nondestructive technique which relies on the inelastic scattering (or Raman scattering) of the specimen. In the 3-D structure, the thermal stresses in the Cu via induce stresses in the Si matrix surrounding the TSVs, and the presence of strain in Si will result in the frequency shift of the Raman modes. The measured frequency shift can be converted to stresses using the secular equation [19]. By using optical lenses to focus the laser beam, high spatial resolution of less than 1 μm can be achieved in micro-Raman spectroscopy. Raman signal usually penetrates ~0.2 μm from the wafer surface, making this technique suitable for studying the near-surface stresses in Si surrounding TSVs. On the other hand, most Raman measurement systems adopt the backscattering configuration, under which only the sum of the in-plane stresses ($\sigma_r + \sigma_\theta$) can be deduced. From the stress analysis in the 3-D structure, the in-plane radial and circumferential stresses are opposite in sign with almost identical magnitudes. Therefore, the sum of the in-plane stresses is nearly canceled out, making Raman measurement difficult.

Wafer curvature technique has been widely used to measure stresses in thin films and line structures [18]. Recently, it has been extended to evaluate the stresses in periodic Cu/TSV structures [20]. The system for the wafer curvature measurements employs an optical method to monitor the curvature change of the specimen during thermal cycling. With a high precision curvature measurement, it is possible to distinguish elastic and plastic behaviors of the TSV structures. However, unlike the thin film structures, where the average stress in the film can be deduced directly from the curvature using the classic Stoney's equation [18], finite element analysis (FEA) has to be performed to delineate the stress distribution in the TSV structures.

X-ray diffraction is a powerful technique that can study the crystalline phase, grain orientation, as well as strains for a wide range of materials. In recent years, a scanning X-ray microdiffraction (mSXRD) technique has been developed based on synchrotron radiation. Using advanced optics and large-area fast-detector technology, the X-ray beam can be focused to submicron size and scanned across the specimen. The mSXRD technique has been applied to TSV structures, allowing in situ measurement of the stresses in the Cu via and its surrounding Si [21]. From the measurement, grain orientation and triaxial strain in the TSV/Si structure can be obtained [16]. In principle, synchrotron X-ray microdiffraction can measure the local stresses both in Cu and in Si with submicron resolution. However, it requires special facilities that are not widely accessible.

Nanoindentation is an instrumented indentation technique that measures the indentation load and displacement during loading and unloading. From the load–displacement data, the hardness and elastic modulus of the material can be deduced. By using a small indenter tip and well-controlled loading, precise measurement of mechanical properties at small scales can be achieved by this technique. For TSV structures, the mechanical response of the Cu in the TSV can be directly probed. Nanoindentation test has also been used to study the residual stresses in the electroplated Cu vias [22]. Interpretation of the measured indentation data remains a challenge, which often requires numerical simulations.

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Thermal Stress in a Multi-leg Thermoelectric Module (TEM) Design

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Overview

Physically meaningful analytical (mathematical) model is suggested for the prediction of the interfacial shearing thermal stress in an assembly comprised of two identical components, subjected to different temperatures. The bonding system is comprised of a plurality of identical column-like supports located at equal distances (spaces) from each other. The model is developed in application to a thermoelectric module (TEM) design where bonding is provided by multiple thermoelectric material supports (legs). We show that thinner (dimension in the horizontal direction) and longer (dimension in the vertical direction) TEM legs could result in a significant stress relief and that such a relief could be achieved even if shorter legs are employed, as long as they are thin and the spacing between them is significant. It is imperative, of course, that if thin legs are employed for lower stresses, there is still enough interfacial "real estate" so that the adhesive strength of the assembly is not compromised. On the other hand, owing to a lower stress level in an assembly with thin legs and large spacing, assurance of its interfacial strength is less of a challenge than for a conventional assembly with stiff, thick, and closely positioned legs.