Thermomechanical Reliability of Through-Silicon Vias in 3D Interconnects

Kuan-Hsun Lu[1], Suk-Kyu Ryu[2], Jay Im[1], Rui Huang[2] and Paul S. Ho[1]
[1]Microelectronics Research Center
[2]Department of Aerospace Engineering and Engineering Mechanics
University of Texas at Austin
Austin, TX 78712
paulho@mail.utexas.edu

***Abstract*—This paper investigates two key aspects of thermomechanical reliability of through-silicon vias (TSV) in 3D interconnects. One is the piezoresistivity effect induced by the near surface stresses on the charge mobility for p- and n- channel MOSFET devices. The other problem concerns the interfacial delamination induced by thermal stresses including the pop-up mechanism of TSV with a 'nail head'. We first analyze the three-dimensional distribution of the thermal stresses near the TSV and the wafer surface. The stress characteristics are inherently 3D in nature with the near-surface stress distributions distinctly different from the 2D solution. The energy release rate for interfacial delamination of TSV is evaluated under both cooling and heating conditions, using an analytical solution for a steady-state crack growth as an upper bound and numerical solutions by finite element analysis (FEA) for more detailed calculations. Based on these results, we examine the piezoresistivity effect induced by the near surface stresses on the charge mobility for p- and n- channel MOSFET devices, including the study of the effect of TSV scaling on the keep-out zone for MOSFET devices. This is followed by analyzing the energy release rate for interfacial delamiantion for a fully filled TSV and the potential mechanisms for TSV pop-up due to interfacial fracture.**

Keywords-3D interconnect, TSV, Thermo-mechanical reliability, FEA, Crack driving force

I. INTRODUCTION

Three dimensional (3D) integration with through-silicon-vias (TSVs) has emerged as an effective solution to meet the future interconnect requirements beyond the 32nm technology node [1, 2]. The through-silicon via (TSV) is a critical structural element in the 3D interconnects, which directly connects stacked structures die-to-die. The incorporation of TSV structures can significantly impact the thermomechanical reliability of 3D interconnects. The mismatch in thermal expansion between the TSV and Si can induce large thermal stresses during TSV fabrication to degrade the performance of stress-sensitive devices. It has been reported that 100 MPa of stress can change more than 7% of carrier mobility in MOSFET devices [3]. In addition, the thermal stresses can drive interfacial delamination between the TSV and the silicon matrix [4-8], thus the stress impact on device reliability and performance has to be considered in the development of 3-D integrated circuits.

In this paper, we first analyze the characteristics of the thermal stress induced by TSVs. Three-dimensional finite element simulation and analytical solutions are applied to characterize the stress distribution in the Si wafer surrounding an isolated TSV. Here the analysis is focused on the near surface region in the Si surrounding the TSV since most of the devices are located very close (about 1 μm) to the surface. Then we examine two key issues of TSV reliability based on the stress characteristics deduced. One is the piezoresistivity effect induced by the near surface stresses on the charge mobility for p- and n- channel MOSFET devices. Here we extend the study to examine the impact of TSV scaling on the keep-out zone for MOSFET devices. The other issue concerns the interfacial delamination and its impact on TSV reliability. We will deduce an analytical solution for the steady state energy release rate as an upper bound for the fracture driving force. The analysis, together with numerical results using FEA, is used to investigate the mechanism of TSV pop-up due to interfacial delamination.

II. THREE DIMENSIONAL STRESS ANALYSIS

Finite element methods have been used to analyze the thermo-mechanical stresses of TSV structures, which were found to depend on the materials, processes and structural designs of the 3D integrated structures [4-8]. To assess the thermo-mechanical reliability, the driving forces for the growth of both cohesive and interfacial cracks were calculated based on the concepts of facture mechanics [8-10]. So far, the previous studies have focused mainly on the TSV structural reliability and little information was available about the stress behavior near the wafer surface. The latter was required to understand the stress effect on device performance since most of the active devices are located very close to the Si surface. In a recent study, a 2-D analytical solution was deduced to analyze the stress interaction in TSV arrays [11]. The 2D solution, however, does not capture the 3D nature of the stress field near the wafer surface around a TSV. For the present study, we analyze the 3D near-surface stress field around a single TSV embedded in an infinite Si wafer. In this analysis,

we first assume that all materials are isotropic and linear elastic. Under the assumption of linear elasticity, the stress field in the TSV structure can be obtained by superposition of the two problems sketched in Fig. 1. In Problem A, the system is subjected to a thermal loading ΔT and a uniform stress σ_z on the surface of the via, where the stress field is homogeneous in the via. The exact solution to Problem A in Fig. 1 is identical to the 2D plane-strain solution to the classical Lame problem [12]. The 2D solution does not satisfy the traction-free boundary condition on the surfaces in the original problem (Fig. 1a) because of the presence of the axial stress σ_z^A in the via. To recover the traction-free boundary condition, the normal stress on the surface is removed by superimposing Problem B, in which the via is subjected to a pressure of the same magnitude ($p = \sigma_z$) at both ends, but no thermal load [13]. The stress field due to the surface pressure is typically localized near the ends of the via. Thus, the stress distribution from the 2D solution is an accurate solution far away from the TSV ends, especially for TSVs with a high aspect-ratio (height/diameter, H/D_f) embedded in a thick wafer. However, the correction due to Problem B renders a very different stress distribution near the wafer surface around the TSV. For a relatively thin wafer, the stress in the entire via and its surrounding can be affected and thus comes out different from the 2D solution. This can impact the near-surface thermal stress distribution and the device characteristics surrounding the TSV.

Problem A can be solved analytically, while an approximate solution to Problem B can be obtained semi-analytically. The thermal stress in the via is uniform and tri-axial. The detailed solutions can be found in our previous publication [14].

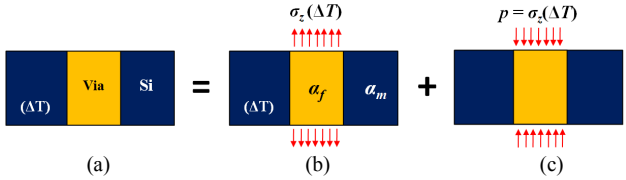
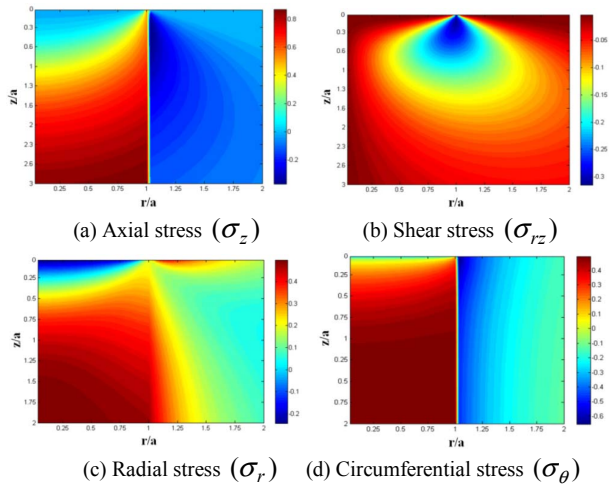


Fig. 1. Illustration of the method of superposition to obtain the semi-analytical solution for the thermal stresses in a TSV structure: (a) the original problem, with a thermal load and traction-free surfaces; (b) Problem A, with a thermal load; (c) Problem B, with surface load only.

Figure 2 shows the distributions of various stresses in the model structure for the negative thermal load, $\Delta T = -250$ ºC. Figure 2a shows that the normal stress σ_z is zero on the surface ($z = 0$), as required by the traction-free boundary condition. The normal stress is non-uniform in the via and Si near the surface. Unlike the 2D solution, the shear stress σ_{zr} is not zero near the end of the via. In fact, a concentration of the shear stress is predicted at the junction between the surface ($z = 0$) and via/Si interface ($r = D_f/2$), which can contribute to the driving force to cause interfacial delamination. The distributions of the radial stress σ_r and the circumferential stress σ_θ near the end of TSV are also very different from the 2D solution (Figs. 2c and 2d).



(a) Axial stress (σ_z) (b) Shear stress (σ_{rz})

(c) Radial stress (σ_r) (d) Circumferential stress (σ_θ)

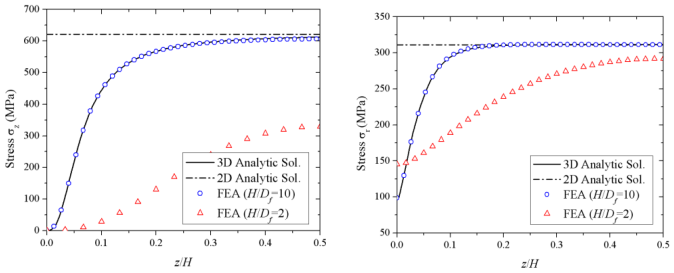
Fig. 2. Near-surface stress distributions predicted by the semi-analytical solution for thermal load, $\Delta T = -250$ ºC. The stress magnitudes are normalized by $p = -E\varepsilon_T/(1-\nu)$.

The fracture behavior depends on the character of the stress components and the sign of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$, which can be either tensile or compressive where the subscripts f and m refer to the TSV and Si, respectively. For example, if $\alpha_f > \alpha_m$, $\varepsilon_T > 0$ for heating ($\Delta T > 0$) and $\varepsilon_T < 0$ for cooling ($\Delta T < 0$). Under cooling, the radial stress is tensile along the via/Si interface, which can contribute to the driving force for interfacial delamination. The radial stress is also tensile in Si near the surface, which can induce circumferential cracking of the Si. Under heating, the circumferential stress is tensile in Si, which can induce radial cracks to form in Si. In contrast, the shear stress σ_{rz} along the TSV/Si interface contributes to the driving force for interfacial delamination under both heating and cooling. In the present study we focus on interfacial delamination as the critical failure mode under both heating and cooling conditions.

To verify the semi-analytic solution, finite element analysis (FEA) is performed using the commercial package, ABAQUS (v6.8). Since the thickness of the Si wafer is one of the key design parameters for the TSV structure, the effect of wafer thickness on thermal stress distribution is examined by FEA models with two different thicknesses. The model structure is shown in Fig. 1a, with the TSV diameter $D_f = 30$ µm and the wafer thickness H=300 µm and 60 µm. A negative thermal loading (cooling), $\Delta T = -250$ ºC, is assumed. The material properties are: $E_f = E_m = 110$ GPa, $\nu_f = \nu_m = 0.35$, and $\alpha_f = 17$ ppm/ºC and $\alpha_m = 2.3$ ppm/ ºC. The model is an approximation to a Cu TSV in Si, neglecting the elastic mismatch between Cu and Si. In practice a thin barrier layer is

typically placed between the Cu via and Si, which has minimal effect on the stress distribution and is thus ignored here.

In Figure 3, the results from the FEA are compared with those obtained by the semi-analytical solution. First, the axial stress (σ_z) along the center line of the TSV (r = 0) shows a transition from zero stress at the surface (z = 0) to a tensile stress away from the surface (Fig. 3a). For the thick wafer ($H/D_f = 10$), the FEA result shows excellent agreement with the analytical solution, both approaching the 2D solution (the dashed line) away from the surface. Similarly, the radial stress (σ_r) at the interface for the thick wafer approaches a finite value at z = 0 and the 2D solution far away from the surface (Fig. 3b). In contrast, for the thin wafer, the stresses are not built up high enough to reach the 2D solution; more so for the axial stress.



(a) σ_z at the via center ($r = 0$) (b) σ_r at the TSV/Si interface ($r = D_f / 2$)

Fig. 3. Effect of wafer thickness on stress distributions ($D_f = 30$ µm, $\Delta T = -250$ ºC).

It is worth noting the 3D nature of the near-surface stresses, which has to be taken into account to determine the keep-out zone around the TSV. This is discussed in the following section. In addition, the near surface stresses can induce channeling cracks at the Si surface near the TSV in either the radial or the circumferential direction, depending on the magnitudes and signs of the stresses.

III. TSV-INDUCED PIEZORESISTIVITY EFFECT ON MOSFETS

A. *Piezoresistivity of silicon*

Piezoresistivity of Si refers to the effect of stresses on the mobility of the charge carriers of Si. The incorporation of TSV can introduce undesired stresses in the Si matrix to degrade the performance of the adjacent MOSFETs. As illustrated in a previous study, a Cu TSV of 30 µm diameter can induce a thermal stress greater than 100 MPa at a distance 10 µm away from the TSV edge [14]. Stresses of such magnitude can affect the carrier mobility and will have to be taken into account in the design of the keep-out zone (KOZ). To design the KOZ, the piezoresistivity effect in Si induced by stresses around the TSV on the carrier mobility has to be considered. This effect has been reviewed recently [15]. In a Si substrate, the general relations among the electric field E, current density J, and the stress components can be expressed as:

$$\begin{aligned}
\frac{\Delta E_1}{\rho} &= [\pi_{11}\sigma_1 + \pi_{12}(\sigma_2+\sigma_3)]J_1 + (\pi_{44}\sigma_6)J_2 + (\pi_{44}\sigma_5)J_3, \\
\frac{\Delta E_2}{\rho} &= [\pi_{11}\sigma_2 + \pi_{12}(\sigma_1+\sigma_3)]J_2 + (\pi_{44}\sigma_6)J_1 + (\pi_{44}\sigma_4)J_3, \\
\frac{\Delta E_3}{\rho} &= [\pi_{11}\sigma_3 + \pi_{12}(\sigma_1+\sigma_2)]J_3 + (\pi_{44}\sigma_5)J_1 + (\pi_{44}\sigma_4)J_2,
\end{aligned} \tag{1}$$

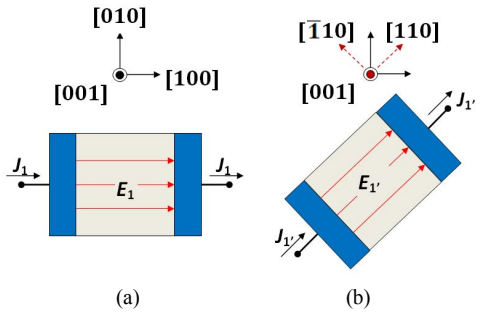
where ρ is the resistivity of the unstrained Si. π_{11}, π_{12}, and π_{44} are the piezoresistivity coefficients of Si. The subscripts of E and J (1, 2, and 3) designate the components along the three (100) crystal axes, while the six subscripts of σ designate the components of a stress matrix. In the following, we consider first the case where a MOSFET is located on a (001) Si wafer with its channel direction aligned with the [100] direction (Fig. 4a). Assume that the electrical current only flows along the channel direction, i.e. $J_2 = J_3 = 0$, and only the electric field across the channel (ΔE_1) is measured. The average resistivity (or mobility) change along the channel direction can be obtained from Eq. (1):

$$\frac{\Delta\rho_1}{\rho} = \frac{\Delta\mu_1}{\mu} = \pi_{11}\sigma_1 + \pi_{12}(\sigma_2+\sigma_3), \tag{2}$$

The channel direction of a MOSFET is often aligned along the [110] direction on a (100) wafer (Fig. 4b). In this case, the resistivity or the mobility change in Eq. (2) can be deduced by rotating the coordinate system as [15, 16]:

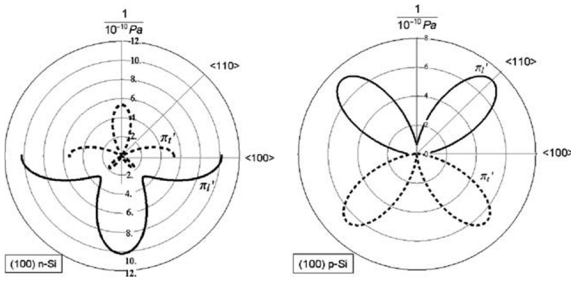
$$\begin{aligned}
\frac{\Delta\rho_{1'}}{\rho} &= \frac{\Delta\mu_{1'}}{\mu} = \pi'_l\sigma_{1'} + \pi'_t(\sigma_{2'}+\sigma_{3'}), \\
\pi'_l &= \frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}, \\
\pi'_t &= \frac{\pi_{11}+\pi_{12}-\pi_{44}}{2},
\end{aligned} \tag{3}$$

where σ' are the stress components in the new coordinate system, which is illustrated by red dash lines in Fig. 4b. π'_l and π'_t are the longitudinal and transverse piezoresistive coefficients of the new channel direction, respectively. Figure 5 shows the graphic representations of the variations of the longitudinal and transverse piezoresistive coefficients with the channel directions on (001) surface in p- and n-Si [15, 17].



(a) (b)

Fig. 4. Channel direction of MOSFETs on (001) Si wafer.



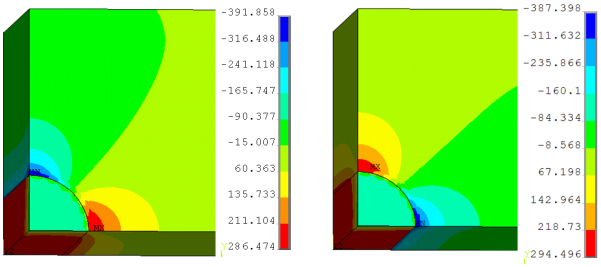
(a) (b)

Fig. 5. Longitudinal and transverse piezoresistive coefficients on (001) Si wafer [15, 17].

B. *Analysis of mobility change and keep-out zone*

Because the MOSFETs are usually fabricated very near the wafer surface, the out-of-plane stress component σ_3, is about two orders smaller than the in-plane component σ_2, and thus is negligible. Additionally, it is clear from Eq. (1) and Eq. (2) that the shear stress components do not contribute to the mobility change. Therefore, the configuration of the KOZ is mainly controlled by the in-plane normal stresses parallel and perpendicular to the channel direction of MOSFETs. To deduce the piezoresistivity effect for Si devices, it is convenient to express the stress distribution in Cartesian coordinates. Accordingly, the distribution of normal stresses on the wafer surface is two-fold rotational symmetric and the distribution of the mobility change (or the KOZ) should have a two-fold rotational symmetry as well.

To calculate the mobility change induced by an isolated TSV, thermal stress analysis is performed using FEA simulation. The model consists of a quarter of a TSV embedded in a Si matrix with a TSV diameter D_f of 20 µm and wafer thickness of 100 µm. The TSV material is taken to be Cu and a negative thermal load, ΔT = -180°C, is applied to calculate the thermal stresses. The distributions of the normal stresses σ_{xx} and σ_{yy} are shown in Fig. 6. Since the devices are fabricated very near the Si surface, the normal stresses (σ_{xx}, σ_{yy}, and σ_{zz}) are simply taken to be on the wafer surface (z = 0) from the simulation results. In the calculation, the channel direction of MOSFETs is assumed to be parallel to the [110] direction, and the piezoresistivity coefficients of bulk n-Si and p-Si (Table 1) are used.



(a) σ_{xx} (b) σ_{yy}

Fig. 6. Distribution of thermal stress component σ_{xx} and σ_{yy} in a quarter Cu TSV model.

Table 1. Piezoresistivity coefficients for bulk Si (10^{-4} MPa^{-1}) [15]

	π_{11}	π_{12}	π_{44}	$\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2}$	$\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2}$
Direction	π//[100]	$\pi\perp$[100]		π//[110]	$\pi\perp$[110]
n-Si	-10.22	5.37	-1.36	-3.16	-1.76
p-Si	0.66	-0.11	13.81	7.18	-6.63

The results obtained for the mobility changes along the [110] channel direction are shown in Figure 7 revealing a significant difference of the stress effect on the carrier mobility for the n- and p-MOS devices. With the same TSV geometry and thermal load (-180°C), the maximum mobility change can reach 35% for the p-MOSFET while only 7% for the n-MOSFET. The result can be attributed to the combination of the sign and magnitude of the stresses and the piezoresistivity coefficients for these two types of devices. First, TSV-induced in-plane normal stresses (σ_{xx} and σ_{yy}) are of similar magnitude but the piezoresistivity coefficients parallel and perpendicular to [110] crystal direction are opposite in sign for p-Si (7.18 v.s. -6.63×10^{-4} MPa^{-1}), but of the same sign for n-Si (-3.16 v.s. -1.76×10^{-4} MPa^{-1}). This results in an addition of the contributions from σ_{xx} and σ_{yy} for the p-MOSFET, but a subtraction for the n-MOSFET.

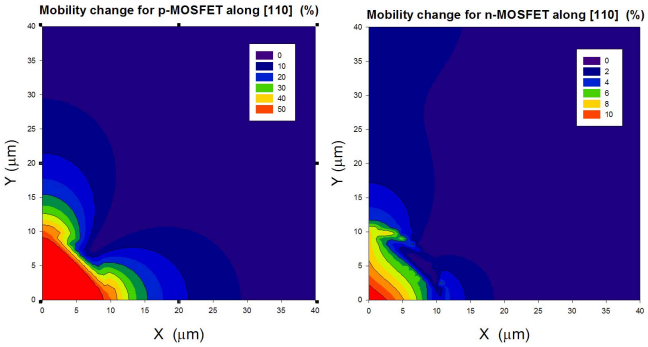


Fig. 7. Distribution of mobility change for p- and n-MOSFETs along [110].

Along the [100] direction, the effect is quite different. Here the piezoresistivity coefficients for n-Si along the parallel and perpendicular directions are opposite in sign (-10.22 v.s. 5.37×10^{-4} MPa^{-1}) and also about an order of magnitude larger than that for p-Si (0.66 v.s. -0.11×10^{-4} MPa^{-1}). Consequently, n-MOSFETs are more sensitive to the TSV-induced thermal stresses than p-MOSFETs along the [100] direction.

The scaling effect on KOZ is investigated as a function of TSV diameter following a similar procedure. For this purpose, FEA models of Cu TSVs are built with a fixed wafer thickness (100 µm) and varying diameter (D_f = 10 ~ 30 µm). A negative thermal load, ΔT = -180°C, is applied. After calculating the mobility change on the wafer surface for both p-Si and n-Si, an arbitrary criterion for KOZ with 10% change in mobility is

applied to calculate the area of KOZ surrounding the TSV. The results are plotted in Fig. 7 for the p-MOSFET devices.

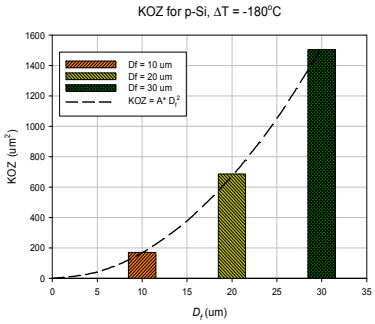


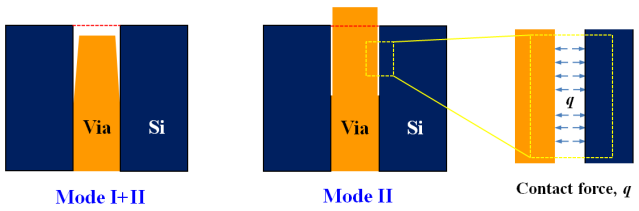
Fig. 8. Effect of TSV diameter on Keep-out Zone.

The results in Fig. 8 indicate a significant effect due to the scaling of the TSV diameter on the area of KOZ for p-MOSFET, increasing approximately with the square of D_f. Overall, the effect yields an area ratio between KOZ and TSV of about 2. It is interesting to note that the TSV-induced stresses cannot generate a mobility change greater than 10% in n-MOSFET under the given thermal load (-180°C), therefore, there is no KOZ for n-MOSFET in this study.

IV. INTERFACIAL DELAMINATION OF TSV

A. *Fully filled TSV*

The stress analysis in the previous section suggests a potential failure mechanism of the TSV structure due to interfacial delamination. Figure 9 depicts two modes of interfacial delamination for a fully-filled TSV structure. With a negative thermal load ($\Delta T < 0$), the radial stress along the via/Si interface is tensile (assuming $\alpha_f > \alpha_m$). Consequently, the interfacial delamination crack can grow in a mixed mode (peeling and shearing). With a positive thermal load ($\Delta T > 0$), however, the radial stress is compressive which does not contribute to the driving force for delamination. This results in an interfacial crack with a pure shearing mode (mode II). In this case, the two crack faces are in intimate contact and may be subject to friction. For simplicity, we assume a frictionless contact in the present study and develop analytical solutions for the steady-state energy release rates of the interfacial crack, under both cooling and heating conditions. The analytical solutions are then compared to finite element analysis, which is extended to study the effects of crack length and wafer thickness on the fracture driving force.



(a) Cooling ($\Delta T < 0$) (b) Heating ($\Delta T > 0$)

Fig. 9. Schematics of interfacial delamination of TSV under cooling and heating conditions.

For a TSV with a relatively high aspect ratio (H / D_f), the energy release rate for interfacial delamination reaches a steady state when the crack length is several times greater than the via diameter. Since the energy release rate is usually lower for shorter cracks, the steady-state value sets an upper bound for the fracture driving force, which may be used as the critical condition for conservative design of reliable TSV structures.

Consider an infinitely long fiber (TSV) in an infinite matrix (Si wafer), with a pre-existing semi-infinite, circumferential crack along the interface and subjected to a thermal load ΔT . The steady-state energy release rate (ERR) for the interfacial crack growth (per unit area) is obtained by comparing the elastic strain energy far ahead of the crack front and that far behind the crack front. While the stress field near the crack front is complicated with singularity and 3D distribution, it merely translates in the steady state as the crack front advances. Far ahead of the crack front, the stress field can be obtained analytically by solving the 2D plane-strain problem (Problem A in Fig. 1). Far behind the crack front, since the TSV is debonded from Si, the stress is relaxed in both the via and Si. For the case of cooling ($\Delta T < 0$), the stress is zero in both TSV and Si. For heating ($\Delta T > 0$), however, the contact between the crack faces induces a stress field similar to Problem A, but the axial stress (σ_z) in the via is zero from the assumption of frictionless contact. If the elastic mismatch is neglected (i.e., $\alpha = 0$ and $\nu_f = \nu_m = \nu$), the steady state energy release rate under cooling can be expressed in a simple form:

$$G_{cooling}^{SS} = \frac{E\varepsilon_T^2 D_f}{4(1-\nu)}. \tag{4}$$

Under heating with $\Delta T > 0$, due to the contact of the crack faces (Fig. 9b), the stress state in the TSV far behind the crack front is equibiaxial. As a result, the steady state ERR under heating can be obtained by neglecting the elastic mismatch, namely

$$G_{heating}^{SS} = \frac{1+\nu}{8(1-\nu)} E\varepsilon_T^2 D_f. \tag{5}$$

To verify the steady state ERR solution, a FEA model of the TSV structure is constructed, and the energy release rates are calculated by the J-integral method. As expected, the energy release rate increases with the crack length and approaches the steady-state solution when the crack length is longer than about 2-3 times the via diameter (Fig. 10).

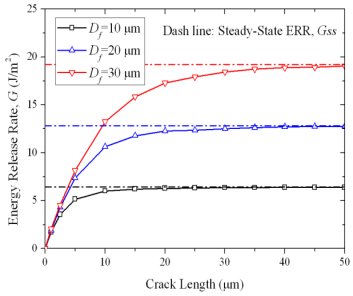


Fig. 10. Effect of crack length on the energy release rate for interfacial delamination of TSVs ($H = 300$ μm and $\Delta T = -250$ °C).

Several interesting results can be deduced based on the analytical solutions for the steady-state energy release rates. First, the steady-state ERR for interfacial delamination is linearly proportional to the TSV diameter, which may set an upper bound for the via diameter in order to avoid delamination. Second, the ERR is proportional to the square of the thermal mismatch strain, $\varepsilon_T = (\alpha_f - \alpha_m)\Delta T$. Thus the delamination driving force can be reduced by either using TSV materials with smaller thermal expansion mismatch ($\alpha_f - \alpha_m$) and/or by reducing the thermal loads (ΔT). Third, the energy release rate for interfacial delamination increases with the elastic modulus of the TSV material, however, the effect is less important than the effect of the thermal expansion mismatch. Finally, a comparison between Eq. (4) and (5) indicates that, with the same thermal load ΔT , the driving force for interfacial delamination under cooling is about twice that under heating, a result that can be attributed to the presence of a tensile radial stress (σ_r) across the interface (opening mode) for the case of cooling.

B. The "pop-up" of TSV with a nail head

In practice, a hard mask for etching Cu TSVs in silicon substrate often results in a ledge or overhang called 'nail head' over the TSV. The nail head can also be used on purpose to facilitate connection to the upper die. The presence of the nail head changes the boundary conditions at the crossing point of Cu/Si/Nail head and interfacial end of Si/Nail head, which in turn affects the stress distribution around both the TSV and Si. In particular, under negative thermal loading, the concentration of the shear stress along the TSV/Si will decrease but the shear concentration along nail head/Si will develop due to the nail head. In addition, the opening stress at the nail head perimeter/Si interface possesses singularity. As a result, the stress concentration contributes to interfacial failures. To analyze this problem, we calculate the steady-state energy release rate for the TSV structure with nail head under cooling. Here the dimensions of thickness and diameter for nail head simply are assumed to be sufficiently large. This yields zero radial and circumferential stresses far behind the crack tip while the out-of plane stress exists due to the constraint by the nail head. The ERR obtained under these assumptions is close to that obtained by FEA.

To evaluate the effect of nail head on energy release rate, we compare ERR between fully filled TSV ($D_f = 30\,\mu\text{m}$) and TSV with a nail head ($H_n = 0.5D_f$) under cooling ($\Delta T = -250$ ºC). The cooling condition contributes to failure of only the vertical surface, so that we vary the vertical crack length (c_1) with zero horizontal crack ($c_2 = 0$). As crack propagates along the vertical interface, the ERR approaches the steady-state solution. The steady-state ERR for TSV with a nail head drops about 30% due to the constraint effect of the nail head (Fig.11). Thus the nail head can be helpful to improve the TSV reliability.

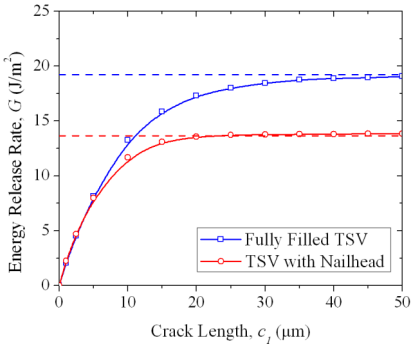
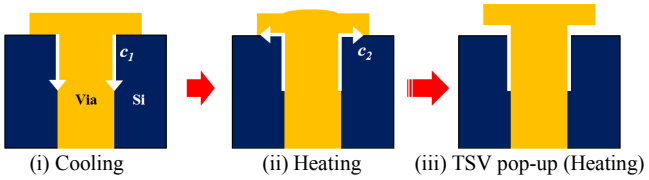


Fig. 11. Comparison of steady-state ERRs between a fully filled TSV and a TSV with nail head ($D_f = 30$ μm, $H_n = 0.5D_f$, $c_2 = 0$, and $\Delta T = -250$ ºC).

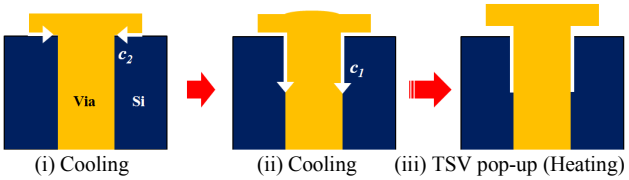
TSV pop-up describes a phenomenon of TSV lifting off from the surrounding matrix as schematically depicted in Fig. 12. The interface between the nail head and Si is subjected to shearing near the perimeter of the nail head, which may cause delamination at that location. Therefore, analysis of the interfacial reliability of TSVs with nail head should consider both interfaces, vertical and horizontal. If both interfaces fail during thermal cycling, TSV can be extruded from the Si substrate. Here, we describe two thermal processes that can cause TSV pop-up.

First, by comparing the energy release rates under cooling and heating, we observe that the interface is more prone to delamination under cooling than under heating. Under cooling, a vertical crack (c_1) initiated at the TSV/Si interface can reach a stationary crack through repeated thermal cycles. Then, during the ensuing heating cycling, a horizontal crack (c_2) can be generated at the Si/nail head interface from inside toward the outside of the nail head (Fig. 12a). Finally, the delamination at both interfaces can bring about TSV pop-up. Alternately, after vertical crack failure, horizontal crack could start from outside toward the inside of the nail head. However, the ERR for this failure mode is relatively small, e.g. less than $1\ \text{J/m}^2$. Thus, this process can be ruled out from consideration.

Another possibility for TSV pop-up arises from the concentration of opening and shearing stress under cooling (Fig. 12b). The driving force can cause initial crack growth at the free end of the nail head/Si interface, followed by an interfacial crack expanding inward due to the positive opening stress. Then, after fully debonded at the nail head/Si interface, a vertical crack propagates along the TSV/Si interface under an ERR corresponding to that of the fully filled TSV.



(a) A first scenario for TSV pop-up



(b) A second scenario for TSV pop-up

Fig. 12. Two probable thermal processes for TSV pop-up

V. CONCLUSIONS

In this study, the thermo-mechanical reliability of a TSV structure in 3D interconnect is investigated by a semi-analytical approach and FEA calculations. The stress characteristics are inherently 3D in nature with the near-surface stress distributions distinctly different from the analytical solution based on a simple 2D model. The energy release rate for interfacial delamination of TSV is evaluated under both cooling and heating conditions, using an analytical solution for a steady-state crack growth and numerical solutions obtained by FEA for non-steady state crack growth. Based on these results, the interfacial reliability of a fully filled TSV together with the potential mechanisms for TSV pop-up are discussed. In this paper, we also examine the piezoresistivity effect induced by the near surface stresses on the charge mobility for p- and n- channel MOSFET devices and investigate the impact of scaling on the keep-out zone for MOSFET devices. Together, the results of this study provide a basis to explore the potential of using materials and structure optimization for improving TSV reliability for 3D interconnects.

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