Effect of Thermal Stresses on Carrier Mobility and Keep-Out Zone Around Through-Silicon Vias for 3-D Integration

Suk-Kyu Ryu, Kuan-Hsun Lu, Tengfei Jiang, Jang-Hi Im, *Senior Member, IEEE*, Rui Huang, and Paul S. Ho, *Fellow, IEEE*

***Abstract*—Three-dimensional (3-D) integration with through-silicon vias (TSVs) has emerged as an effective solution to overcome the wiring limit imposed on device density and performance. However, thermal stresses induced in the TSV structures can affect the device performance by degrading carrier mobility and raise serious reliability concerns. In this paper, the effect of thermal stresses in TSV structures on carrier mobility and keep-out zone (KOZ) was investigated by focusing on the characteristics of the stresses near the surface where the electronic devices are located. The near-surface stresses were characterized by finite element analysis, and the stress effect on carrier mobility was evaluated by considering the piezoresistivity effect near the Si surface. In this paper, the elastic anisotropy of Si was taken into account to evaluate the effect on carrier mobility for both n- and p-channel MOSFET devices aligned along the [100] and [110] directions. The results showed a significant stress effect on carrier mobility, particularly for n-type Si with [100] device alignment and p-type Si with [110] device alignment. Based on these results, the dimension of the KOZ was estimated based on a criterion of 5% change in the carrier mobility. Finally, the effects due to stress interactions in a TSV array and plasticity in Cu vias on the KOZ were investigated. The effect of stress interaction was found to depend on the ratio of the pitch to diameter of the TSV array. When this ratio is less than 5, the stress interaction can increase the size of the KOZ. In contrast, the via material plasticity was found to be useful in reducing the stress level and hence the size of the KOZ.**

***Index Terms*—Finite element analysis (FEA), keep-out zone (KOZ), thermomechanical reliability, through-silicon via (TSV), three-dimensional interconnects.**

I. Introduction

THREE-DIMENSIONAL (3-D) integration presents an effective solution in meeting the challenges in the development of on-chip interconnections beyond the 32-nm technology node. A critical structural element in the 3-D interconnects is the through-silicon via (TSV) that directly connects the stacked die structures. By using TSVs in 3-D integration, the system performance can be significantly improved and the manufacturing costs reduced [1]–[3]. However, due to the mismatch in the coefficient of thermal expansion (CTE) between the via materials and Si, thermal stresses are ubiquitously induced during processing and thermal cycling of TSV structures [4], [5]. The thermal stresses can drive interfacial delamination between the TSV and the Si matrix, resulting in the TSV "pop-up" to damage the on-chip wiring structures [6]–[9]. The stress induced by TSV can also affect the carrier mobility due to the piezoresistivity effect to degrade the performance of the MOSFET devices [10]–[12]. For TSV structures, a tensile stress of 100 MPa was found to enhance the electron mobility of up to 7% for n-type Si. For p-type Si, however, the stress can either enhance or degrade the hole mobility, depending on the transistor channel direction [12]. It has also been reported that the TSV-induced stresses can cause up to 30% shift in the saturation drain current (I_{DSAT}) of the transistor to degrade the device performance [13]. Further studies are required to understand the impact of material properties and TSV design on the overall stress behavior and the keep-out zone (KOZ) around the TSVs for MOSFET devices.

In this paper, the effect of thermal stresses in TSV structures on carrier mobility was investigated, including a study on the piezoresistivity effect and the impact of material properties and TSV dimensions on the design of the KOZ. In actual IC structures, the intrinsic stresses from the fabrication processes could affect the final stress state in the TSV structures. Depending on the fabrication conditions, the intrinsic stress could vary significantly either to reduce the KOZ or increase it. For simplicity, the effect of stresses due to additional processing was not considered in the present study. First we analyzed the stress characteristics in the near surface region surrounding the TSV since most of the active devices are fabricated within a few micrometers of the Si surface. To account for the 3-D nature of the near-surface stresses, a 3-D finite element analysis (FEA) is employed and the elastic anisotropy of silicon is taken into account. This is followed by examining the piezoresistivity effect on the carrier mobility along different channel directions for n- and p-type MOSFET devices. Based on these results, we estimate the size of the KOZ. Finally, the possibility of design optimization for reduced KOZ is explored by investigating the effects of material properties, TSV layout and Cu plasticity.

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S.-K. Ryu and R. Huang are with the Department of Aerospace Engineering and Engineering Mechanics, The University of Texas at Austin, Austin, TX 78712 USA (e-mail: ruihuang@ mail.utexas.edu).

K.-H. Lu, T. Jiang, J.-H. Im, and P. S. Ho are with the Microelectronics Research Center, The University of Texas at Austin, Austin, TX 78712 USA (e-mail: paulho@mail.utexas.edu).

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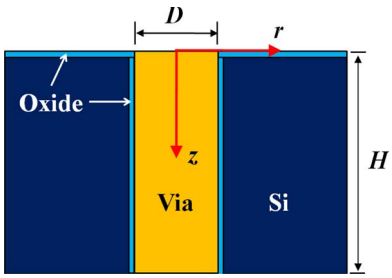

Fig. 1. Illustration of a TSV structure (D: via diameter, H: TSV height).

II. Stress Analysis for TSV Structures

A. Characteristics of Near-Surface Stresses

Most electronic devices are fabricated within a few micrometers from the wafer surface. Since the stress distribution near the surface is distinctly 3-D in nature [14], the 2-D plane-strain solution to the classical Lame problem cannot provide an accurate stress distribution to evaluate the stress effect on the device characteristics. For this reason, a semi-analytic solution for the 3-D stress distribution was derived using a superposition method, as described in our previous study [14]. However, to determine the size of the KOZ, more accurate analysis based on a 3-D FEA was used in this study to quantify the thermal stress distribution near the TSV structure. The stress analysis was first performed for an isolated TSV of 10 μm diameter and 200 μm height as illustrated in Fig. 1, and only considered the effect of thermal stresses, while neglecting any intrinsic stresses in the TSV structures. The oxide barrier layer was also neglected for simplicity. The FEA was performed using a quarter model of the via to improve the computational efficiency. For boundary conditions, the top surface was set to be traction free while the out-of-plane (z-direction) displacement at the bottom surface was set to be zero. Linear 3-D solid elements (C3D8R) of the size of 0.5 μm $\times$ 1 μm were used with a negative thermal loading (cooling) of -250 °C. The material properties used are: Young's modulus $E_{\mathrm{Cu}} = 110$ GPa, Poisson's ratio $\nu_{\mathrm{Cu}} = 0.35$, and the coefficient of thermal expansion, $\alpha_{\mathrm{Cu}} = 17$ ppm/°C for Cu, and $E_{\mathrm{Si}} = 130$ GPa, $\nu_{\mathrm{Si}} = 0.28$, and $\alpha_{\mathrm{Si}} = 2.3$ ppm/°C for Si.

The stress distributions and the deformation in the TSV structure under the applied thermal load ($\Delta T = -250$ °C) are shown in Fig. 2. The negative thermal load induces a sink-in of the Cu via near the wafer surface although its effect on the Si surface deformation is rather small. In Fig. 2(a), the normal stress σ_z is zero on the surface ($z = 0$), as is required by the traction-free boundary condition. Near the surface, σ_z is nonuniform in both the Cu via and Si and becomes negligible in Si away from the via. In contrast, the shear stress (σ_{zr}) in Fig. 2(b) is concentrated at the junction between the wafer surface ($z = 0$) and via/Si interface ($r = D/2$) where the stress may be sufficient to delaminate the via interface [14]. Close to the free surface, the radial stress (σ_r) and the circumferential stress (σ_θ) [Fig. 2(c) and (d)] are quite different from those obtained by the 2-D solution. In the following analysis of the piezoresistivity effect, we found that all these stress components are large enough to induce mobility variations near the surface. Thus the 3-D characteristics of the stress distributions have to be taken into account to analyze the stress effect on the KOZ.

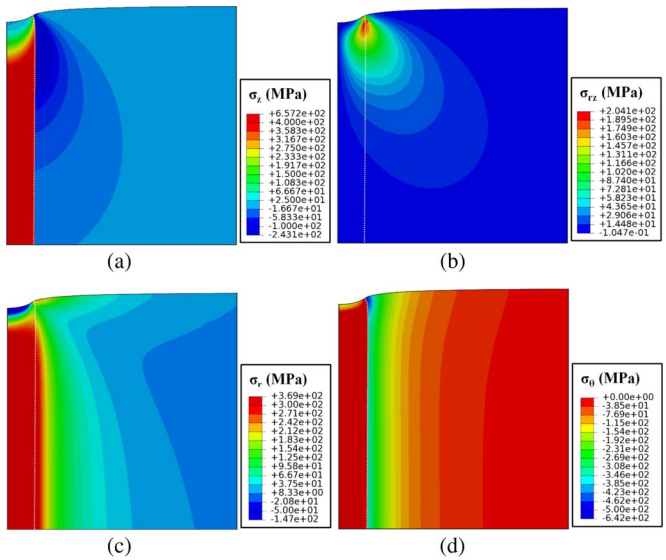

Fig. 2. Deformation and stress distributions in a TSV structure ($D = 10$ μm, and $\Delta T = -250$ °C). (a) Out-of-plane stress, σ_z. (b) Shear stress, $\sigma_{r\theta}$. (c) Radial stress, σ_r. (d) Circumferential stress, σ_θ.

B. Effect of Si Anisotropy on Stresses

Since the material properties of Si are anisotropic, the effect of elastic anisotropy of silicon on thermal stresses is included in this study. Specifically, the anisotropic effect is evaluated for the (001) Si wafer, the common type of device wafers, which has the following stiffness matrix in the natural coordinates of the crystal ([100], [010], and [001]) [15]

$$\mathrm{C}_{(001)} = \begin{bmatrix} 166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\ 64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\ 64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.8 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.8 & 0 \\ 0 & 0 & 0 & 0 & 0 & 79.8 \end{bmatrix} \text{GPa}. \quad (1)$$

In the FEA analysis, the stiffness matrix in Eq. (1) is applied to calculate the stress distribution in Si, and the result is compared to that of the isotropic model ($E_{\mathrm{Si}} = 130$ GPa and $\nu_{\mathrm{Si}} = 0.28$). For FEA, the same geometry and boundary conditions are used as described in the previous section for an isolated TSV with $\Delta T = -250$ °C. Since the out-of-plane stress (σ_r) is negligible near the surface, the analysis focuses on the in-plane stresses near the surface.

Fig. 3 shows the stress contours in the cylindrical coordinates, comparing the results from the isotropic and anisotropic models. Overall, the stress distributions in the isotropic Si are axisymmetric with concentric circular contours. This is in contrast to the stress contours in the anisotropic (001) Si which exhibits a fourfold symmetry due to the cubic crystal structure of Si. Interestingly, the in-plane shear stress ($\sigma_{r\theta}$) is zero everywhere in the isotropic model, while the shear stress in the anisotropic (001) Si is not zero near the via/Si interface [Fig. 3(c)]. These results indicate that the near-surface stresses are strongly orientation dependent for the anisotropic Si. Consequently, the stress effect on the carrier mobility also strongly depends on the device orientation in the wafer.

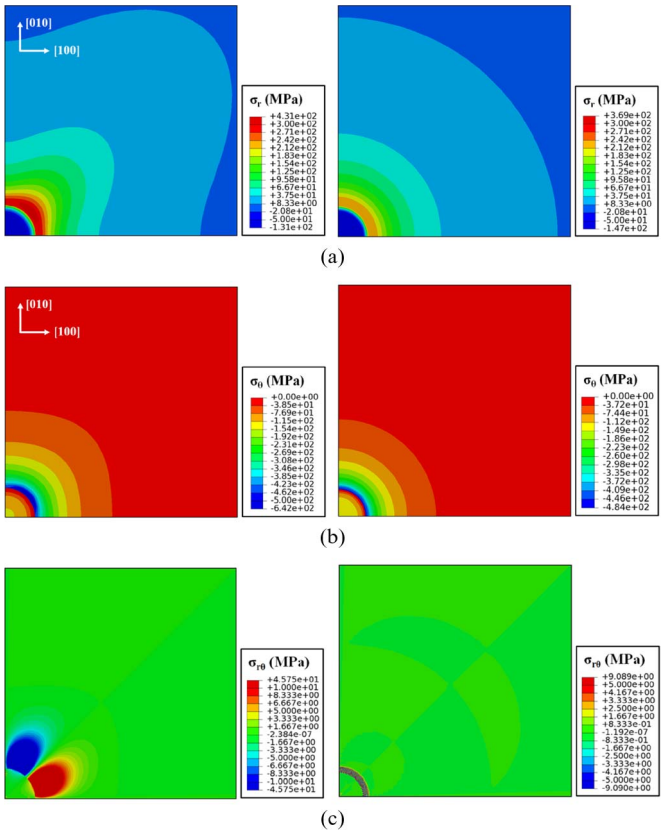

Fig. 3. Deformation and stress distributions in a TSV structure ($D = 10\ \mu$m, and $\Delta T = -250\ ^\circ$C). (a) Radial stress, σ_r. (b) Circumferential stress, σ_θ. (c) Shear stress, $\sigma_{r\theta}$.

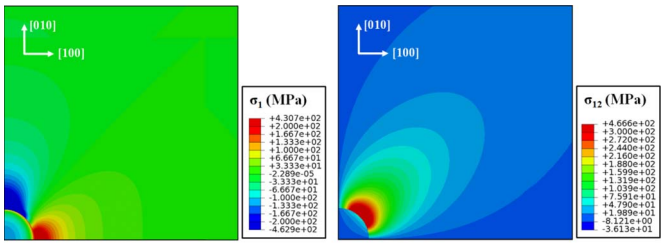

Fig. 4. Near-surface stress distributions around a TSV in (001) Si wafer (D = 10 μm and $\Delta T = -250\ ^\circ$C). (a) Normal stress, σ_1. (b) Shear stress, σ_{12}.

To calculate the mobility change for devices with carrier channels aligned along specific directions, it is more convenient to express the stress components in the Cartesian coordinates. In Fig. 4, the stress components (σ_1, σ_{12}) on the surface $(z = 0)$ are shown for the anisotropic (001) Si. By symmetry, the other normal stress σ_2 is the same as σ_1 with a 90° rotation. In the following section, the effects of elastic anisotropy on piezoresistivity and the KOZ are analyzed.

III. Effect of Thermal Stresses on Carrier Mobility

A. Piezoresistivity Effect of Si

Piezoresistivity of Si refers to the effect of stresses on the mobility of the charge carriers of Si. Specific stress characteristics are commonly used to promote the performance of Si MOSFETs, and such "strained-Si" technology has been implemented in manufacturing of high-performance microprocessors since the 90-nm technology node in 2002 [16]–[21]. For this purpose, Ge is implanted into the source/drain region for the pMOS devices and a silicon nitride capping layer is applied for the nMOSFETs [22]. These processes induce a uniaxial residual stress in the middle of the respective device channel to enhance the carrier mobility, by 35% for the nMOSFETs and 90% for the pMOSFETs for the 65-nm node [23].

TABLE I
Piezoresistance Coefficients for n- and p-Type Si (in Units of 10^{-11} Pa^{-1})

	π_{11}	π_{12}	π_{44}
n-type Si	-102.2	53.7	-13.6
p-type Si	6.6	-1.1	138.1

The change of the electric field, $\Delta\tilde{E}$, corresponding to a resistivity change can be expressed as following:

$$\Delta\tilde{E}_i = \Delta\rho_{ij} J_j. \tag{2}$$

Under the piezoresistivity effect, the relative change of resistivity can be related to the applied stress (σ_{kj}) by the piezoresistance coefficient (π_{ijkl}) [23]

$$\Delta\rho_{ij}/\rho = \pi_{ijkl}\sigma_{kl}. \tag{3}$$

And the change of the electric filed can be expressed as

$$\frac{\Delta\tilde{E}_i}{\rho} = (\pi_{ijkl}\sigma_{kl})J_j. \tag{4}$$

Applying the symmetries of the piezoresistance coefficients, e.g., $\pi_{ijkl} = \pi_{jikl}$, $\pi_{ijkl} = \pi_{ijlk}$ and $\pi_{ijkl} = \pi_{klij}$, the 4th order tensor for silicon can be simplified to a matrix form

$$\pi = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ & & \pi_{11} & 0 & 0 & 0 \\ & & & \pi_{44} & 0 & 0 \\ & sym & & & \pi_{44} & 0 \\ & & & & & \pi_{44} \end{bmatrix}. \tag{5}$$

Table I lists the values of piezoresistance coefficients for n-type and p-type Si, where π_{11}, π_{12}, and π_{44} are measured with current flows in the [100] direction in the natural coordinates of the crystal [23].

When the device channels are aligned along the [100] direction, and the electric field $(\tilde{E})$ and current density (J) are applied in the same direction [Fig. 5(a)], Eq. (4) becomes

$$\frac{\Delta\tilde{E}_1}{\rho} = \left[\pi_{11}\sigma_{11} + \pi_{12}\left(\sigma_{22} + \sigma_{33}\right)\right] J_1. \tag{6}$$

The carrier mobility is inversely proportional to the resistivity, and thus its change due to the piezoresistivity effect can be expressed as

$$\Delta\mu/\mu = -\Delta\rho/\rho. \tag{7}$$

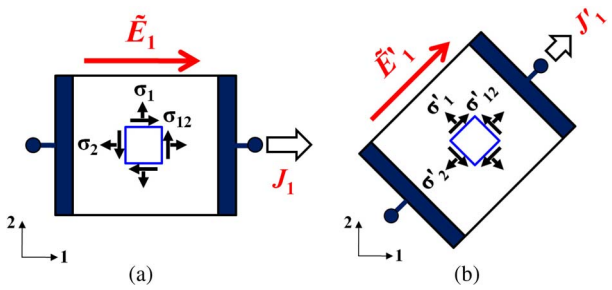

Fig. 5. Illustration of the device channels in different directions, with the in-plane stress components. (a) Electric field ($\tilde{E}$) and current density (J) in the [100] direction. (b) Electric field ($\tilde{E}$) and current density (J) in the [110] direction.

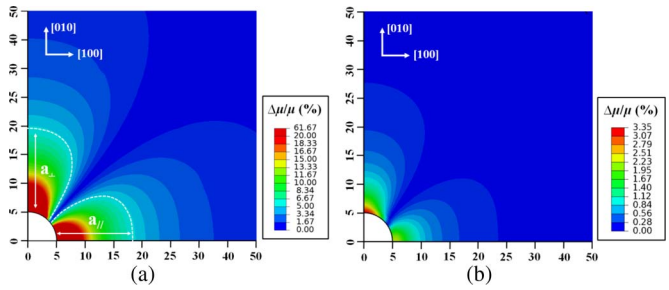

Fig. 6. Distribution of the mobility change for (a) n-type MOSFET and (b) p-type MOSFETs with the electric field and current density in [100] direction. The dashed lines indicate the 5% mobility change (D = 10 μm, H = 200 μm, and $\Delta T = -250$ °C).

Then, from Eq. (6) and (7), the absolute value of the relative mobility change along the [100] channel direction can be obtained as [24]

$$\frac{\Delta\mu_1}{\mu} = |\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})|\,. \tag{8}$$

When the devices are aligned along other directions such as [110] or [1$\bar{1}$0], and with the electric field and current density along the same direction [Fig. 5(b)], the piezoresistance coefficients and stresses have to be transformed to the new direction. For an arbitrary angle, θ, from the [100] direction, the piezoresistance coefficients can be transformed as

$$\pi'_{11} = \pi_{11} + 2(\pi_{44} + \pi_{12} - \pi_{11})\cos^2\theta\sin^2\theta \tag{9}$$

$$\pi'_{12} = \pi_{12} - 2(\pi_{44} + \pi_{12} - \pi_{11})\cos^2\theta\sin^2\theta \tag{10}$$

where the superscript ($'$) indicates the component in the new direction after the transformation.

Similarly, the in-plane stress components become

$$\sigma'_{11} = \sigma_{11}\cos^2\theta + \sigma_{22}\sin^2\theta + 2\sigma_{12}\sin\theta\cos\theta \tag{11}$$

$$\sigma'_{22} = \sigma_{11}\sin^2\theta + \sigma_{22}\cos^2\theta - 2\sigma_{12}\sin\theta\cos\theta. \tag{12}$$

And the mobility change along the arbitrary channel direction can be expressed as [24]

$$\frac{\Delta\mu'_1}{\mu'} = |\pi'_{11}\sigma'_{11} + \pi'_{12}(\sigma'_{22} + \sigma'_{33})| \tag{13}$$

where σ'_{33} is zero on the wafer surface.

Depending on the design of the 3-D structures, the active devices could be located a few micrometers below the free surface, with multilayer interconnect structures built above. In such situations, the stress state becomes triaxial, and the out-of-plane stress component, σ_{33} should not be neglected. Although not discussed in this paper, the mobility change for the triaxial stress situation can be computed using the same approach as outlined in this work.

B. Comparison of the Mobility Change for n- and p-Type MOSFETs

As can be seen from Table I, the piezoresistance coefficients are different for n- and p-type Si, and thus the mobility change induced by the piezoresistivity effect will also be different. In this section, the mobility changes for the two types of Si is investigated. To estimate the size of the KOZ, the absolute value of mobility change [Eq. (8)] is considered and the KOZ is defined by the region with a change of carrier mobility over 5%. This was first evaluated for an isolated TSV structure on (001) Si with a thermal load of $\Delta T = -250$ °C. Here, FEA was used to evaluate the stress components on the wafer surface and the results were used to calculate the mobility changes Eq. (8) based on the piezoresistance coefficients listed in Table I. The out-of-plane stress, σ_3, being zero on the wafer surface, was ignored in the analysis. For the calculation, the devices are assumed to be aligned along [100] and with the electric field and current density applied in the same direction. The contours of mobility changes deduced for n- and p-type Si are shown in Fig. 6, where the mobility changes are orientation dependent, reflecting the anisotropic material properties and piezoresistivity effect of Si. In particular, for n-type Si, the maximum mobility change is about 61%. The boundary of the KOZ corresponding to 5% mobility change is marked by the dashed line in Fig. 6(a). To define the KOZ, two characteristic distances, $a_{//}$ and $a_\perp$, which are slightly different for the distances in the parallel and perpendicular directions of the [100] device, are used to represent the anisotropy of the KOZ. In contrast, for p-type Si, the maximum mobility change does not exceed 5% as shown in Fig. 6(b). Therefore, for p-type (001) Si subjected to the same thermal load, the KOZ by the same definition vanishes for devices with [100] alignment.

C. Effect of Device Alignment on the Mobility Change

W Since the material properties of Si are anisotropic, the mobility change induced by the piezoresistivity effect depends on the device orientation. If the devices are aligned along the [110] direction, which corresponds to $\theta = 45^\circ$ in Eqs. (9)–(12), the stress components and piezoresistance coefficients become

$$\sigma'_1 = \frac{\sigma_1 + \sigma_2}{2} + \sigma_{12}, \quad \sigma'_2 = \frac{\sigma_1 + \sigma_2}{2} - \sigma_{12} \tag{14}$$

$$\pi'_{11} = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}, \quad \pi'_{12} = \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2}. \tag{15}$$

Under the assumption that the directions of electric field and current flow are identical to the device alignment, [110], the

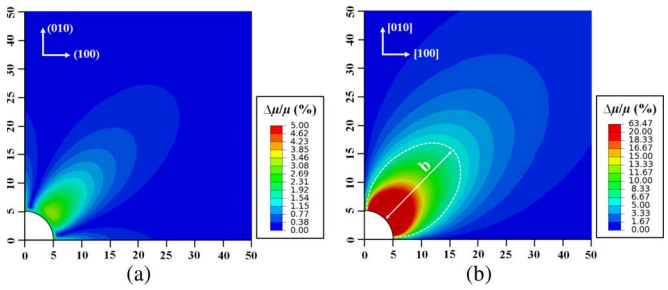

Fig. 7. Distribution of the mobility change for (a) n-type MOSFET and (b) p-type MOSFET with the electric field and current density in [110] direction. The dashed lines indicate the 5% mobility change (D = 10 μm, H = 200 μm, and $\Delta T = -250\,^{\circ}$C).

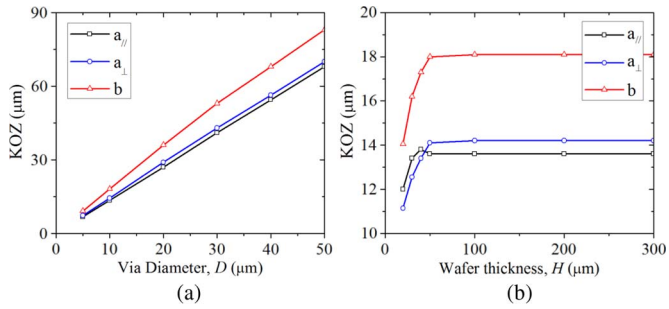

Fig. 8. Effect of via dimensions on KOZ for n-type Si with [100] device alignment and p-type Si with [110] device alignment ($\Delta T = -250\,^{\circ}$C). (a) Effect of via diameter (H = 200 μm). (b) Effect of wafer thickness (D = 10 μm).

mobility change becomes

$$\frac{\Delta\mu'}{\mu'} = \left|\frac{\pi_{11}+\pi_{12}}{2}(\sigma_{11}+\sigma_{22}) + \pi_{44}\sigma_{12}\right|. \qquad (16)$$

By Eq. (16), the mobility changes calculated for the [110] device alignment are plotted in Fig. 7 for n- and p-type Si. Contrary to the [100] device alignment, the mobility change for n-type Si for the [110] device alignment is less than 5% [Fig. 7(a)]. For p-type Si, however, the maximum mobility change can be up to 63% for the [110] device alignment [Fig. 7(b)]. Based on the 5% mobility change criterion, the boundary of the KOZ is plotted, with a characteristic distance, b, for the extent of the KOZ.

Combining with the results for the [100] channel direction, this study suggests that for n-type devices, the [110] alignment is preferred from the point of view of minimizing KOZ due to TSVs. For p-type devices, the [100] channel orientation is preferred instead in order to minimize the stress effect on the carrier mobility.

IV. Effect of Structural Design and Material Properties on KOZ

A. Effect of TSV Dimensions on KOZ

Depending on the integration strategy, the diameter of TSV used in 3-D interconnects can range from 20 micrometers to a few micrometers with its height ranging from 200 μm to 10 μm. Down scaling of via dimensions such as diameter and height can increase the interconnect density and reduce the package size. However, the scaling of the TSV dimensions raises manufacturing problems such as difficulties in metal filling for high-aspect-ratio TSVs, and handling of ultrathin Si wafers. In addition, the thermal stresses near the surface in the TSVs vary with the via dimensions. Here, the scaling effect on KOZ is studied. Since the piezoresistivity effect is more pronounced for n-type Si along the [100] channel direction and p-type Si along the [110] channel direction, respectively, these two cases are considered to estimate the upper limits of the KOZ.

To study the effect of via diameter, an isolated TSV structure was evaluated for (001) Si under a thermal load of $\Delta T = -250\,^{\circ}$C and with the via height fixed at H = 200 μm. The results are expressed in terms of the characteristic distances: $a_{//}$ and $a_{\perp}$ for n-type Si, and b for p-type Si, and plotted in Fig. 8(a). For both n- and p-type Si, the size of the KOZ was found to increase with increasing via diameter. For example, in n-Si with [100] channel direction, the KOZ is about 7 μm for a TSV with 5 μm diameter. However, when the TSV diameter increases to 50 μm, the size of the KOZ reaches 60 μm. For p-type Si with [110] channel direction, the increase is even larger with increasing via diameter. In general, there is a relatively large effect on the KOZ size due to increasing via diameter and for a given via diameter, the KOZ for p-type Si with [110] device alignment is larger than that for n-type Si with [100] direction.

The results for TSVs with a fixed diameter of D = 10 μm but varying via heights are shown in Fig. 8(b). For the same TSV height, the size of KOZ is larger for p-type Si with [110] channel direction. For via heights less than 50 μm, the KOZ increases steadily with the via height. This is because the thermal stress is relaxed through the free surface for a thin TSV wafer, and thus resulting in a smaller KOZ. Interestingly, for both types of Si, the KOZ eventually converges to a stable dimension once the via height exceeds 50 μm. When the wafer is sufficiently thick, the near-surface stresses become independent of the wafer thickness, and thus the size of the KOZ saturates. Comparing Fig. 8(a) and (b), the KOZ appears to be more sensitive to the variation of the via diameter than to the via height.

B. Effect of Stress Interaction on KOZ

The analysis in the previous section was based on an isolated TSV structure. Here, the analysis is extended to study the effect of a TSV array where the pitch between the TSVs can be small enough to generate interaction between neighboring vias. When the TSVs are close to each other, the thermal stresses are enhanced due to via-to-via interactions. For this study, a periodic array of TSV structure is considered, as illustrated in Fig. 9(a). In the FEA model, the via diameter is fixed at D = 10 μm while the pitch between the adjacent vias (p) is varied. With a thermal load of $\Delta T = -250\,^{\circ}$C, the stress components in the Cartesian coordinate are evaluated for locations A and B [Fig. 9(a)] to represent stress interactions along the [100] and [110] directions, respectively. Fig. 9(b) plots stress components (σ_1, σ_2) at A and B as a function of the pitch-to-diameter (p/D) ratio. At point B, the two stress components are identical,

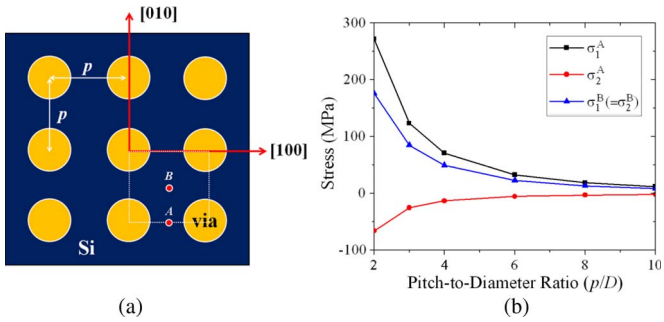

Fig. 9. Effect of the pitch distance on thermal stresses. (a) Illustration of a TSV array (p: pitch size between neighboring vias). (b) Stress components at A and B.

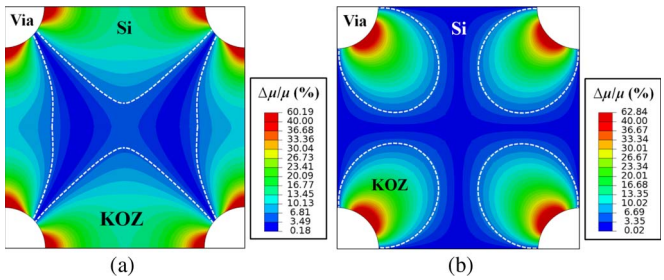

Fig. 10. Effect of stress interaction $(p/D = 3)$ on Keep-Out Zone (KOZ) for (a) n-type MOSFET with [100] alignment and (b) p-type MOSFET [110] alignment, where dashed lines indicate the 5% mobility change.

while the stress components at point A have opposite signs and different magnitudes. As the p/D ratio becomes smaller and the vias are placed closer together, the stress interaction becomes more severe and the stresses in the Si increases. The overall effect of stress interaction becomes negligible when p/D is larger than ~5.

Based on the stress dependence on the p/D ratio, the effect of stress interaction on KOZ can be evaluated. In particular, for $p/D = 3$, the contours of mobility change are plotted for n-type Si with [100] channel direction and p-type Si with [110] channel direction, respectively (Fig. 10). In the contours, the KOZ boundaries for 5% mobility change are highlighted by the dashed lines. For n-type Si, the KOZs from the neighboring vias overlap and merge into larger KOZs [Fig. 10(a)]. For p-type Si, the KOZs do not overlap, but the stress interaction still increases the size of the KOZ, as compared with the isolated TSV structure [Fig. 10(b)]. When the p/D is larger than 5, the KOZs for the both cases have the same size as those deduced for isolated TSV in Figs. 6(a) and 7(b), respectively. Therefore, if the TSV arrays are located closer than $p/D = 5$, the stress interaction needs to be taken into account in the TSV design.

C. Effect of Cu Plasticity on KOZ

In the fabrication of TSV structures, annealing at a high temperature above 200 °C is typically required. Such annealing condition may develop plasticity in the Cu vias, which may impact the reliability of TSV structures. The effect of Cu plasticity on the KOZ is studied for an isolated TSV structure with varying yield strength and thermal loads.

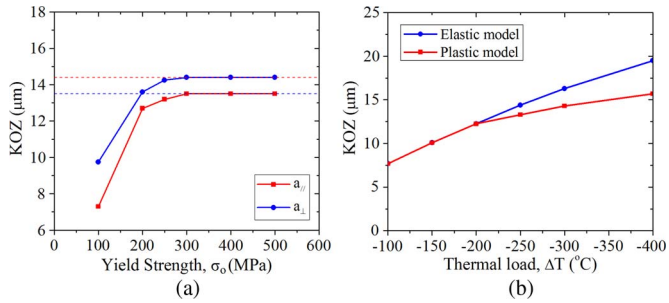

Fig. 11. Effect of Cu plasticity on keep-out zone size (D = 10 μm and H = 200 μm). (a) KOZ for different yield strengths with $\Delta T = -250$ °C. (b) KOZ size $(a_{\perp})$ calculated by the elastic and plastic models for different thermal loads ($\sigma_y = 200$ MPa).

For simplicity, Cu is assumed to be elastic and perfectly plastic in the FEA model. The plastic deformation in Cu is analyzed based on the associated flow rule of plasticity [25], in which the second invariant of the stress deviator tensor is used to determine the yield criterion based on the von Mises yield criterion. For electroplated Cu with a grain size in the micrometer range, previous studies [26], [27] have reported that the yield strength (σ_y) varies from 250 MPa to 100 ~ 150 MPa. To illustrate the effect of yield strength on the KOZ size, several yield strength values are chosen for the analysis subjected to a thermal load of $\Delta T = -250$ °C. In general, the yield strength depends on temperature, but it is assumed to be independent of temperature in the modeling study. The assumption may be oversimplified to properly account for the plasticity effect on mobility change; nevertheless, the plasticity is capable to induce local deformation in the via [4] and its effect on the carrier mobility will be examined.

To examine the difference between the plastic model and elastic model, we first calculate the size of the KOZ as a function of yield strength. Since the overall behavior of plasticity is similar for n- and p-type Si, only the effect for n-type Si with [100] channel direction is analyzed. The results are represented by $a_{//}$ and $a_{\perp}$, as shown in Fig. 11(a), where the KOZs calculated from the elastic model are also plotted for comparison. It is clear that the KOZ is small for low yield strength, as plastic deformation provides an efficient mechanism to relax stresses in Cu. Consequently, the KOZ increases with increasing yield strength. Eventually, when the yield strength becomes so high, plasticity rarely occurs under the thermal load ($\Delta T = -250$ °C). In that case, the calculated KOZ coincides with that from the elastic model.

This is followed by a study of the effect of plasticity on KOZ as a function of thermal load. In this paper, a fixed yield strength of $\sigma_y = 200$ MPa is used and the result is illustrated in Fig. 11(b) for different thermal loads, and compared with the elastic model. For small thermal loads below 200 °C, the KOZ from the plastic model follows the same curve as the elastic model, since the equivalent stress in the via does not exceed the yield strength (200 MPa). At around 200 °C, the results from the plastic model begin to deviate from the elastic model, when yielding occurs. The increase of KOZ is less in the plastic model due to stress relaxation. In particular, with a thermal load of 400 °C the KOZ in the plastic model is reduced by 25% as compared with the elastic model. Overall, the results from this

study suggest that the material plasticity can help in reducing the size of the KOZ. However, plasticity in the via has to be carefully considered since it could cause other reliability issues such as via extrusion [4].

V. Summary

In this paper, the effect of thermal stresses in TSV structures on the carrier mobility and the design of the keep-out zone have been systematically investigated by focusing on the characteristics of the near-surface stresses. The near-surface stresses were characterized using finite element analysis (FEA) and the results were used to evaluate the change in the carrier mobility induced by the piezoresistivity effect. The effect of the anisotropic properties of Si on the carrier mobility was studied for both n- and p-channel MOSFET devices. The extent of the keep-out zone (KOZ) was determined based on a 5% mobility change for n- and p-types of Si with device alignment along the [100] and [110] directions. The stress-induced mobility changes were found to be significant for n-type Si with the [100] device alignment and p-type Si with the [110] device alignment. Finally, the effects due to stress interactions in TSV arrays and Cu plasticity on the design of the KOZ were investigated. The effect of stress interaction on KOZ was found to depend on the ratio of the pitch to diameter of the TSV array. When this ratio is less 5, the stress interaction can increase the size of the KOZ. In contrast, the material plasticity was found to be useful in reducing the size of the KOZ. In 3-D IC processing, the intrinsic stresses generated during deposition of the barrier layer and the Cu via can also affect the final stress state near the TSV. Depending on the sign of the intrinsic stress, the final stress that the active devices experience could be higher or lower than the thermal stress alone. In addition, the interconnect structures above the active devices could also affect the stress characteristics and thus the size of KOZ. Those effects are not considered in the present study, and will be addressed in future studies.

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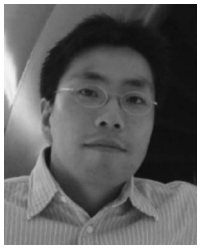

Suk-Kyu Ryu received the B.S. and M.S. degrees in aerospace engineering from Korea Aerospace University, Goyang, Korea, in 1998 and 2000, respectively, and the Ph.D. degree in aerospace engineering and engineering mechanics from The University of Texas, Austin, in 2011.

He had several years of working experience in the composite material industry, and he was a Researcher in a microsystem laboratory of Korea Institute of Science and Technology. Currently, he is a Senior Process Engineer with Applied Materials, Sunnyvale, CA. His research interests include the areas of thermomechanical and process-related reliability issues in electronics materials and microelectronic packaging.

Kuan-Hsun Lu received the B.S. and M.S. degrees in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2000 and 2002, respectively, and the Ph.D. degree in materials science and engineering from The University of Texas, Austin, in 2010.

He is currently a Senior Engineer with Intel Corporation, Chandler, AZ. His research interests include microelectronic packaging and advanced microelectronic technologies, including 3-D ICs.

Tengfei Jiang received the B.S. degree in materials science and engineering from Tsinghua University, Beijing, China, in 2006 and the M.S. degree in materials science and engineering from The Ohio State University, Columbus, in 2009. She is currently working toward the Ph.D. degree in materials science and engineering from The University of Texas, Austin.

Currently, her research is focused on the thermomechanical reliability of 3-D nterconnects.

Jang-Hi Im (SM'04) received the B.S. degree in mechanical engineering from Seoul National University, Seoul, Korea, in 1964 and the M.S. degree in mechanical engineering and the Ph.D. degree in materials science and engineering from Massachusetts Institute of Technology, Cambridge, in 1971 and 1976, respectively.

He is currently a Research Professor with the Laboratory for Interconnect and Packaging, The University of Texas, Austin. Until 2004, he was with The Dow Chemical Company for 28 years, taking on various R&D positions, including Research Scientist in electronic materials. In this last capacity, he had headed materials science and adhesion efforts for BCB and SiLK dielectrics. He has more than 100 published papers and holds nine U.S. patents.

Rui Huang received the B.S. degree in theoretical and applied mechanics from the University of Science and Technology of China, Hefei, China, in 1994 and the Ph.D. degree in civil and environmental engineering, with specialty in mechanics, materials, and structures, from Princeton University, Princeton, NJ, in 2001.

In 2002, he joined the faculty at The University of Texas, Austin, where he is currently an Associate Professor of aerospace engineering and engineering mechanics and holds the position of Mrs. Pearlie Dashiell Henderson Centennial Fellowship in Engineering. His research interests include mechanics of integrated materials and structures at microscale and nanoscale, reliability of advanced interconnects and packaging for microelectronics, and mechanical instability of thin films and nanostructures.

Paul S. Ho (M'91–SM'93–F'02) received the Ph.D. degree in physics from Rensselaer Polytechnic Institute, Troy, NY.

He joined the Department of Materials Science and Engineering, Cornell University, Ithaca, NY, in 1966, where he became an Associate Professor in 1972. In 1972, he joined the IBM T. J. Watson Research Center, where he became the Senior Manager of the Interface Science Department in 1985. In 1991, he joined the faculty at The University of Texas, Austin, and was appointed as Cockrell Family Regents Chair in Materials Science and Engineering, where he is currently the Director of the Laboratory for Interconnect and Packaging. His current research includes the areas of materials and processing science for interconnect and packaging applications.