Study of Stresses and Plasticity in Through-Silicon Via Structures for 3D Interconnects by X-Ray Micro-Beam Diffraction

Tengfei Jiang, Chenglin Wu, Nobumichi Tamura, Martin Kunz, Byoung Gyu Kim, Ho-Young Son, Min-Suk Suh, Jay Im, *Senior Member, IEEE*, Rui Huang, and Paul S. Ho, *Fellow, IEEE*

***Abstract*—X-ray microbeam diffraction measurements were conducted for copper (Cu) through-silicon via (TSV) structures. This technique has the unique capability to measure stress and deformation in Cu and in silicon with submicron resolution, which enables direct observation of the local plasticity in Cu and the deformation induced by thermal stresses in TSV structures. Grain growth in Cu vias was found to play an important role in controlling the stress relaxation during thermal cycling and, thus, the residual stress and plasticity in the TSV structure. The implication of the local plasticity on TSV reliability is discussed based on the results from this study and finite element analysis.**

***Index Terms*—TSV, X-ray microbeam diffraction, thermal stress, local plasticity.**

I. Introduction

THREE-DIMENSIONAL (3D) integration with through-silicon vias (TSVs) has emerged as an effective approach to overcome the wiring limit of on-chip interconnects beyond the 22 nm technology node. By using the Cu vias to provide short vertical interconnects in die stacks, the electrical performance, power consumption, and form factor can be much improved for 3D integrated circuits [1]–[3]. However, due to the large mismatch of thermal expansion coefficients (CTE) between the Cu vias and Si wafer, considerable thermal stresses are generated in and around the Cu vias, which can lead to serious reliability issues in the 3D integrated structures [4]–[6]. The thermal stress in TSV structures has generated great research interests, and several techniques have been employed to study the thermal stresses, including micro-Raman spectroscopy [7], [8], wafer curvature method [9], [10], and electrical measurement [11], [12]. Each of these techniques has certain inherent limitations. For example, micro-Raman spectroscopy can measure stresses in Si with submicron resolution, but not in Cu, and the measured stress is limited to certain combinations of the in-plane stress components [8], [9]. The wafer curvature method provides a global measurement of the volume-averaged stress in the Cu vias, but lacks the capability to resolve detailed stress distributions in individual vias [10], [11]. Nevertheless, in combination with finite element analysis (FEA), considerable progress has been made in the measurement and analysis of the stress behavior of the TSVs. In particular, the near-surface stress behavior has been found to be distinctly different from that of thin films, which can be attributed to the 3D confinement effect by the Si wafer surrounding the vias in the TSV structure [14]. Evolution of the Cu grain structure during thermal cycling was found to be important in controlling the stress characteristics [11]. During heating, Cu grain growth dominated in stress relaxation. During subsequent cooling, with the grain structure stabilized, the TSV exhibited a nearly linear elastic behavior, accumulating large residual stresses in both Cu and Si. The residual stress can degrade carrier mobility and directly impact the size of the keep-out zone (KOZ) for devices [6]. FEA modeling suggested that the Cu vias remain largely elastic with localized plasticity near the top of the via at the Cu/Si interface [11]. The local plasticity could enhance the interfacial adhesion, effectively changing the potential mechanism for via "pop-up" from interfacial debonding to plastic extrusion during thermal processing.

Results of previous studies highlight the importance of the local plasticity and the impact of the residual stress near the wafer surface on TSV reliability and device performance. However, the experimental methods described earlier lack the capability to directly measure the local plasticity and near-surface residual stress characteristics. In this study, X-ray micro-beam diffraction is used to investigate the stress and plasticity characteristics in a blind via structure, where the vias are etched partially into, but not completely, through the Si wafer. The X-ray micro-beam diffraction technique has the unique capability to examine both Cu and Si with submicron resolution [15]–[17], which enables the direct observation of the local plasticity in Cu and the stress/strain distribution in the surrounding Si. The micro-diffraction results are correlated to the wafer curvature measurements, and the local plasticity are traced to Cu yielding induced by grain growth and dislocation creep during thermal processing. Combining with elastic-plastic FEA, the effect of

Manuscript received December 13, 2013; revised March 2, 2014; accepted March 3, 2014. Date of publication March 11, 2014; date of current version June 3, 2014. This work was supported by the Semiconductor Research Corporation.

T. Jiang, J. Im, and P. S. Ho are with the Microelectronics Research Center and the Texas Materials Institute, The University of Texas at Austin, Austin, TX 78712 USA (e-mail: paulho@mail.utexas.edu).

C. Wu and R. Huang are with the Department of Aerospace Engineering and Engineering Mechanics, The University of Texas at Austin, Austin, TX 78712 USA (e-mail: ruihuang@mail.utexas.edu).

N. Tamura and M. Kunz are with the Advanced Light Source, Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA (e-mail: ntamura@lbl.gov).

B. G. Kim, H.-Y. Son, and M.-S. Suh are with SK Hynix Inc., Icheon 467-866, Korea (e-mail: hoyoung.son@sk.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2014.2310705

1530-4388 © 2014 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

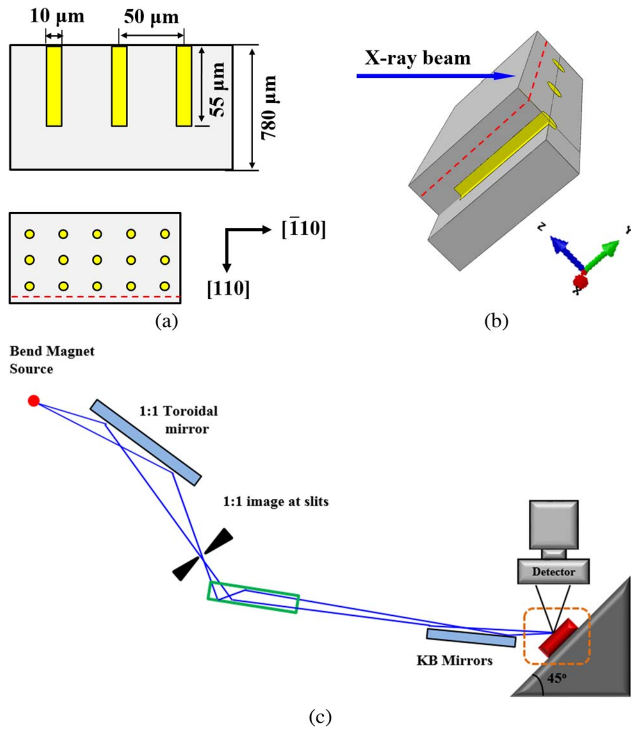


Fig. 1. Illustrations of (a) the TSV sample used for X-ray measurements. The dashed line indicates the location of the polished plane; (b) the sample set-up for X-ray micro-beam diffraction and (c) the layout of the X-ray micro-beam diffraction set-up.

Cu yielding on residual stress and local plasticity is elucidated, and the effects on via extrusion and device keep-out zone (KOZ) are discussed.

II. Experiments

The samples used in this study are blind Cu vias fabricated in a 780 μm thick (001) Si wafer. The via diameter is 10 μm, and the via height is 55 μm. The Cu vias are patterned in periodic arrays with 40 μm spacing along the [110] direction and 50 μm spacing along the [$\bar{1}$10] direction of the Si wafer, as shown in Fig. 1(a). The TSV structure was fabricated by the standard etching and electroplating processes, which consisted of etching the via holes in Si, deposition of 0.4 μm oxide dielectric, 0.1 μm Ta barrier and Cu seed layers, and electroplating of Cu to fill the vias. To study the thermal stresses, thermal cycling measurements were carried out under various conditions, with the TSV samples thermal cycled from room temperature (RT) to 200 °C, 300 °C, and 400 °C. To prepare for X-ray micro-beam diffraction measurements, all samples were mechanically polished along a Si [110] plane perpendicular to the wafer surface to a position about a few microns before a row of vias without exposing the Cu [see Fig. 1(a)]. Such sample preparation method allowed the Cu vias to be directly measured since the X-ray can penetrate through the Si, while avoiding the adverse polishing effect on Cu.

The X-ray micro-beam diffraction measurement was carried out using beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL) [15]. The high brilliance X-ray source, advanced X-ray focusing optics,

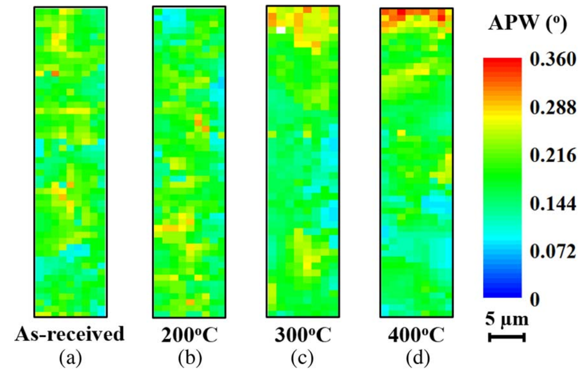


Fig. 2. Average peak width (APW) of Cu in the TSV samples (a) as-received and after thermal cycling to (b) 200 °C, (c) 300 °C, and (d) 400 °C.

and a high precision sample stage enable a submicron resolution to be achieved for local stress measurements [16]. Scanning X-ray microdiffraction with polychromatic beam (white beam) was performed on the polished cross-section of the TSV samples described above with X-ray energies from 5 keV to 22 keV. The X-ray micro-beam was focused to a spot size of 1 μm × 1 μm, and the scan step size was 1 μm/step. The sample was mounted in a 45° reflective geometry with the Laue diffractions collected by a DECTRIS Pilatus pixel array detector vertically positioned at ∼147 mm distance from the sample area. The sample and the X-ray microdiffraction measurement set-ups are illustrated in Fig. 1(b) and (c).

III. Scanning X-Ray Microdiffraction Measurements

The white beam microdiffraction generated a Laue pattern for each point in the scan matrix. By analyzing the Laue patterns, complete grain orientation, deviatoric strain tensors, and evidence of plasticity can be obtained [16]. In this study, the Laue reflections collected from scanning of the Cu TSVs were indexed for Cu and Si separately. In Fig. 2, maps of the average peak width (APW) of the indexed Laue reflections are plotted for the as-received sample and the samples after thermal cycling to the temperatures described before. An increased APW can be clearly seen for Cu vias after thermal cycling to 300 °C and 400 °C, concentrating particularly in the area near the top of the vias. In the Cu via after thermal cycling to 200 °C, there seems to be little change of the APW. To further show this peak broadening, the peak shapes are examined for Laue reflections from Cu grains near the top of the via and the middle of the via for the as received TSV samples and samples thermal cycled to 200 °C, 300 °C, and 400 °C, and the results are compared in Fig. 3.

The broadening of the APW in the Cu via can be correlated to an increase of the geometrically necessary dislocations and microstrains induced by diffusional creep in the Cu grains during thermal cycling and provides a direct evidence of the local plastic deformation in the Cu grains near the top of the via [18]–[20]. This results suggest that local plasticity has occurred significantly after thermal cycling to 400 °C, but not so after thermal cycling to 200 °C. In addition, for the Cu via subjected to thermal cycling temperatures as high as 400 °C, splitting of the Laue reflection into multiple peaks has occurred for grains

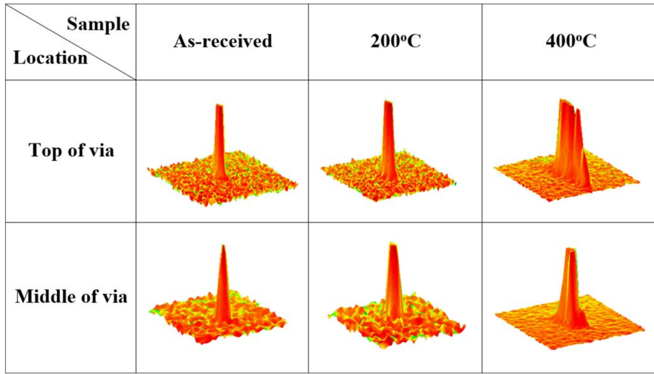


Fig. 3. Shapes of the $(1\bar{1}3)$ Laue reflection from grains near the top and in the middle of the vias for the as-received sample and samples subjected to thermal cycling of 200 °C and 400 °C.

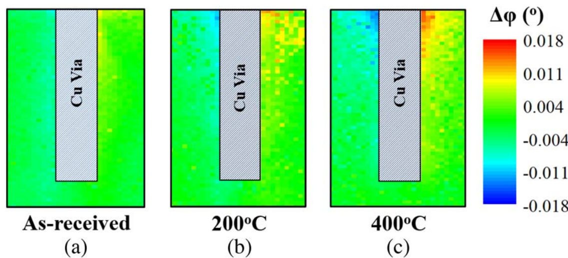
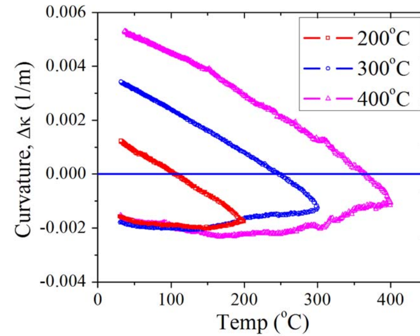


Fig. 4. Relative changes of the out-of-plane orientation in Si in the TSV samples: (a) as-received and after thermal cycling to (b) 200 °C and (c) 400 °C. The diameter of the Cu via is 10 μm.



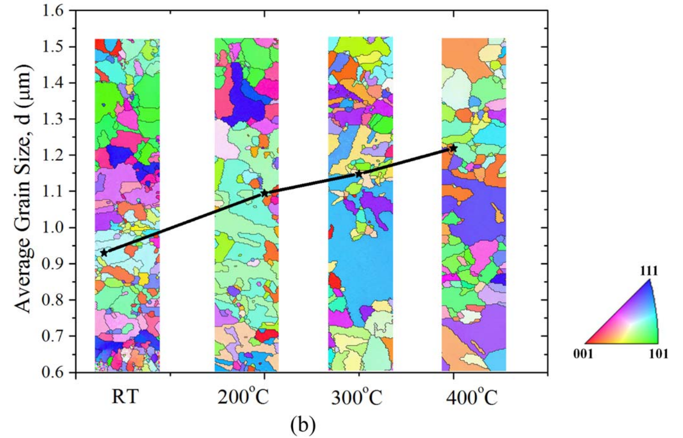


Fig. 5. (a) Precision wafer curvature measurements for three TSV samples thermal cycled to 200 °C, 300 °C, and 400 °C, respectively. (b) Grain growth observed by EBSD and mappings of the grains in the Cu vias.

near the via top, as shown in Fig. 3. The peak splitting suggests the formation of subgrains, which can be caused by the large degree of plastic deformation in the Cu grains [18], [19].

For Si, the Laue patterns are indexed; and the out-of-plane orientation, φ, defined as the angle between the [100] crystal direction and the (110) polished surface normal, is calculated and plotted in Fig. 4. Interestingly, a gradient of the out-of-plane orientation, $\Delta\varphi$, became visible around the top of the via under thermal cycling. The orientation gradient was not observed in the as-received sample but became observable after heating to 200 °C. The bending deformation became more pronounced near the top of the via after thermal cycling to 400 °C, suggesting a higher residual stress in Si around the Cu via. The local lattice rotation of Si was found to be in opposite directions on two sides of the Cu via, indicating an axially symmetric bending of the Si lattice around the Cu via. This axial symmetric Si lattice bending can be attributed to the elastic deformation of Si caused by the residual stresses in Si in the TSV structure. The residual stress is known to be a source for reliability concern. In particular, the stress/strain in Si can cause mobility changes through the piezoresistive effect and affects the size of the KOZ for CMOS devices [14].

The results from the X-ray micro-beam diffraction measurements were qualitatively correlated to the wafer curvature measurements, which have been reported previously [10], [11]. TSV samples with the same geometry and processing conditions were thermal cycled to 200 °C, 300 °C, and 400 °C; and the measured curvature-temperature behaviors were plotted in Fig. 5(a). During heating, nonlinear curvature behavior was attributed to stress relaxation in Cu, which can be attributed to grain growth and diffusional creep. Grain growth in the Cu vias with increasing temperature was measured by EBSD and summarized in Fig. 5(b), where both the grain size and the grain mapping of the Cu via are shown. The results from EBSD indicate that grain growth continued in the TSV with increasing temperature. To delineate these two mechanisms, isothermal stress relaxation measurements were performed at 200 °C, 300 °C, and 400 °C in the thermal cycling experiment. The results indicated that grain growth dominated the stress relaxation, although the contribution from diffusional creep increased with temperature as expected. At 400 °C, with the grains size stabilized during the heating cycle, diffusional creep was found to contribute about 30% to stress relaxation. Together, they accounted for the stress relaxation and, consequently, the residual stress in the TSV after cooling down to RT. The residual stress induced the bending deformation of the Si lattice near the top surface of the via, which increased with the thermal cycling temperature. This is consistent with results from the X-ray microdiffraction measurements shown in Fig. 4.

IV. Finite Element Analysis (FEA)

To further understand results from the X-ray micro-beam diffraction and wafer curvature measurements, a three-dimensional FEA model was constructed using the commercial finite-element package, ABAQUS (v6.12), as shown in Fig. 6. Linear 3-D solid elements (C3D8R) were used with a relatively fine mesh (element size $= 0.5$ μm) for the Cu via and an

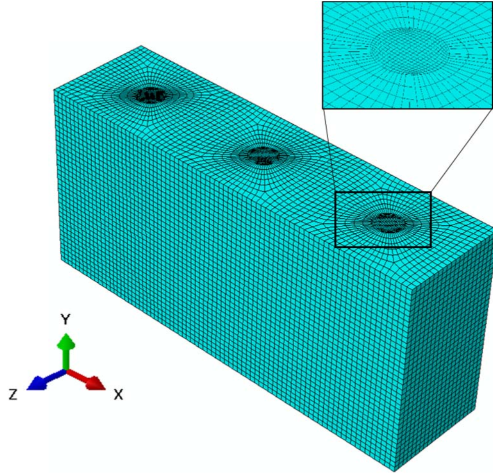


Fig. 6. Three-dimensional FEA model, showing only the upper portion with TSVs; the full model is 780 μm thick.

increasingly coarse mesh for the Si away from the vias. Symmetric boundary conditions were applied on all sides of the model to simulate the periodic TSV arrays, while the upper surface is traction free and the bottom is fixed. The material properties used are as follows: Young's modulus, $E_{Cu} = 110$ GPa and $E_{Si} = 130$ GPa; Poisson's ratio, $\nu_{Cu} = 0.35$ and $\nu_{Si} = 0.28$; CTE, $\alpha_{Cu} = 17$ ppm/°C and $\alpha_{Si} = 2.3$ ppm/°C; the thin oxide layer is ignored. For simplicity, Cu is assumed to be elastic and perfectly plastic with the yield strength of 250 MPa.

The FEA simulations were conducted for the cooling process with $\Delta T = -70$ °C, $\Delta T = -220$ °C, and $\Delta T = -320$ °C, corresponding to thermal loads from the zero-curvature temperature (assumed to be stress free) to RT for the three thermal cycles in Fig. 5(a) [11]. The results show that for $\Delta T = -70$ °C, the von Mises stress, σ_v, is largest at the top of the via near the Cu/Si interface but below 250 MPa in the entire via. Therefore, no plastic yielding is expected for this cooling condition. For the higher thermal loads of $\Delta T = -220$ °C and $\Delta T = -320$ °C, the stress in Cu reaches the yielding strength of 250 MPa near the top of the via, hence inducing local plastic deformation. The amount of plastic deformation in the Cu via is described by the equivalent plastic strains, ε_{eq}^p as $\varepsilon_{eq}^p = (3/2)\sqrt{\varepsilon_{ij}^p \cdot \varepsilon_{ij}^p}$, where ε_{ij}^p are the plastic strains. In Fig. 7, the equivalent plastic strains were projected to the x-y plane to compare with the micro-beam measurements. For $\Delta T = -70$ °C, ε_{eq}^p is zero in the entire via for the absence of plasticity. For $\Delta T = -220$ °C, the plastic strain accumulates locally near the top of the via. For $\Delta T = -320$ °C, the amount of plasticity is much greater but remains localized near the top of the via at the Cu/Si interface. The results from the FEA simulations are consistent with the X-ray micro-beam diffraction measurements. With increasing thermal cycling temperature, local plastic deformation occurs in the Cu vias, and the amount increases. The plastic deformation is more significant near the top of the via and results in the increase of dislocation densities in the Cu grains, which was observed in Figs. 2 and 3 as the broadening of the APW. The increase of APW was found to be most significant near the top of the via, in agreement with the FEA prediction. In this way, the X-ray micro-beam diffraction

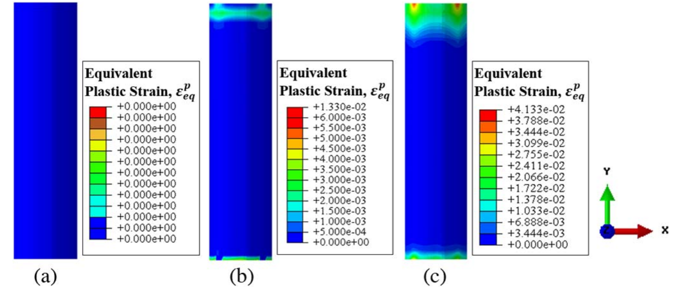


Fig. 7. Projected distribution of equivalent plastic strains for different thermal loads: (a) $\Delta T = -70$ °C, (b) $\Delta T = -220$ °C, (c) $\Delta T = -320$ °C.

studies in this work provide the experimental evidence of the local plasticity in TSVs.

V. Implication on TSV Reliability

Via extrusion and stress-induced mobility changes are two important reliability issues for 3D integration with TSVs. Results from the wafer curvature measurements show overall stress build-up in the TSV structure during thermal cycling, while X-ray microbeam diffraction provided evidence of local plastic deformation near the top of the Cu via. Together, the stress build-up and plasticity lead to Cu extrusion or "pop-up" of the TSV top surface after thermal cycling, which has been confirmed by atomic force microscopy (AFM) measurements [21]. The near surface stresses in Si surrounding the Cu vias can cause mobility change through the piezoresistive effect, and the magnitude of the residual stress directly affects the size of the keep-out zone for CMOS devices [6].

Prior studies suggest that grain growth plays an important role in controlling the stress relaxation and, thus, the residual stress in the Cu TSVs during thermal cycling [9]–[11]. The stress relaxation at high temperatures facilitated by grain growth sets a zero-stress temperature, which increases with the temperature of thermal cycling. Consequently, the residual stress increases after cooling to RT, which, in turn, leads to more plastic deformation in the Cu vias and more lattice deformation in Si surrounding the vias. On the other hand, the yield strength in Cu would decrease with grain growth following the classical Hall-Petch relation. This suggests that the extent of the plastic deformation in the via can be controlled by optimizing the grain growth in the Cu via. Since grain growth in electroplated Cu depends on the additive chemistry and other processing conditions, this suggests the possibility that the stress characteristics and, thus, the thermo-mechanical reliability of the Cu TSVs can be optimized by controlling the electrochemistry and thermal processing of TSV fabrication.

VI. Summary

In summary, we have conducted synchrotron X-ray microbeam diffraction measurements on TSV structures. The measurements provided direct evidence of the local plasticity in Cu via and the residual stress in Si. The results from the X-ray microdiffraction measurements were qualitatively correlated with precision wafer curvature measurements and FEA simulations. Grain growth was found to play an important role in controlling the stress relaxation during thermal cycling and, thus, the residual stress and local plasticity in the Cu TSV.

The microdiffraction results are significant as they constitute a direct observation of the local plasticity in a Cu TSV and the near-surface strain distribution in the surrounding Si. The local plasticity induces irreversible deformation at the top of TSV and is responsible for via extrusion during thermal cycling, which has important consequences on reliability. The near surface stresses extending several microns below the Si can cause mobility change through the piezoresistive effect to affect the size of the keep-out zone for CMOS devices. These are key aspects of the thermomechanical properties of TSV structures that control the reliability of 3D interconnects.

Acknowledgment

We are thankful to SK Hynix Inc. for providing the TSV specimens. The Advanced Light Source is supported by the Director, Office of Science, Office of Basic Energy Sciences, Materials Sciences Division, of the U.S. Department of Energy under Contract DE-AC02-05CH11231 at Lawrence Berkeley National Laboratory and University of California, Berkeley, CA, USA. The move of the micro-diffraction program from ALS beamline 7.3.3 onto to the ALS superbend source 12.3.2 was enabled through NSF Grant 0416243.

References

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] J. U. Knickerbocker, C. S. Patel, P. S. Andry, C. K. Tsang, L. P. Buchwalter, E. J. Sprogis, G. Hua, R. R. Horton, R. J. Polastre, S. L. Wright, and J. M. Cotte, "3-D silicon integration and silicon packaging technology using silicon through-vias," *IEEE J. Solid-State Circle*, vol. 41, no. 8, pp. 1718–1725, Aug. 2006.

[3] J. Lau, "Evolution and outlook of TSV and 3D IC/Si integration," in *Proc. Electron. Packag. Technol. Conf.*, 2010, pp. 560–570.

[4] S. Kang, S. Cho, K. Yun, S. Ji, K. Bae, W. Lee, E. Kim, J. Kim, J. Cho, H. Mun, and Y. L. Park, "TSV optimization for BEOL interconnection in logic process," in *Proc. IEEE Int. 3DIC*, 2012, pp. 1–4.

[5] J. Van Olmen, C. Huyghebaert, J. Coenen, J. Van Aelst, E. Sleeckx, A. Van Ammel, S. Armini, G. Katti, J. Vaes, W. Dehaene, E. Beyne, and Y. Travaly, "Integration challenges of copper through silicon via (TSV) metallization for 3D-stacked IC integration," *Microelectron. Eng.*, vol. 88, no. 5, pp. 745–748, May 2011.

[6] S. K. Ryu, K. H. Lu, T. Jiang, J. Im, R. Huang, and P. S. Ho, "Effect of thermal stresses on carrier mobility and keep-out zone around through-silicon vias for 3-D integration," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 255–262, Jun. 2012.

[7] W. S. Kwon, D. T. Alastair, K. H. Teo, S. Gao, T. Ueda, T. Ishigaki, K. T. Kang, and W. S. Yoo, "Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy," *Appl. Phys. Lett.*, vol. 98, no. 23, pp. 232106-1–232106-3, Jun. 2011.

[8] I. De Wolf, "Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits," *Semicond. Sci. Technol.*, vol. 11, no. 2, pp. 138–154, 1996.

[9] S. K. Ryu, Q. Zhao, J. Im, M. Hecker, P. S. Ho, and R. Huang, "Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects," *J. Appl. Phys.*, vol. 111, p. 063513, 2012.

[10] S. K. Ryu, T. Jiang, K. H. Lu, J. Im, H.-Y. Son, K.-Y. Byun, R. Huang, and P. S. Ho, "Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique," *Appl. Phys. Lett.*, vol. 100, no. 4, pp. 041901-1–041901-4, Jan. 2012.

[11] T. Jiang, S. K. Ryu, Q. Zhao, J. Im, R. Huang, and P. S. Ho, "Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 53–62, Jan. 2013.

[12] A. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, A. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. S. Tezcan, P. Soussan, J. H. Cho, A. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k/metal gate CMOS performance," in *Proc. IEEE IEDM*, 2010, pp. 2.2.1–2.2.4.

[13] D. Perry, J. Cho, S. Domae, P. Asimakopoulos, A. Yakovlev, P. Marchal, G. Van der Plas, and N. Minas, "An efficient array structure to characterize the impact of through silicon vias on FET devices," in *Proc. IEEE ICMTS*, 2011, pp. 118–122.

[14] S. K. Ryu, K. H. Lu, X. Zhang, J. H. Im, P. S. Ho, and R. Huang, "Impact of near-surface thermal stresses on interfacial reliability of through-silicon-vias for 3-D interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 35–43, Mar. 2011.

[15] M. Kunz, N. Tamura, K. Chen, A. A. MacDowell, R. S. Celestre, M. M. Church, S. Fakra, E. E. Domning, J. M. Glossinger, J. L. Kirschman, G. Y. Morrison, D. W. Plate, B. V. Smith, T. Warwick, V. V. Yashchuk, H. A. Padmore, and E. Ustundag, "A dedicated superbend X-ray microdiffraction beamline for materials, geo-, and environmental sciences at the advanced light source," *Rev. Sci. Instrum*, vol. 80, no. 3, p. 035108, 2009.

[16] N. Tamura, A. A. MacDowell, R. Spolenak, B. C. Valek, J. C. Bravman, W. L. Brown, R. S. Celestre, H. A. Padmore, B. W. Batterman, and J. R. Patel, "Scanning X-ray microdiffraction with submicrometer white beam for strain/stress and orientation mapping in thin films," *J. Synchrotron. Radiat.*, vol. 10, pp. 137–143, 2003.

[17] A. S. Budiman, H.-A.-S. Shin, B.-J. Kim, S.-H. Hwang, H.-Y. Son, M.-S. Suh, Q.-H. Chung, K.-Y. Byun, N. Tamura, M. Kunz, and Y.-C. Joo, "Measurement of stresses in Cu and Si around through-silicon via by synchrotron X-ray microdiffraction for 3-dimensional integrated circuits," *Microelectron. Rel.*, vol. 52, no. 3, pp. 530–533, Mar. 2012.

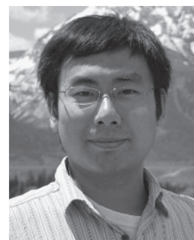
[18] B. C. Valek, J. C. Bravman, N. Tamura, A. A. MacDowell, R. S. Celestre, H. A. Padmore, R. Spolenak, W. L. Brown, B. W. Batterman, and J. R. Patel, "Electromigration-induced plastic deformation in passivated metal lines," *Appl. Phys. Lett.*, vol. 81, no. 22, pp. 4168–4170, Nov. 2002.

[19] B. C. Valek, N. Tamura, R. Spolenak, W. A. Caldwell, A. A. MacDowell, R. S. Celestre, H. A. Padmore, J. C. Braman, B. W. Batterman, W. D. Nix, and J. R. Patel, "Early stage of plastic deformation in thin films undergoing electromigration," *J. Appl. Phys.*, vol. 94, no. 6, pp. 3757–3761, Sep. 2003.

[20] E. Arzt, G. Dehm, P. Gumbsch, O. Kraft, and D. Weiss, "Interface controlled plasticity in metals: Dispersion hardening and thin film deformation," *Progr. Mater. Sci.*, vol. 46, no. 3/4, pp. 283–307, 2001.

[21] T. Jiang, C. Wu, L. Spinella, J. Im, N. Tamura, M. Kunz, H.-Y. Son, B. G. Kim, R. Huang, and P. S. Ho, "Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects," *Appl. Phys. Lett.*, vol. 103, no. 21, p. 211906, Nov. 2013.

Tengfei Jiang received the B.S. degree in materials science and engineering from Tsinghua University, Beijing, China, in 2006 and the M.S. degree in materials science and engineering from The Ohio State University, Columbus, OH, USA, in 2009. She is currently working toward the Ph.D. degree in materials science and engineering at The University of Texas at Austin, Austin, TX, USA, in 2010. Her current research interests include materials- and process-related reliability issues in advanced microelectronic technologies, including 3-D integrated circuits.



Chenglin Wu received the B.S. degree in Civil Engineering from Tongji University, Shanghai, China in 2006 and the M.S. degree in Civil Engineering from Lawrence Technological University, Michigan, in 2009. He has several years of working experience in the field of structural materials and mechanics. In 2013, he joined the Ph.D. program at the department of Aerospace Engineering and Engineering Mechanics at The University of Texas, Austin. His research interests are in the area of multi-scale computational mechanics.

Nobumichi Tamura, photograph and biography not available at the time of publication.

Martin Kunz, photograph and biography not available at the time of publication.

Byoung Gyu Kim, photograph and biography not available at the time of publication.

Ho-Young Son, photograph and biography not available at the time of publication.

Min-Suk Suh, photograph and biography not available at the time of publication.

Jay Im (SM'04) received the B.S. degree in mechanical engineering from Seoul National University, Seoul, Korea, in 1964 and the M.S. degree in mechanical engineering and the Ph.D. degree in materials science and engineering from the Massachusetts Institute of Technology, Cambridge, in 1971 and 1976, respectively.

He is currently a Research Professor with the Laboratory for Interconnect and Packaging, The University of Texas, Austin. Up until 2004, he was with The Dow Chemical Company for 28 years, taking on various R&D positions, including Research Scientist in electronic materials. In this last capacity, he had headed materials science and adhesion efforts for BCB and SiLK dielectrics. He has over 100 published papers and is the holder of nine U.S. patents.

Rui Huang received his B.S. degree in Theoretical and Applied Mechanics from the University of Science and Technology of China in 1994 and his Ph.D. degree in Civil and Environmental Engineering, with specialty in Mechanics, Materials, and Structures, from Princeton University in 2001.

In 2002, he joined the faculty at The University of Texas, Austin, where he is currently an associate professor of Aerospace Engineering and Engineering Mechanics and holds the position of Mrs. Pearlie Dashiell Henderson Centennial Fellowship in Engineering. His research interests include mechanics of integrated materials and structures at micro and nano scales, reliability of advanced interconnects and packaging for microelectronics, and mechanical instability of thin films and nanostructures.

Paul S. Ho (M'91–SM'93–F'02) received his Ph.D. degree in physics from Rensselaer Polytechnic Institute, Troy, NY.

He joined the Department of Materials Science and Engineering, Cornell University, Ithaca, NY, in 1966 and became an Associate Professor in 1972. In 1972, he joined the IBM T. J. Watson Research Center and became the Senior Manager of the Interface Science Department in 1985. In 1991, he joined the faculty at The University of Texas, Austin, and was appointed as Cockrell Family Regents Chair in Materials Science and Engineering, where he is currently the Director of the Laboratory for Interconnect and Packaging. His current research is in the areas of materials and processing science for interconnect and packaging applications.