# Processing Effect on Via Extrusion for TSVs in Three-Dimensional Interconnects: A Comparative Study

Tengfei Jiang, *Member, IEEE*, Laura Spinella, Jang-Hi Im, *Senior Member, IEEE*, Rui Huang, and Paul S. Ho, *Fellow, IEEE* 

Abstract—A comparative study has been performed to investigate the processing effects on via extrusion for through-silicon vias (TSVs) in 3-D integration. This paper is focused on three TSV structures with identical geometry but different processing conditions. The thermomechanical behavior, microstructure, via extrusion, and additives incorporated during electroplating are examined by various techniques, including the electron backscatter diffraction and the time-of-flight secondary ion mass spectroscopy. By comparing the stress, material, and via extrusion behaviors of the TSV structures, the effect of processing conditions, particularly electroplating and postplating annealing, on via extrusion are discussed.

*Index Terms*—Through-silicon via (TSV), via extrusion, thermal stress, electroplating.

#### I. INTRODUCTION

N three-dimensional (3D) integration, two or more thin dies are stacked and connected by through-silicon vias (TSVs). Such an integration scheme offers several distinct advantages to overcome the wiring limit imposed on chip performance, power dissipation and package form factor beyond the 14 nm technology node [1]-[3]. In the commonly used "via-middle" scheme, TSVs are incorporated into the wafer after fabrication of transistors and before processing the back-end-of-the-line (BEOL) interconnects. The fabrication of TSVs involves deepetching of via holes, deposition of oxide liner, diffusion barrier, and seed layers, electroplating of Cu to fill the via holes, and finally chemical-mechanical planarization (CMP) [4]. The thermal expansion mismatch between copper (Cu) and silicon (Si) can induce large thermal stresses in and round the TSV when it is subjected to temperature excursions during BEOL processing [5]. Several yield and reliability issues resulted from the thermal

Manuscript received October 8, 2015; revised May 11, 2016; accepted July 1, 2016. Date of publication July 18, 2016; date of current version December 1, 2016. This work was supported by the Semiconductor Research Corporation.

- T. Jiang is with the Department of Materials Science and Engineering and the Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando, FL 32816 USA (e-mail: Tengfei.Jiang@ucf.edu).
- L. Spinella, J.-H. Im, and P. S. Ho are with the Microelectronics Research Center and Texas Materials Institute, University of Texas, Austin, TX 78712 USA.
- R. Huang is with the Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712 USA.
- Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2016.2591945

stress have been reported for TSV. Cu extrusion or TSV "popup," which describes the irreversible vertical protrusion of Cu, is of particular concern since the vertical protrusion of Cu can damage the adjacent interconnect structures during fabrication or thermal cycling [5]–[7]. It is thus desirable to optimize the processing condition to minimize via extrusion. In this paper, by examining TSV structures with different electroplating and post-plating annealing conditions, the effect of TSV processing on via extrusion is investigated. Potential approaches to improve via extrusion reliability by microstructure control with optimized processing conditions are discussed.

#### II. EXPERIMENTS

#### A. Test Vehicle

TSV samples from two different sources were used in this study. Both sets of TSVs were blind vias with identical dimension of  $5.5 \times 50 \,\mu\mathrm{m}$  (diameter  $\times$  height) and were fabricated in 760  $\mu$ m thick Si wafers. The electroplating chemistries used to produce the two TSV sets were different, and are referred to as Chemistry A and Chemistry B. Details of Chemistry A and B were not disclosed by the suppliers. When received, the TSVs fabricated with Chemistry A had already been subjected to postplating annealing at 430 °C for 10 minutes prior to CMP. This set of TSV samples will be called Chem A-430C. The other set of TSVs fabricated with Chemistry-B received no post-plating annealing prior to CMP, and will be called ChemB-NA. To further compare these two TSV sets, the original ChemB-NA TSVs were annealed at 430 °C for 10 minutes and then underwent CMP. The resulting TSVs are called ChemB-430C. The rest of the study will focus on these three TSV samples which have identical geometry but different processing conditions.

### B. Thermo-Mechanical Characterization

Recent studies have shown that substrate curvature method can be extended from thin film to TSV structures and serves as an effective way to capture the materials and thermosmechanical behaviors of TSV structures [8]. Thermal cycling measurements were carried out on the three TSV samples, and the curvature-temperature behaviors after three thermal cycles to  $400\,^{\circ}\text{C}$  are plotted in Fig. 1.

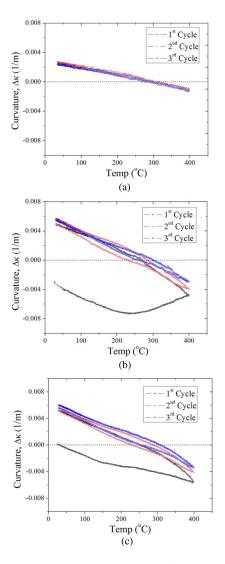


Fig. 1. Substrate curvature measurement of (a) ChemA-430C, (b) ChemB-NA, and (c) ChemB-430C.

ChemA-430 C shows linear curvature up to 400 °C throughout the measurement, suggesting that the Cu TSVs behave mostly linear elastic in this sample. ChemB-NA, on the other hand, has large relaxation above 200 °C during heating of the first half-cycle, which is followed by a small but visible nonlinearity during cooling of the first cycle and in subsequent cycles. Comparing to ChemB-NA, ChemB-430C showed less curvature relaxation. In the 2nd and 3rd cycles, hysteresis loops are clearly observed in ChemB-430C.

Isothermal measurements were also carried out, where the samples were heated to 400 °C and held for 1 hour before cooling to room temperature. The curvature changes at 400 °C are plotted as a function of time (t) in Fig. 2. To compare the amount of curvature relaxation, the curvatures at time t=0 are shifted to the same point. Here ChemA-430C has minimal curvature relaxation, while ChemB-NA showed significantly larger curvature change at 400 °C. The relaxation of ChemB-430C was slightly smaller than ChemB-NA but still much larger than ChemA-430C. The large curvature relaxation in both ChemB-NA and ChemB-430C indicates the presence of diffusional creep in these samples [9].

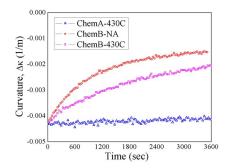


Fig. 2. Isothermal relaxation measurement of  ${\rm Chem}A\text{-}430C,~{\rm Chem}B\text{-NA},$  and  ${\rm Chem}B\text{-}430C.$ 

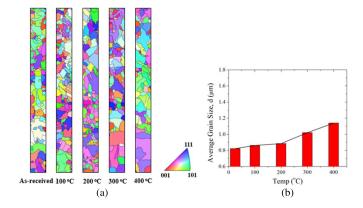


Fig. 3. Grain growth in Chem B-NA. (a) EBSD grain orientation map. (b) Grain size.

# C. Microstructure Analysis

The evolution of Cu grain structure during temperature cycling was studied by electron backscatter diffraction (EBSD). For each sample, individual thermal cycling tests to 100, 200, 300, and 400 °C were carried out, respectively. After each single temperature thermal cycling test, the TSVs were cross-sectioned by focused ion beam (FIB) for EBSD measurement. An "as-received" via was also examined to provide a reference point. Grain growth was observed only in ChemB-NA, occurring most noticeably beyond 200 °C, as shown in Fig. 3. For ChemA-430C and ChemB-430C, the grain structure appeared to be stable with no apparent size and orientation changes before and after thermal cycling to 400 °C.

The percentage of  $\Sigma 3$  boundary, which is a twin boundary for Cu, is analyzed. There is about 77%  $\Sigma 3$  boundary in ChemA-430C, which is much larger than the amount of  $\Sigma 3$  boundaries in ChemB-NA and ChemB-430C, which are 56% and 53%, respectively. For all three samples, there is no systematic change in the percentage of twin boundaries with increased thermal cycling temperatures.

## D. Via Extrusion

Via extrusion was examined by AFM after the samples were subjected to a single thermal cycling to 400  $^{\circ}$ C. The height profiles across the top of the vias before  $(H_0)$  and after thermal cycling  $(H_{400})$  are extracted and plotted in Fig. 4. The depression at the top surface of ChemA-430C and

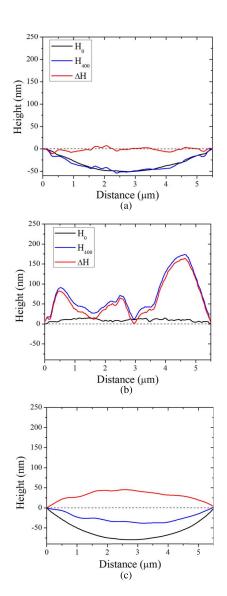


Fig. 4. Height profile across the via diameter for (a) ChemA-430C, (b) ChemB-NA, and (c) ChemB-430C. The red lines correspond to the net via extrusion ( $\Delta H = H_{400} - H_0$ ).

ChemB-430C is due to dishing effect in CMP. To show the extent of Cu protrusion after thermal cycling, the original via height,  $H_0$ , is subtracted from via height after thermal cycling,  $H_{400}$ . The difference,  $\Delta H = H_{400} - H_0$ , corresponds to the net via extrusion and is also plotted. For ChemA-430C, after thermal cycling to 400 °C, there is slightly increased surface roughness near grain boundaries but no apparent via extrusion. ChemB-NA has the most significant extrusion, which is non-uniform with hillocks and large height variations across the via top. There is still via extrusion for ChemB-430C but the magnitude is less than that for ChemB-NA. The maximum extrusion height is 7.0 nm, 173.9 nm, and 44.9 nm for ChemA-430C, ChemB-NA, and ChemB-430C respectively.

# E. Time-of-Flight Secondary Ion Mass Spectrometry

To examine the additive elements incorporated in Cu vias during electroplating, the TSV samples were cross-sectioned by FIB and measured by time-of-flight secondary ion mass

TABLE I COUNTS OF  $CL^-$ ,  $F^-$ ,  $S^-$ , and  $CN^-$  Elements IN the TSV (Normalized by  $CU^-$ )

Counts	ChemA-430C	ChemB-NA	ChemB-430C
Cl-	337.6	1.26	0.25
F-	147.2	10.9	8.44
s-	7.3	0.60	0.06
CN-	114.3	0.61	0.30

TABLE II
COMPARISON OF THREE TSV SAMPLES

	ChemA-430C	ChemB-NA	ChemB-430C
Annealing	430°C, 10min	No Annealing	430°C, 10min
Σ 3 boundary	77%	56%	53%
Amount of Incorporated Additives	Large	Small	Small
Max Extrusion (nm)	7.0	173.9	44.9
Grain growth	No	Yes	No
Relaxation	No	Yes	Yes

spectrometry (TOF-SIMS). Specifically, elements commonly found in electrodeposited Cu, including Cl-, F-, S-, and CN-were measured and summarized in Table I [10]. In comparison, ChemA-430C incorporated much larger amount of additives than both ChemB-NA and ChemB-430C. No noticeable changes in element concentration are observed for ChemA-430C and ChemB-430C after thermal cycling, while reduced element concentration is observed for ChemB-NA. The difference in the amount of additive elements as measured by TOF-SIMS together with the results on microstructure and stress behavior presented in this paper allow us to discuss qualitatively the effect of electroplating chemistry on TSV reliability even though detailed electroplating chemistry was not available.

## III. DISCUSSION

## A. Comparison of TSV Samples

The thermo-mechanical behavior, microstructure, extrusion behaviors, and additive elements of the three TSV samples are summarized in Table II.

Several differences can be seen among the three samples. Chem A-430C, which has minimal via extrusion, shows no relaxation both during thermal cycling and isothermal measurements. It has a stable grain structure with a large amount of twin boundaries, and has incorporated the most additive elements. In comparison, Chem B-NA, which has the largest via extrusion, shows largest relaxation during thermal cycling and isothermal measurements. There are fewer twin boundaries in Chem B-NA, and almost no grain growth during thermal cycling. The amount of additive elements incorporated in Chem B-NA is small and decreased with grain growth. Chem B-430C showed a small stress relaxation during thermal cycling but a large relaxation during isothermal annealing. It

has a stable grain structure with a small percentage of twin boundaries and small amount of additive elements. The amount of extrusion in ChemB-430C is smaller than ChemB-NA but larger than ChemA-430C.

#### B. Mechanism of Via Extrusion

Grain growth, plastic yielding by dislocation glide, and diffusional creep are three inelastic processes that could cause extrusion in the measured samples [11]. As no obvious via extrusion was observed in Chem A-430C, it can be assumed that for the given testing condition, all three inelastic processes are absent. For ChemB-430C, grain growth is absent but the hysteresis loop during thermal cycling and the curvature relaxation during isothermal annealing suggest that plastic yielding and diffusional creep are both present and have contributed to via extrusion [9], [10]. Due to the confinement of surrounding Si, plasticity in TSVs is mostly localized [12]. Given the relatively large curvature relaxation during isothermal measurement, it is likely that diffusional creep is more dominant in contributing to via extrusion. For ChemB-NA, the results suggest that all three inelastic processes have happened, which leads to the largest amount of via extrusion in that sample.

## C. Effect of Processing

The three TSV samples have identical geometries but different processing conditions, and the observation of their different extrusion behaviors provides clues to the effect of processing on via extrusion.

Post-plating annealing is known to stabilize grain structure [13], [14]. This is the case for ChemA-430C and ChemB-430C, where no change in microstructure, including grain size and orientation is observed. Comparing to ChemB-NA, the much-reduced via extrusion in ChemB-430C indicates that grain growth is suppressed through post-plating annealing, which is desirable. Similar observations have been made by other groups, and post-plating annealing has been recommended as a fix to the via extrusion problem [14]. Although this appears to be the case for ChemA-430C, the considerable extrusion in ChemB-430C suggests that annealing alone is not sufficient to resolve the via extrusion problem. Specifically, annealing does not seem to eliminate diffusional creep in ChemB-430C which is a major contribution to via extrusion in that sample.

Both grain boundary diffusion and interface diffusion could cause the creep behavior in ChemB-430C. In Cu, it is known that twin boundaries, especially  $\Sigma 3$  boundaries, have significantly smaller diffusivity than high angle boundaries [15]. Therefore, it is as expected that ChemA-430C, which has predominantly  $\Sigma 3$  boundaries, has very small diffusional creep. Similarly, with fewer  $\Sigma 3$  boundaries, ChemB-430C is more prone to grain boundary diffusion, which leads to larger extrusion.

Given that the major difference between ChemA-430C and ChemB-430C is electroplating condition, it is clear that electroplating plays a key role in controlling via extrusion. Although it is difficult to quantitatively discuss the effect of

electroplating conditions without details of the electroplating chemistry, the results seem to suggest that the larger amount of additive elements incorporated in  $\operatorname{Chem} A\text{-}430C$  may be beneficial for reduced via extrusion.

#### D. Discussion of Approaches to Reduce Via Extrusion

An interesting observation in this study is that ChemA-430C may be treated as an "ideal" TSV structure in terms of its resistance to via extrusion. Qualitatively, by examining ChemA-430C, useful guidelines to improve via extrusion reliability may be deduced.

First of all, the post-plating annealing at 430 °C helps to stabilize the grain structure in the sample. In recent years, the importance of stabilizing grain structure had been recognized by the industry, and a high temperature post-plating annealing step has been widely incorporated in the via middle process after electroplating of Cu and before CMP [6], [16], [17]. Secondly, the electroplating condition for ChemA-430C leads to the incorporation of relatively large amount of additive elements in the vias. Typically, the additives are segregated at grain boundaries, which could affect the properties of TSV in several ways. For example, the impurity elements could pin grain boundary movement and increase the resistance for dislocation glide. The pinning of impurity elements at grain boundaries could also affect microstructure evolution in the TSVs and their thermo-mechanical behaviors, which in turn change the via extrusion characteristics. Further studies with proper test structures will be needed to elucidate the role of electroplating. Finally, the microstructure of Cu plays an important role in via extrusion, both by affecting the yield strength and by diffusion at grain boundaries [18], [19]. To improve the resistance to via extrusion, it is important to optimize the microstructure of Cu. In particular, the results in this study and other studies seem to suggest that a large amount of twin boundaries is desirable [19].

# IV. SUMMARY

In this study, TSV structures with different electroplating and post-plating annealing conditions are studied. By examining the thermos-mechanical behaviors, microstructure, additive incorporation, and via extrusion behaviors, the inelastic processes in the Cu via contributing to via extrusion are discussed. Electroplating and post-plating annealing play important but different roles in controlling via extrusion. These conditions need to be optimized during the fabrication of TSVs to minimize via extrusion. Ideally, optimized processing condition would lead to an optimal microstructure similar to that of ChemA-430C with stabilized grain structure and a large amount of twin boundaries to suppress the inelastic processes and control via extrusion.

## ACKNOWLEDGMENT

The authors gratefully acknowledge financial support of this work by Semiconductor Research Corporation. We are thankful to SK Hynix Inc. and SEMATECH for providing the TSV specimens.

#### REFERENCES

- K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.
- [2] J. U. Knickerbocker et al., "Three-dimensional silicon integration," IBM J. Res. Dev., vol. 52, no. 6, pp. 553–569, 2008.
- [3] S. S. Iyer, "Three-dimensional integration: An industry perspective," MRS Bull., vol. 40, no. 3, pp. 224–232, 2015.
- [4] P. Garrou, C. Bower, and P. Ramm, Handbook of 3D Integration. Weinheim, Germany: Wiley-VCH, 2008.
- [5] T. Jiang, J. Im, R. Huang, and P. S. Ho, "Through-silicon via stress characteristics and reliability impact on 3D integrated circuits," MRS Bull., vol. 40, no. 3, pp. 248–256, 2015.
- [6] J. Van Olmen et al., "Integration challenges of copper Through Silicon Via (TSV) metallization for 3D-stacked IC integration," Microelectron. Eng., vol. 88, no. 5, pp. 745–748, 2011.
- [7] D. Zhang, K. Hummler, L. Smith, and J. J.-Q. Lu, "Backside TSV protrusion induced by thermal shock and thermal cycling," in *Proc. IEEE Electron. Compon. Technol. Conf.*, 2013, pp. 1407–1413.
- [8] T. Jiang, S.-K. Ryu, Q. Zhao, J. Im, R. Huang, and P. S. Ho, "Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias," *Microelectron. Reliab.*, vol. 53, no. 1, pp. 53–62, 2013
- [9] D. Gan, P. S. Ho, R. Huang, J. Leu, J. Maiz, and T. Scherban, "Isothermal stress relaxation in electroplated Cu films. I. Mass transport measurements," *J. Appl. Phys.*, vol. 97, no. 10, 2005, Art. no. 103531.
- [10] P. M. Vereecken, R. A. Binstead, H. Deligianni, and P. C. Andricacos, "The chemistry of additives in damascene copper plating," *IBM J. Res. Dev.*, vol. 49, no. 1, pp. 3–18, 2005.
- [11] H. J. Frost and M. F. Ashby, Deformation-Mechanism Maps: The Plasticity and Creep of Metals and Ceramics. Oxford, U.K.: Pergamon, 1982.
- [12] T. Jiang et al., "Plasticity mechanism for copper extrusion in throughsilicon vias for three-dimensional interconnects," Appl. Phys. Lett., vol. 103, no. 21, 2013, Art. no. 211906.
- [13] J. De Messemaeker et al., "Impact of post-plating anneal and throughsilicon via dimensions on Cu pumping," in Proc. IEEE Electron. Compon. Technol. Conf., 2013, pp. 586–591.
- [14] I. De Wolf et al., "Cu pumping in TSVs: Effect of pre-CMP thermal budget," Microelectron. Reliab., vol. 51, no. 9–11, pp. 1856–1859, 2011.
- [15] L. E. Murr, Interfacial Phenomena in Metals and Alloys. Reading, MA, USA: Addison-Wesley, 1975.
- [16] J. C. Lin et al., "High density 3D integration using CMOS foundry technologies for 28 nm node and beyond," in *Proc. IEEE IEDM*, 2010, pp. 2.1.1–2.1.4.
- [17] T. C. Tsai et al., "CMP process development for the via-middle 3D TSV applications at 28 nm technology node," *Microelectron. Eng.*, vol. 92, pp. 29–33, 2011.
- [18] T. Jiang, C. Wu, J. Im, R. Huang, and P. S. Ho, "Impact of grain structure and material properties on via extrusion in 3-D interconnects," *J. Microelectron. Electron. Packag.*, vol. 12, pp. 118–122, 2015.
- [19] J. De Messemaeker *et al.*, "Correlation between Cu microstructure and TSV Cu pumping," in *Proc. IEEE 64th ECTC*, 2014, pp. 613–619.

**Tengfei Jiang** (M'12) received the B.S. degree from Tsinghua University, Beijing, China, in 2006, the M.S. degree from The Ohio State University, Columbus, OH, USA, in 2009, and the Ph.D. degree from The University of Texas at Austin, Austin, TX, USA, in 2015, all in materials science and engineering.

She is an Assistant Professor with the Department of Materials Science and Engineering and the Advanced Materials Processing and Analysis Center, University of Central Florida, Orlando, FL, USA. Her research interests include materials characterization by synchrotron radiation, reliability of emerging interconnect and packaging systems, micro/nanofabrication, and novel drug delivery devices.

**Laura Spinella** received the B.S. degree in materials science and engineering from Rice University, Houston, TX, USA, in 2012. She is currently working toward the Ph.D. degree in materials science and engineering at The University of Texas at Austin, Austin, TX, with an anticipated graduation date in 2017.

She has completed research internships with Georgia Institute of Technology, Atlanta, GA, USA; the University of Colorado at Boulder, Boulder, CO, USA; and Rice University investigating novel materials and processes. Her dissertation research is focused on the stress and reliability of through-silicon vias for 3-D integration.

**Jang-Hi Im** (SM'04) received the B.S. degree in mechanical engineering from Seoul National University, Seoul, South Korea, in 1964 and the M.S. degree in mechanical engineering and the Ph.D. degree in materials science and engineering from Massachusetts Institute of Technology, Cambridge, MA, USA, in 1971 and 1976, respectively.

Up until 2004, he was with The Dow Chemical Company for 28 years, taking on various R&D positions, including Research Scientist in electronic materials. In this last capacity, he had headed materials science and adhesion efforts for Benzocyclobutene and SiLK dielectrics. He is currently a Research Professor with the Laboratory for Interconnect and Packaging, The University of Texas, Austin, TX, USA. He has over 100 published papers and is the holder of nine U.S. patents.

**Rui Huang** received the B.S. degree in theoretical and applied mechanics from the University of Science and Technology of China, Hefei, China, in 1994 and the Ph.D. degree in civil and environmental engineering, with specialty in mechanics, materials, and structures from Princeton University, Princeton, NJ, USA, in 2001.

In 2002, he joined the Faculty with The University of Texas, Austin, TX, USA, where he is currently an Associate Professor of aerospace engineering and engineering mechanics and holds the position of Mrs. Pearlie Dashiell Henderson Centennial Fellowship in engineering. His research interests include mechanics of integrated materials and structures at micro- and nanoscales, reliability of advanced interconnects and packaging for microelectronics, and mechanical instability of thin films and nanostructures.

**Paul S. Ho** (M'91–SM'93–F'02) received the Ph.D. degree in physics from Rensselaer Polytechnic Institute, Troy, NY, USA.

He joined the Department of Materials Science and Engineering, Cornell University, Ithaca, NY, in 1966 and became an Associate Professor in 1972. In 1972, he joined the IBM T. J. Watson Research Center and became the Senior Manager with the Interface Science Department in 1985. In 1991, he joined the Faculty with The University of Texas, Austin, TX, USA, and was appointed as Cockrell Family Regents Chair in materials science and engineering, where he is currently the Director with the Laboratory for Interconnect and Packaging. He is also with the Texas Materials Institute, The University of Texas. His current research interests include materials and processing science for interconnect and packaging applications.