

# Material Characterization and Failure Analysis of Through-Silicon Vias

Chenglin Wu, Tengfei Jiang, Jay Im, Kenneth M. Liechti, Rui Huang and Paul S. Ho

Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712, USA

Microelectronics Research Center and Texas Materials Institute, University of Texas, Austin, TX 78712, USA

Email: [ruihuang@mail.utexas.edu](mailto:ruihuang@mail.utexas.edu); [paulho@mail.utexas.edu](mailto:paulho@mail.utexas.edu)

**Abstract -** In this paper, the effects of Cu microstructure on the mechanical properties of TSV and via extrusion are studied using two types of though-silicon vias (TSVs) with different grain size distributions. A direct correlation is found between the Cu grain size and the mechanical properties of the TSVs. An analytical model is used to explore the relationship between the mechanical properties and via extrusion. The results show that small and uniform grains in the Cu vias led to smaller via extrusion. Such grain structures are effective for reducing via extrusion failure to improve TSV reliability.

## I. INTRODUCTION

Copper (Cu) through-silicon via (TSV) is a critical element in three-dimensional (3D) integrated circuits. Typically, fabrication of TSVs involves etching of via holes, deposition of liner and Cu seed layers, electroplating of Cu, post-electroplating annealing, and CMP removal of Cu overburden. In the via-middle scheme widely adopted for 3D integration, the back-end-of-the-line (BEOL) layers are deposited on top of the wafer after the fabrication of TSVs. As one of the reliability issues, extrusion of the Cu vias occurs primarily during the BEOL processing, which can cause the BEOL layers to deform, leading to mechanical and electrical failures of the interconnect structures (Fig. 1) [1-5]. Thus via extrusion has been a major concern for yield and reliability of 3D integration. Previous studies have suggested that the stress and mechanical properties of the Cu via directly affect via extrusion [4-6]. The underlying mechanism of via extrusion has been examined by considering plastic deformation in Cu and via/Si interfacial sliding [7,8]. For the purpose of process optimization, it is important to establish a correlation between the microstructures of the Cu via and the mechanical properties, which in turn can be correlated to via extrusion. In this work, we characterized the microstructures and mechanical properties of Cu TSVs, followed by measurements and modeling of via extrusion.

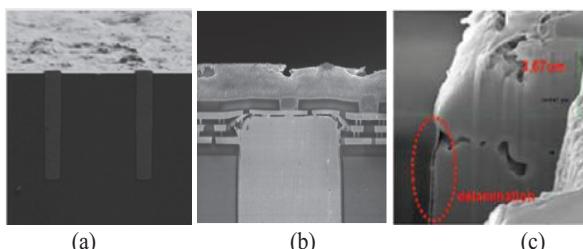


Fig. 1. Observations of via extrusion and failure in TSV structures: (a) Via extrusion after thermal cycling [4]; (b) and (c) Fracture and delamination due to via extrusion [3].

## II. MICROSTRUCTURES OF COPPER VIAS

The TSV samples used in this study were fabricated using the standard via-middle scheme. The via diameter was  $D = 5.5 \mu\text{m}$  and the via depth was  $H = 55 \mu\text{m}$ . The total thickness of the wafer was  $780 \mu\text{m}$ . Two different processing conditions were used to fabricate two types of TSVs with different microstructures, referred to as TSV-A and TSV-B. A number of vias from each type were cross-sectioned by focused ion beam (FIB) and their microstructures were measured by electron backscatter diffraction (EBSD). Both types of vias were found to have essentially random grain orientations (Fig. 2a). However, the grain size distributions were different (Fig. 2b): in TSV-A, the grain sizes were relatively uniform while the distribution in TSV-B was rather polarized, with several large grains mixing with small grains. The large grains in TSV-B sometimes spanned across the entire via diameter. This can be seen from the grain mapping and grain size distribution in Figure 2. Quantitatively, the average grain size was found to be  $2.83 \mu\text{m}$  for TSV-A and  $3.82 \mu\text{m}$  for TSV-B.

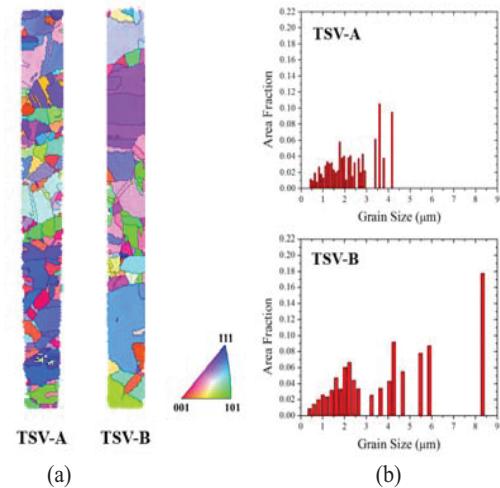


Fig. 2. EBSD measurement of Cu microstructures for TSV-A and TSV-B: (a) grain mapping; (b) grain size distributions.

## III. MECHANICAL PROPERTIES OF COPPER VIAS

To determine the elastic and plastic properties of the Cu vias, nanoindentation measurements were carried out. For several vias of each type, the BEOL layers were removed by FIB, and then quasi-static indentations were conducted on the top of the vias using Hysitron TI 950 TribolIndenter® equipped with a

Berkovitch diamond tip. A two-segment load versus time profile was applied with a loading/unloading rate of 100 nN/s and a peak load of 800  $\mu$ N. Figure 3 shows the measured load-displacement responses. The elastic moduli of the Cu vias were deduced from the unloading curves based on the Oliver-Pharr method [9], as shown in Figure 4. The average elastic modulus was found to be 117 GPa for TSV-A and 93 GPa for TSV-B. The elastic modulus for TSV-B is lower than typically expected for Cu (~110 GPa) based on previous studies on electroplated Cu thin films [10], which may be related to the surface roughness or the grain textures near the top surface of the via.

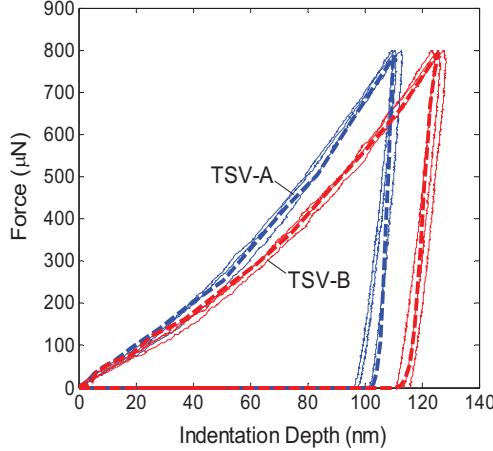


Fig. 3. Nanoindentation measurements for TSV-A (red) and TSV-B (blue), in comparison with FEA simulations (dashed lines).

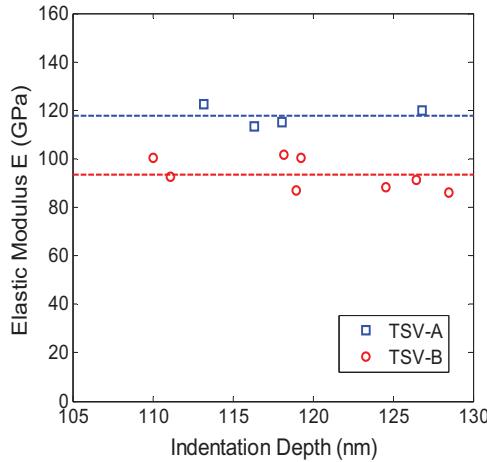


Fig. 4. Elastic modulus of Cu vias extracted from nanoindentation measurements.

To determine the plastic properties of the Cu vias, an axisymmetric finite element analysis (FEA) model was constructed to simulate the nanoindentation experiments (Fig. 5). An elastic diamond indenter with the cono-spherical shape was used with a tip radius of 100 nm. The material properties used for the diamond tip were:  $E_i = 1222$  GPa and  $v_i = 0.2$ . For the Cu vias, the average elastic moduli obtained from the nanoindentation measurements were used for TSV-A and TSV-B along with Poisson's ratio  $v_{\text{Cu}} = 0.35$ . The elastic

properties for Si were:  $E_{\text{Si}} = 130$  GPa and  $v_{\text{Si}} = 0.28$ . The interface between Cu and Si are assumed to be perfectly bonded.

To model plasticity in the Cu vias, we used a classical metal plasticity model in ABAQUS [11] with Mises yield surface and isotropic hardening in the FEA simulations. The yield stress was specified as a function of plastic strain:

$$\sigma_y(\bar{\varepsilon}_p) = \sigma_{y0} \left[ 1 + \frac{7E\bar{\varepsilon}_p}{3\sigma_{y0}} \right]^{1/n}. \quad (1)$$

where  $\sigma_{y0}$  is the initial yield strength,  $\bar{\varepsilon}_p$  is the equivalent plastic strain, and  $n$  is the hardening exponent. The initial yield strength  $\sigma_{y0}$  and the hardening exponent  $n$  were deduced using an iterative approach based on comparison between the FEA simulations and the nanoindentation experiments. For a given set of yield strength and hardening exponent, the indentation response of the TSV was simulated and compared to the force-displacement curve obtained from the experiment. The hardening exponent was fixed while adjusting the yield strength until the peak displacement was within 10% of the experiment value. The hardening exponent was then adjusted to achieve a better fitting to the experimental curve. This process was repeated until a reasonable fitting was obtained (see Fig. 3). The hardening exponent was found to be  $n = 9.5$  for both vias, while the initial yield strength was 250 MPa for TSV-A and 190 MPa for TSV-B. The lower yield strength for TSV-B is qualitatively consistent with the theoretical expectation based on the Hall-Petch relation, namely, the yield strength decreasing with increasing grain size due to the grain boundary strengthening mechanism.

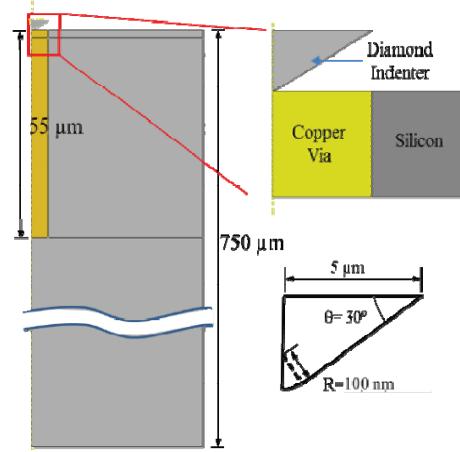


Fig. 5. An axisymmetric model for finite element simulations of nanoindentation using a cono-spherical diamond indenter.

#### IV. MEASUREMENT OF VIA EXTRUSION

For both types of TSVs, via extrusion and damage of the BEOL layers were observed. The extent of the via extrusion was measured at the via cross-section by high resolution scanning electron microscope (SEM), as shown in Figure 6. The average extrusion was 117 nm for TSV-A and 147 nm for TSV-B, showing the amount of via extrusion for TSV-B about 25%

larger than for TSV-A. A clear correlation appeared to exist between the average grain size of the Cu via and the amount of via extrusion (Fig. 6). For TSV-A which has smaller and more uniform grains, the amount of via extrusion is smaller than TSV-B. The difference can be traced to the different mechanical properties of Cu due to different grain structures resulting from different process conditions. Based on the observed correlation, TSVs with uniform small grains would be more favorable for reducing via extrusion.

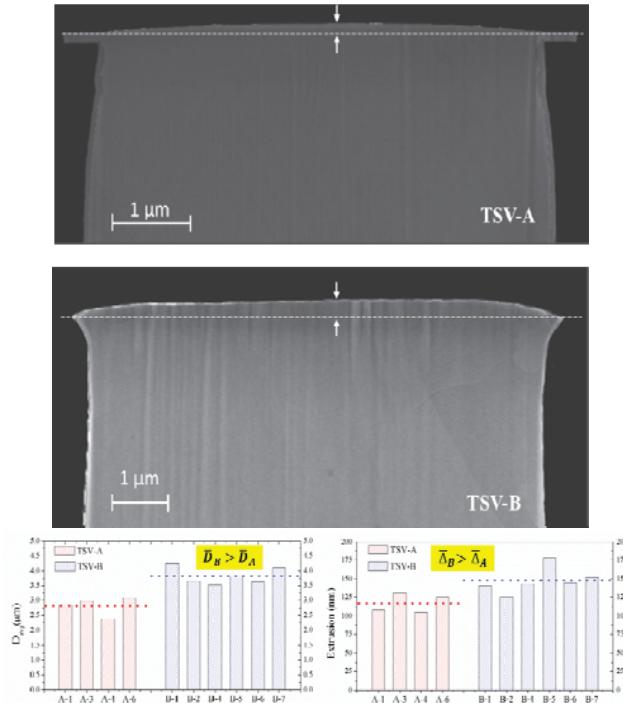


Fig. 6. SEM images of via extrusion (upper panel), and correlation between grain size and via extrusion for TSV-A and TSV-B.

## V. MODELING OF VIA EXTRUSION

To elucidate the effects of mechanical properties on via extrusion, a simple analytical model was formulated taking into account Cu Plasticity [7], followed by FEA simulations. Both the analytical model and FEA considered TSVs subject to a thermal cycle from the room temperature ( $T_R$ ) to a high process temperature ( $T_H$ ) and then back to the room temperature, with a thermal load  $\Delta T = T_H - T_R$ . First, assuming a free sliding interface, the mismatch of thermal expansion between the Cu via and Si induces a biaxial compressive stress in Cu upon heating:

$$\sigma_r = \sigma_\theta = -\Delta T (\alpha_{Cu} - \alpha_{Si}) \left( \frac{1-v_{Cu}}{E_{Cu}} + \frac{1+v_{Si}}{E_{Si}} \right)^{-1} \quad (2)$$

where  $\alpha_{Cu}$  and  $\alpha_{Si}$  are the coefficients of thermal expansion (CTEs) for Cu and Si, respectively. The stress induces an elastic strain in the axial direction of the via, which result in an elastic extrusion at the high temperature  $T_H$ :

$$\begin{aligned} \frac{\Delta H_e}{H} &= \epsilon_{z,Cu} - \epsilon_{z,Si} \\ &= \Delta T (\alpha_{Cu} - \alpha_{Si}) \left( 1 + \frac{2v_{Cu}}{E_{Cu}} \left( \frac{1-v_{Cu}}{E_{Cu}} + \frac{1+v_{Si}}{E_{Si}} \right)^{-1} \right) \end{aligned} \quad (3)$$

where  $H$  is the via height and  $\Delta H_e$  is elastic extrusion. The elastic extrusion increases linearly with temperature as,  $\Delta H_e = \beta_e H \Delta T$ , with  $\beta_e = 20.64 \text{ ppm}/^\circ\text{C}$  by using the typical values for the thermomechanical properties of Cu and Si ( $\alpha_{Cu} = 17 \text{ ppm}/^\circ\text{C}$ ,  $\alpha_{Si} = 2.3 \text{ ppm}/^\circ\text{C}$ ,  $E_{Cu} = 110 \text{ GPa}$ ,  $E_{Si} = 130 \text{ GPa}$ ,  $v_{Cu} = 0.35$ , and  $v_{Si} = 0.28$ ).

If no plastic yielding in Cu, the elastic via extrusion would decrease with the same rate upon cooling and vanish at the room temperature after a full thermal cycle. On the other hand, assuming perfect plasticity with a yield stress  $\sigma_y$  for the Cu via, plastic yielding of Cu is predicted when heating above a critical temperature

$$\Delta T_y = \frac{\sigma_y}{\alpha_{Cu} - \alpha_{Si}} \left( \frac{1-v_{Cu}}{E_{Cu}} + \frac{1+v_{Si}}{E_{Si}} \right) \quad (4)$$

which is proportional to the yield strength of Cu. Beyond the critical temperature ( $\Delta T > \Delta T_y$ ), the Cu via deforms plastically, resulting in a plastic extrusion [7]:

$$\frac{\Delta H_p}{H} = (3\alpha_{Cu} - 2\alpha_{Si})(\Delta T - \Delta T_y) \quad (5)$$

The plastic extrusion also increases linearly with temperature, but with a higher rate as,  $\Delta H_p = \beta_p H (\Delta T - \Delta T_y)$ , with  $\beta_p = 46.4 \text{ ppm}$ . The plastic extrusion rate is over twice of the elastic extrusion rate, leading to more significant via extrusion at the high temperature. More importantly, the plastic extrusion does not vanish after cooling, resulting in a non-zero residual extrusion after a full thermal cycle [7]:

$$\Delta H_r = H(\beta_p - \beta_e)(\Delta T - \Delta T_y) \quad (6)$$

Thus, the magnitude of the residual extrusion depends on the highest temperature during the thermal cycle and the plastic yield strength of the Cu via. Increasing the yield strength of Cu would increase the yield temperature  $\Delta T_y$  and thus decrease the residual extrusion for the same thermal load  $\Delta T$ .

Using the elastic-plastic properties extracted from the nanoindentation experiments, the magnitude of via extrusion versus the maximum process temperature are plotted in Figure 7 for both TSV-A and TSV-B. Since the yield strength is lower for TSV-B, the critical thermal load for via extrusion is lower. Subject to same thermal load ( $\Delta T > \Delta T_y$ ), the analytical model predicts that the amount of via extrusion for TSV-B is higher than TSV-A, consistent with the experimental observations (Fig. 6). Using the average extrusion measured for TSV-A and

TSV-B, we found that the corresponding thermal load is around  $350^{\circ}\text{C}$  for both TSVs, although the thermal load for TSV-B is slightly lower. The deduced thermal load is in reasonable agreement with typical process temperatures ( $\sim 400^{\circ}\text{C}$ ), although the exact thermal processes are not available for these TSV samples. Incidentally, the predicted via extrusion for TSV-B compare closely with reported data in a previous study [5].

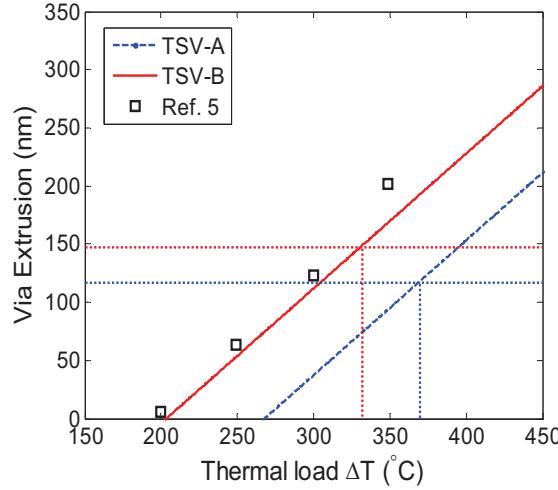


Fig. 7. Via extrusion versus maximum process temperature predicted by the analytical model, in comparison with experiments.

Next we used an axisymmetric FEA model similar to Figure 5 to simulate via extrusion during a thermal cycle, using the elastic-plastic properties extracted for TSV-A and TSV-B. As shown in Fig. 8, the numerical results are consistent with the predictions by the analytical model, where the residual via extrusion after the thermal cycle was higher for TSV-B than for TSV-A, both subject to the same thermal load  $\Delta T = 350^{\circ}\text{C}$ . It was found that the analytical model slightly overestimated the via extrusion due to the assumption of perfect plasticity (no strain hardening) and uniform stress field in the Cu vias.

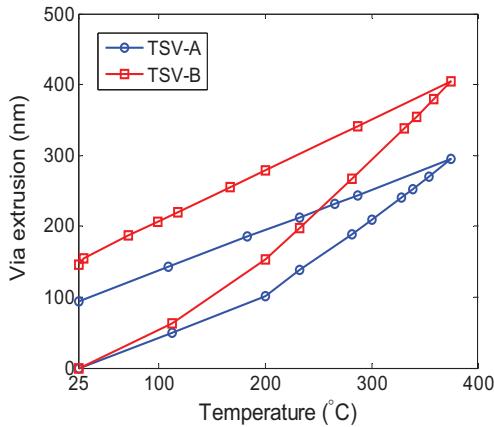


Fig. 8. Numerical simulations of via extrusion during a thermal cycle for TSV-A and TSV-B.

We further apply the FEA model to investigate the effect of interfacial properties on Cu extrusion. The development of via extrusion during a thermal cycle is evaluated for two cases with

different bonding behaviors and the results are shown in Figure 9 for comparison with the analytical model. First, a perfectly bonded interface is assumed between the copper via and silicon, for which the residual extrusion is significantly reduced, by  $\sim 3x$ , at room temperature. The results indicate that the contribution of plasticity to extrusion is reduced by the interfacial bonding between via and silicon. In the second case, a cohesive via/Si interface is assumed, which is represented by a bilinear traction-separation relationship with an adhesion energy of  $2.5 \text{ J/m}^2$  and a shear strength of  $50 \text{ MPa}$ . The via extrusions at both room and maximum temperatures are considerably higher than the bonded case although they are still lower than the analytical model. Hence, the via extrusion depends on both Cu plasticity and interfacial adhesion.

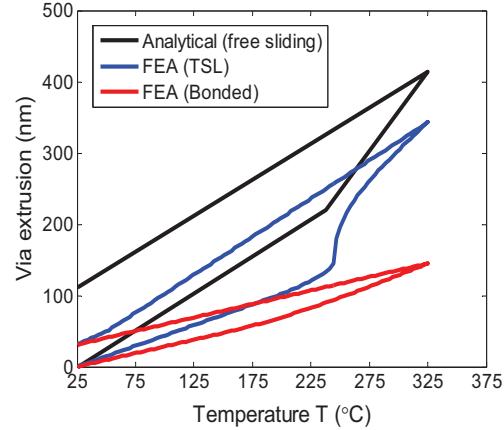


Fig. 9. Comparison of via extrusion calculated from the analytical model and FEA simulations with different interfacial properties: free sliding, perfect bonding, and cohesive with a bilinear traction-separation law (TSL).

## VI. CONCLUSIONS

In summary, the effect of the average grain size on the elastic-plastic properties of Cu TSV has been examined and correlated to via extrusion. The effect was investigated for two types of grain structures. It was found that smaller and more uniform grains resulted in higher yield strength and therefore is more favorable for reducing the via extrusion. The findings in this study suggest that in the fabrication of TSVs, it will be effective to control the processing parameters in order to achieve more uniform and small grains to improve via extrusion reliability.

## ACKNOWLEDGMENT

This work was supported by Semiconductor Research Corp.

## REFERENCES

- [1] I. De Wolf, K. Croes, O. V. Pedreira, R. Labie, A. Redolfi, M. Van De Peer, K. Vanstreels, C. Okoro, B. Vandeveldt, and E. Beyne, "Cu pumping in TSVs: Effect of pre-CMP thermal budget," *Microelectron. Reliab.* 51, 1856–1859 (2011).
- [2] A. Heryanto, W. N. Putra, A. Trigg, S. Gao, W. S. Kwon, F. X. Che, X. F. Ang, J. Wei, R. I Made, C. L. Gan, and K. L. Pey, "Effect of copper TSV

- annealing on via protrusion for TSV wafer fabrication,” J. Electron. Mater. 41 (9), 2533–2542 (2012).
- [3] S. Kang, S. Cho, K. Yun, S. Ji, K. Bae, W. Lee, E. Kim, J. Kim, J. Cho, H. Mun, and Y. L. Park, “TSV optimization for BEOL interconnection in logic process,” in Proc. IEEE Int. 3DIC, Osaka, Japan, Jan. 31/Feb. 2, 2012, pp. 1–4.
  - [4] S. K. Ryu, T. Jiang, K. H. Lu, J. Im, H.-Y. Son, K.-Y. Byun, R. Huang, and P. S. Ho, “Characterization of thermal stresses in through-silicon vias for three-dimensional interconnects by bending beam technique,” Appl. Phys. Lett. 100, 041901 (2012).
  - [5] D. Zhang, K. Hummler, L. Smith, and J.-Q. Lu, “Backside TSV protrusion induced by thermal shock and thermal cycling,” Proceedings of IEEE Electronic Components and Technology Conference (2013), pp. 1407–1413.
  - [6] T. Jiang, S. K. Ryu, Q. Zhao, J. Im, R. Huang, and P. S. Ho, “Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias,” Microelectron. Reliab. 53, 53–62 (2013).
  - [7] T. Jiang, C. Wu, L. Spinella, J. Im, N. Tamura, M. Kunz, H.-Y. Son, B.G. Kim, R. Huang, P.S. Ho, “Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects”, Appl. Phys. Lett. 103, 211906 (2013).
  - [8] S.-K. Ryu, T. Jiang, J. Im, P.S. Ho, R. Huang, “Thermo-mechanical failure analysis of through-silicon via interface using a shear-lag model with cohesive zone”, IEEE Trans. on Device and Materials Reliability 14, 318-326 (2014).
  - [9] W. C. Oliver and G. M. Pharr, “An improved technique for determining hardness and elastic modulus using load and displacement sensing indentation experiments”, J. Mater. Res. 7, 1564-1583 (1992).
  - [10] D. W. Gan, R. Huang, P.S. Ho, J. Leu, J. Maiz, T. Scherban, “Isothermal stress relaxation in electroplated Cu films. Part I: Mass transport measurements”, J. Applied Physics 97, 103531 (2005).
  - [11] ABAQUS Theory and Analysis User’s Manuals (Version 6.13), Dassault Systèmes Simulia Corp., Providence, RI, USA (2013).