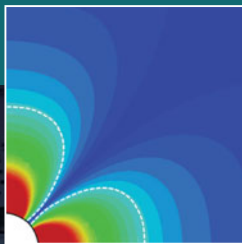

Through-silicon via stress characteristics and reliability impact on 3D integrated circuits

Tengfei Jiang, Jay Im, Rui Huang, and Paul S. Ho

Three-dimensional (3D) integration has emerged as a potential solution to the wiring limits imposed on chip performance, power dissipation, and packaging form factor beyond the 14 nm technology node. In 3D integrated circuits (ICs), the through-silicon via (TSV) is a critical element connecting die-to-die in the integrated stack structure. The thermal expansion mismatch between copper (Cu) vias and silicon (Si) can induce complex stresses in TSV structures to drive interfacial failure and Cu extrusion, degrading the performance and reliability of 3D interconnects. This article reviews current studies on thermal stresses and their effects on reliability of TSV structures. Recent results from measurements of stress and plasticity characteristics of Cu TSV structures are reviewed, including wafer curvature, micro-Raman spectroscopy, and synchrotron x-ray microdiffraction techniques. The effects of the Cu microstructure on stress and reliability, particularly on via extrusion and the device keep-out zone in TSV structures, are discussed. Based on the analysis of the reliability impact, we explore the potential of material and processing optimization to build reliable TSV structures for 3D ICs.

Introduction

As silicon technology continues to advance following Moore's Law, significant challenges in chip design, materials, and processes have emerged beyond the 14 nm technology node. This has led to important developments in technology, including the implementation of Cu/low-*k* interconnects (*k* is the dielectric constant), strained silicon technology, the multi-core processor, and the double gate field-effect transistor, such as the FinFET.[1–5] However, the limits imposed by the wiring delay from on-chip interconnects, power dissipation, and form factor remain key concerns for technology development based on conventional two-dimensional (2D) device integration. Beyond the 14 nm node, there are basic materials and processing issues, including an increase in Cu interconnect resistivity, damage from plasma processing, and the porosity limit for the ultralow-*k* dielectrics. While technology developments have continued, future technologies require further optimizations in design, materials, and processing to improve device density and chip performance. Concerns of cost increase in manufacturing and degradation in yield and reliability have already been reflected in a slower pace in recent advances of 2D integration.[6] This has generated great interest from the industry to develop three-dimensional integrated circuits (3D ICs) where dies are stacked vertically to reduce the wiring delay, power dissipation, and form factor of the integrated system. While the advantages of 3D integration have been recognized for more than a decade, active developments have occurred only in the past few years. This has largely been stimulated by the mobile communication industry where device form factor, power consumption, and manufacturing costs are key drivers for technology development.

In 3D integration, silicon dies are stacked vertically and through-silicon vias (TSVs) are used to provide short vertical interconnects to improve interconnect performance and system integration for 3D ICs.[7–10] The TSVs are critical elements for providing not only electrical interconnects, but also thermal and mechanical functionalities to support the 3D integration. Cu is widely used to form the TSV using a process compatible with the backend integration of Cu/low-*k* interconnects. The fabrication of the TSV structure involves deep etching of the

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Si wafer to form via holes, depositing the barrier and seed layers, and electroplating of Cu to fill the via holes.[11] Thermal stresses can arise during fabrication, testing, and operation of the TSV structures due to the large mismatch in the coefficient of thermal expansion between Cu and Si. The stresses can be large enough to cause serious reliability concerns and even structural failure in the integrated structure, including via extrusion, Si cracking near TSVs, and degradation of device performance.[12–16] Stress management and mitigation for TSV structures require basic understanding and characterization by measurements and modeling analyses. This is challenging but important for the development of 3D ICs since TSV geometry, material, and mechanical behaviors are distinctly different from the on-chip back-end-of-line (BEOL) wiring structures.

In this article, we review the thermal stress characteristics and the impacts on reliability of 3D integrated structures incorporating TSVs from materials and processing perspectives. We analyze the nature of thermal stresses for TSVs embedded in Si, with distinct characteristics near the wafer surface. The near-surface stresses are important for understanding the stress effect on the electrical performance of transistors, which are fabricated within a few micrometers from the surface. It is also important to understand how stresses can induce cracks near the surface, and local plastic deformation leads to structural failure of the Cu/Si interface. The microstructural evolution of the electroplated Cu in TSVs plays an important role in controlling its material properties and stress behavior.[17–19] This suggests a potential approach to improve TSV reliability by optimizing the grain structure and annealing process.

Experimental techniques have been developed to measure the stress behavior of TSV structures, including wafer curvature, micro-Raman spectroscopy, and synchrotron x-ray microdiffraction.[17–32] Each technique has certain limitations, but in combination and by correlating with the microstructural evolution, the results provide a basic understanding of the stress characteristics of TSV structures. Based on experimental results, micromechanics analyses have been performed to examine the mechanism and driving force for interfacial fracture and via extrusion.

Recently, via extrusion has been investigated for large TSV ensembles, and its distribution has been found to be statistical in nature, depending on the microstructure and fabrication processes.[33,34] An analytical model on via extrusion has been formulated to investigate the effects of grain structures and plasticity on via extrusion.[31,32] The implications for optimization of the grain structure and fabrication process to improve TSV reliability are discussed, as well as the stress effect on carrier mobility relating to device placement or the keep-out zone (KOZ), the area around the TSV where placement of active devices is to be avoided.

Stress characteristics and microstructure

Characteristics of near-surface stresses

The stress field for TSV structures is generally 3D in nature, depending on TSV geometry, array configuration, and wafer thickness. The effects of stresses near the wafer surface are of particular interest since most of the transistors are fabricated within a few micrometers from the wafer surface. A semi-analytic solution was deduced for the near-surface stress field of an isolated TSV embedded in the silicon wafer.[35] The contours of the stress components are shown in **Figure 1**, where the stress magnitude is normalized by a reference thermal stress $\sigma_T = -E\varepsilon_T/(1-\nu)$ with $\varepsilon_T = (\alpha_{Cu} - \alpha_{Si})\Delta T$, E = Young's modulus, ν = Poisson's ratio, α_{Cu} = coefficient of thermal expansion for Cu, α_{Si} = coefficient of thermal expansion for Si, and T = temperature. The normal (axial) stress σ_z is zero on the surface (z = 0) but non-uniform in the via (Figure 1a). The radial stress (σ_r) is non-zero on the surface (Figure 1b), whereas the shear stress (σ_{rz}) (Figure 1c) has a singular concentration at the junction between the surface and via/Si interface. Both the radial and shear stresses contribute to the driving force for interfacial delamination in mixed-mode fracture (opening and shearing).[35] Since the radial stress (σ_r) along the via/Si interface is tensile during cooling but compressive during heating, the fracture driving force is higher during cooling. The effect

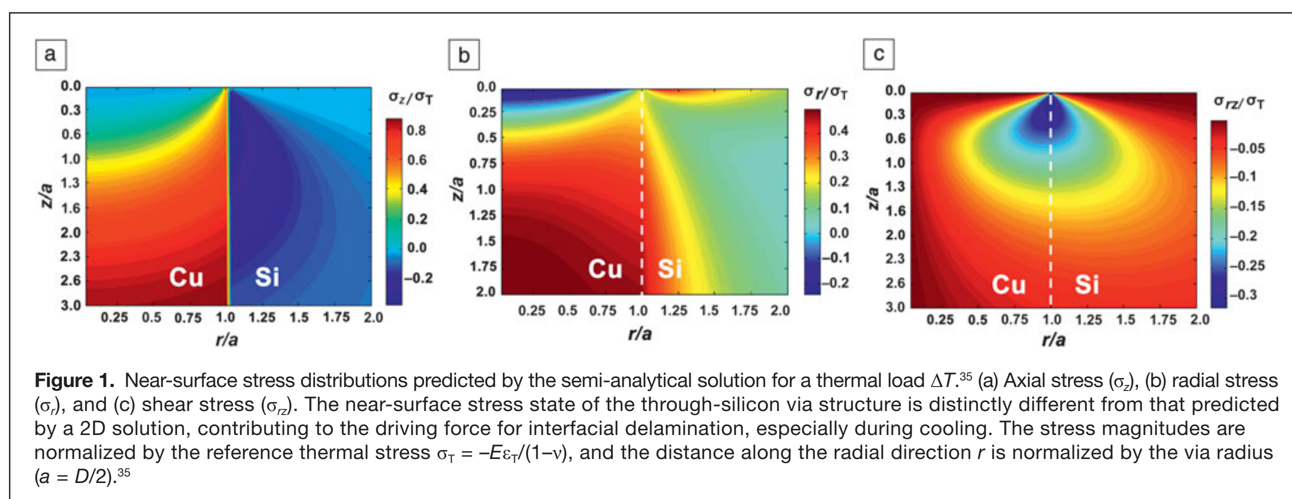

Figure 1. Near-surface stress distributions predicted by the semi-analytical solution for a thermal load ΔT.[35] (a) Axial stress (σ_z), (b) radial stress (σ_r), and (c) shear stress (σ_{rz}). The near-surface stress state of the through-silicon via structure is distinctly different from that predicted by a 2D solution, contributing to the driving force for interfacial delamination, especially during cooling. The stress magnitudes are normalized by the reference thermal stress $\sigma_T = -E\varepsilon_T/(1-\nu)$, and the distance along the radial direction r is normalized by the via radius ($a = D/2$).[35]

of the via depth to diameter ratio (aspect ratio) on stress characteristics was analyzed numerically.[35] Overall, the results are in good agreement with the analytical solution for a thick wafer with an aspect ratio of 10. But for a thin wafer with an aspect ratio of about 2, the stress magnitudes are lower, due to the close proximity of the two free surfaces. This suggests that reducing the aspect ratio can lower the driving force for interfacial delamination.

Detailed modeling analyses have been performed to investigate the effects of materials and processing on the stress characteristics of TSV structures, including studies on different TSV materials (e.g., Cu versus W), barrier layers (oxide/nitride versus polymers), and via configuration (annular versus full).[15,35] The energy release rate for interfacial delamination of TSV has been evaluated based on analytical solutions and finite element models. The results showed that the driving force for interfacial delamination under cooling is about twice that under heating as a result of the change of the radial stress at the interface from compression to tension under thermal cycling. The steady-state energy release rate for interfacial delamination was found to be linearly proportional to the via diameter and the square of the thermal mismatch strain between the via and Si. Therefore, the delamination driving force can be reduced by decreasing the TSV diameter and the thermal load or by using via materials with smaller thermal expansion mismatch with Si. For a Cu TSV of 10 µm diameter, the steady-state energy release rate is 6–7 J/m^2 under a cooling temperature of 250°C. This value is close to the adhesion energy of the Cu/Si and the Cu/oxide interface as well as the cohesive energy of Si.[36] Thus, interfacial delamination and Si cracking are possible failure mechanisms, which have indeed been observed in early 3D developments.[13,37] Recently, considerable advances have been made by optimization of TSV materials and processing to manage stress and reliability for 3D integration.[38,39]

Stress characterization and microstructure evolution

The stress analysis presented illustrates the 3D nature of stress characteristics in TSV structures where Cu was assumed to be elastically isotropic without considering the effects of grain structures. In electroplated Cu thin films, grain growth is commonly observed during annealing, where microstructure evolution plays an important role in controlling the stress and plasticity behavior.[40–44] The stress behavior of TSV structures was measured using wafer curvature, micro-Raman spectroscopy, and synchrotron x-ray microdiffraction techniques.[17–31] Typical results obtained by wafer curvature measurements are shown in **Figure 2**[19] for a TSV array fabricated by a via-middle process under thermal cycling, where TSVs are fabricated into a Si wafer after the transistors but prior to BEOL wiring structures. The 3D confinement by the Si substrate induces a triaxial stress state in the Cu vias, which is different from the biaxial stress state in electroplated Cu thin films where stress hysteresis loops are commonly observed under thermal cycling.[45] In contrast, the results in Figure 2 show no stress hysteresis for the TSV specimen, rather a nonlinear stress relaxation during heating, which was found to be largely due to grain growth in Cu vias. During cooling, with the Cu grain structure stabilized and a low effective shear stress associated with the triaxial stress state, nearly linear elastic behavior was observed for the TSV structure. When cycling to higher temperatures, similar behavior was observed with stress relaxation during heating followed by nearly linear elastic behavior during cooling. In this way, the residual stress after each thermal cycle continued to accumulate with increasing cycling temperature.

Stress relaxation during thermal processing is important in controlling the residual stress and thus via extrusion. For Cu at the TSV processing temperature, it can be attributed to a number of mechanisms, including grain growth, plasticity, and diffusional creep.[46] Grain growth in Cu TSVs was analyzed using electron backscatter diffraction, as shown in **Figure 3**a,[19] with each color corresponding to a specific grain orientation. Grain growth was observable as evidenced by the increase in the average grain size with increasing temperature (Figure 3b). A large fraction of Cu grains was observed to have a 60° misorientation angle after thermal cycling. This suggests that strain energy is important in driving grain evolution in the elastically anisotropic Cu grains with twin formation to facilitate the change from the (111) to the (200) orientation, a phenomenon also observed in electroplated Cu films.[47,48] Other test structures have been measured where grain growth was less dominant, particularly in samples that had been subjected to a high-temperature post-plating anneal, typically 20 min at 375°C to 420°C, to stabilize the grain structure.[19] Such samples exhibited nearly linear elastic behavior during thermal cycling without a significant increase in the residual stress.

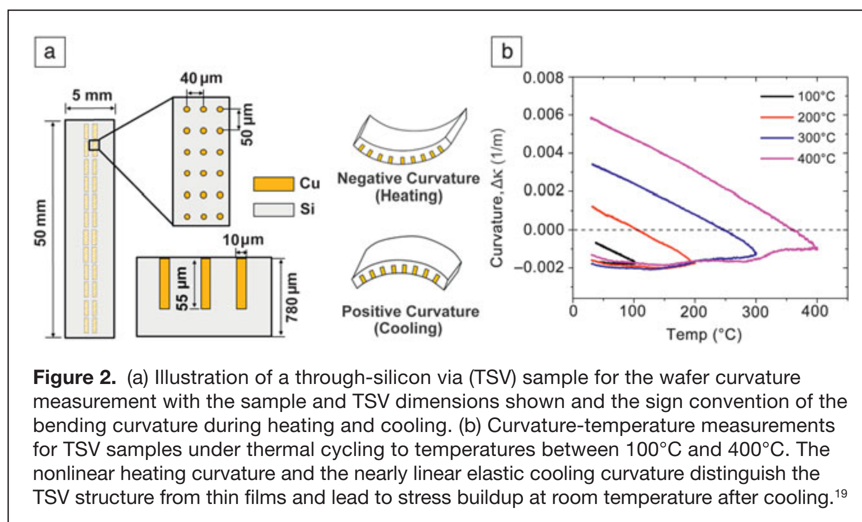

Figure 2. (a) Illustration of a through-silicon via (TSV) sample for the wafer curvature measurement with the sample and TSV dimensions shown and the sign convention of the bending curvature during heating and cooling. (b) Curvature-temperature measurements for TSV samples under thermal cycling to temperatures between 100°C and 400°C. The nonlinear heating curvature and the nearly linear elastic cooling curvature distinguish the TSV structure from thin films and lead to stress buildup at room temperature after cooling.[19]

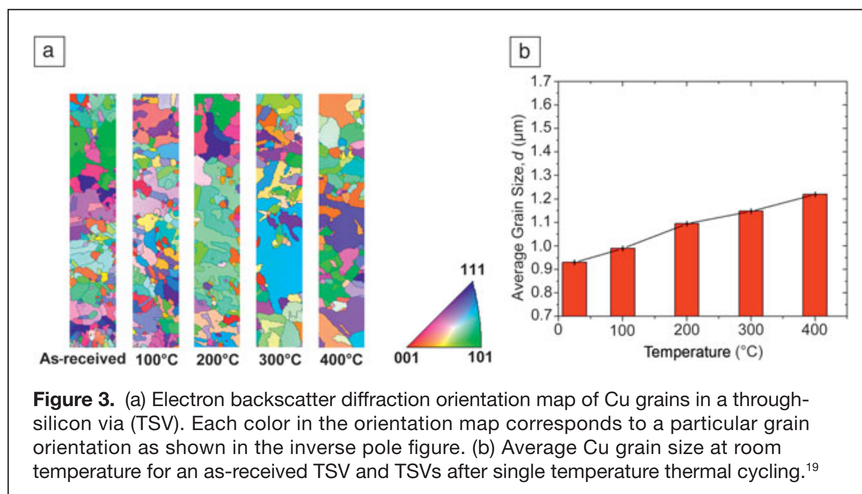

Figure 3. (a) Electron backscatter diffraction orientation map of Cu grains in a through-silicon via (TSV). Each color in the orientation map corresponds to a particular grain orientation as shown in the inverse pole figure. (b) Average Cu grain size at room temperature for an as-received TSV and TSVs after single temperature thermal cycling.[19]

Plastic deformation is important for stress relaxation in Cu films and was proposed as a major mechanism for via extrusion.[17,31,49,50] Although the wafer curvature measurements showed minimal plastic deformation in the volume average stress behavior, x-ray microdiffraction studies observed local plastic deformation in TSV structures.[31] This technique has the unique capability of measuring local strain in both Cu and Si with submicron resolution. In a synchrotron study, polychromatic (white beam) scans were conducted on the cross-section of TSVs with x-ray energies from 5 keV to 22 keV and a beam size of 1 μm. The results revealed asymmetric lattice bending of Si on either side of the Cu via, as measured by the relative change in the lattice orientation, Δφ (**Figure 4**a). The bending was induced by the near-surface stress and can be directly correlated to the residual stress in Si. For Cu, the shape of the Laue reflections showed an increase in the average peak width (APW), a measure of the local plasticity, observed in Cu grains near the via surface after thermal cycling to 300°C and 400°C. As seen in Figure 4b, the asymmetric broadening of the APW after thermal cycling to 400°C was concentrated near the top of the via, which can be attributed to an increase in the geometrically necessary dislocation density in Cu, indicating local plastic deformation.[29,31] The result provided direct evidence of local plasticity and was clearly observed after thermal cycling to 400°C, but was only faintly observable after thermal cycling to 200°C. This indicates that local plasticity occurred after thermal cycling to 400°C but not after thermal cycling to 200°C. In addition, the shape of the (024) reflection for a grain near the top of the via appeared to split into multiple peaks, as observed in 3D contours (Figure 4c). This indicates the formation of sub-grains as a result of local plastic deformation near the top surface of the via.[31]

Elastic-plastic finite element analysis (FEA) was performed to investigate the plastic deformation in the Cu via.[29] The von Mises stress as the effective shear stress for plastic deformation was found to be non-uniform in the Cu vias, reaching the yield strength only in a small region at the via/Si interface near the top surface. This indicates that plastic deformation in the Cu vias is highly localized, which is consistent with the x-ray microdiffraction results. In general, grain growth could lead to lower yield strength due to the Hall–Petch effect, namely, the yield strength decreases with increasing grain size due to the grain boundary strengthening mechanism, which in turn would cause more plastic deformation and Cu extrusion. Thus, a high-temperature post-plating anneal can stabilize the grain structure to limit via extrusion during subsequent thermal processing.[31,32,50,51] It is important, therefore, to obtain the desired grain structure by optimizing the electroplating chemistry and annealing process in order to minimize via extrusion, as discussed later in the text.

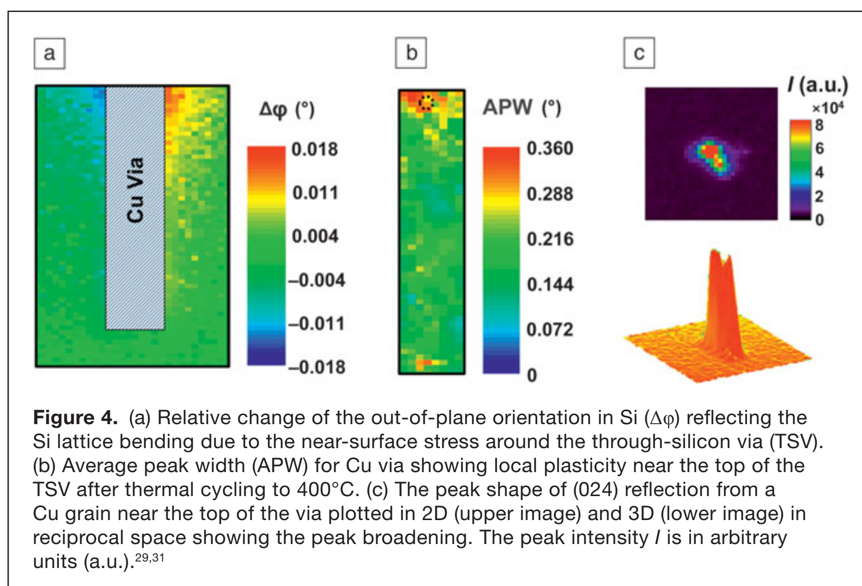

Figure 4. (a) Relative change of the out-of-plane orientation in Si (Δφ) reflecting the Si lattice bending due to the near-surface stress around the through-silicon via (TSV). (b) Average peak width (APW) for Cu via showing local plasticity near the top of the TSV after thermal cycling to 400°C. (c) The peak shape of (024) reflection from a Cu grain near the top of the via plotted in 2D (upper image) and 3D (lower image) in reciprocal space showing the peak broadening. The peak intensity *I* is in arbitrary units (a.u.).[29,31]

Via extrusion

Via extrusion has been a major concern for the yield and reliability of 3D integration. It manifests the non-recoverable plastic deformation near the top of the via during thermal cycles. In a recent study, via extrusion was observed with atomic force microscopy and was found to increase with maximum temperature in thermal cycles.[31] The rough surface profile suggested microscopically stochastic behavior (**Figure 5**a), which was found to follow the grain structure near the surface of the via, possibly due to grain boundary sliding. In a separate study,[33] via extrusion, or Cu pumping was investigated as a function of the process temperature and for two via sizes of 5 μm × 50 μm (diameter × depth) and 10 μm × 100 μm (diameter × depth).

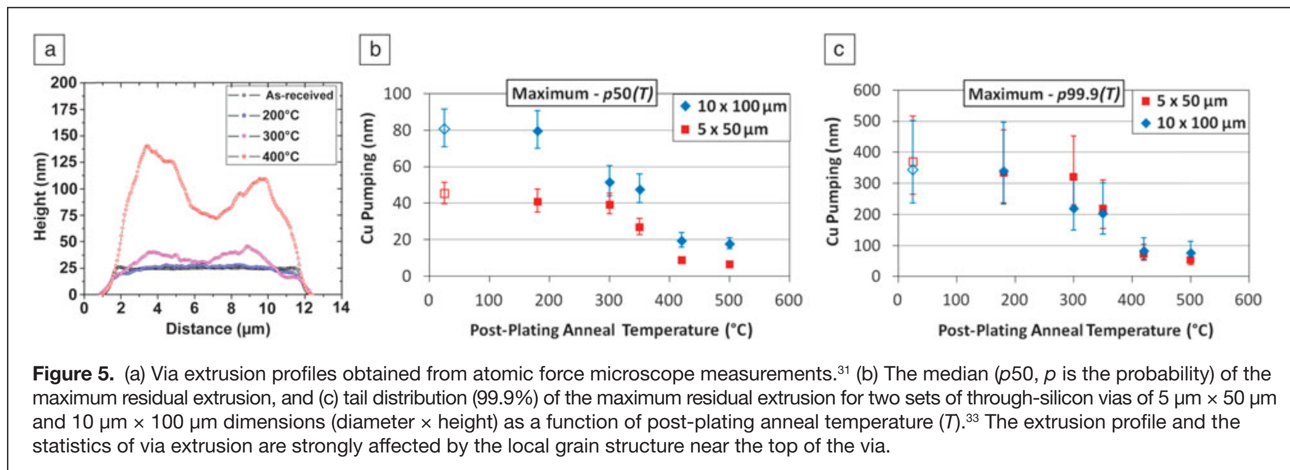

Figure 5. (a) Via extrusion profiles obtained from atomic force microscope measurements.[31] (b) The median (*p*50, *p* is the probability) of the maximum residual extrusion, and (c) tail distribution (99.9%) of the maximum residual extrusion for two sets of through-silicon vias of 5 μm × 50 μm and 10 μm × 100 μm dimensions (diameter × height) as a function of post-plating anneal temperature (T).[33] The extrusion profile and the statistics of via extrusion are strongly affected by the local grain structure near the top of the via.

Large ensembles of vias were used to measure the stochastic behavior and search for an optimal post-plating anneal. Via extrusions were found to follow a lognormal distribution, where the median (*p*50, *p* is the probability) of the maximum via extrusion for the smaller TSVs measured by white light interferometry was about half of that for larger TSVs (Figure 5b). However, the largest extrusions at 99.9% of the lognormal distribution were found to be about the same for both sets of TSVs except at 300°C, independent of via size and post-plating anneal conditions (Figure 5c).

These results indicate that TSV reliability did not improve by reducing via diameter, since the reliability of 3D devices containing a large number of TSVs is determined by the largest extrusions (i.e., the weakest link) in spite of their small percentage (about 0.1%) of occurrence. In a subsequent study, the statistical spread in via extrusion correlated to the grain size and orientation near the top of the vias for two sets of vias fabricated using different electroplating chemistries.[34] The smallest 20% via extrusion seemed to be dominated by (111) grains with large grain (1/3 of the via diameter or larger) size, while the largest 20% extrusion was dominated by (200) and (110) grains with small grain size (1/4 of the via diameter or smaller). For vias containing three grains or more at the top surface, via extrusion was about twice that of vias containing only one large grain (not counting twin boundaries). The results suggest that a single grain at the top of the via would be effective in mitigating via extrusion, which was found to reduce the via extrusion substantially.[34] However, it is unclear how to fabricate such grain structures for all TSVs to completely eliminate the tail of the distribution representing the largest extrusions.

The effect of grain structures on via extrusion was examined recently by experiments and modeling. TSV samples 5.5 μm in diameter and 55 μm in depth were fabricated using different via middle processes to yield different grain structures.[32] The two types of vias were found to have random grain orientations but different average grain sizes: 2.83 μm for small grain (SG) TSVs versus 3.82 μm for large grain (LG) TSVs. Nanoindentation measurements were carried out to measure the elastic and plastic properties of the Cu vias. A classical metal plasticity model was used in FEA simulations to compare with experiments, based on which the yield strength was found to be 250 MPa for SG TSVs and 190 MPa for LG TSVs. The lower yield strength for LG TSVs is consistent with the Hall–Petch relation. For both types of TSVs, via extrusion and damage of the BEOL layers were observed. The average via extrusion was 117 nm for SG TSVs and 147 nm for LG TSVs, indicating a correlation between the average grain size and the amount of via extrusion. These results suggest that TSVs with uniform SGs would be more favorable for reducing the average via extrusion, but not necessarily for improving the statistical distribution of the largest extrusion.

Interfacial sliding and Cu plasticity have been suggested as two possible mechanisms for via extrusion.[31,34,52] Interfacial delamination and subsequent sliding could result in via extrusion at high temperatures but very little extrusion after cooling back to room temperature if no plastic deformation exists in the Cu via. On the other hand, even without interfacial delamination, via extrusion was observed after thermal cycling,[17] which was attributed to local plastic deformation. To elucidate the effects of Cu plasticity on via extrusion, a simple analytical model was formulated by assuming perfect plasticity in Cu and frictionless interfacial sliding.[31] When the TSV is subjected to a thermal cycle from room temperature (T_R) to a high process temperature (T_H) and then back to room temperature with a thermal load $\Delta T = T_H - T_R$, the mismatch of thermal expansion between the Cu via and Si induces a compressive stress in Cu upon heating. Assuming perfect plasticity with a yield strength σ_y for the Cu via, plastic yielding of Cu is predicted when heated above a critical temperature,

$$\Delta T_y = \frac{\sigma_y}{\alpha_{Cu} - \alpha_{Si}} \left(\frac{1 - \nu_{Cu}}{E_{Cu}} + \frac{1 + \nu_{Si}}{E_{Si}} \right), \tag{1}$$

which is proportional to the yield strength of Cu. Beyond the critical temperature ($\Delta T > \Delta T_y$), the Cu via deforms plastically, leading to more via extrusion at higher temperatures.

The plastic extrusion does not vanish after cooling, resulting in a non-zero residual extrusion after a full thermal cycle:[31]

$$\Delta H_r = H(\beta_p - \beta_e)(\Delta T - \Delta T_y), \tag{2}$$

where H is the via height, β_e = 20.64 ppm/°C and β_p = 46.4 ppm/°C are the elastic and plastic extrusion rates, respectively, by using the typical thermomechanical properties of Cu and Si (α_{Cu} = 17 ppm/°C, α_{Si} = 2.3 ppm/°C, E_{Cu} = 110 GPa, E_{Si} = 130 GPa, ν_{Cu} = 0.35, and ν_{Si} = 0.28). Thus, the magnitude of the residual extrusion depends on the highest temperature during thermal cycling and the plastic yield strength of the Cu via. Increasing the yield strength of Cu would increase the yield temperature ΔT_y and thus decrease the residual extrusion for the same thermal load. This is qualitatively consistent with the experimental measurements.[32]

The magnitude of residual via extrusion predicted by the analytical model is plotted in **Figure 6**a as a function of the maximum process temperature. Using the average extrusion measured for SG and LG vias, it was found that the corresponding thermal load is around 350°C for both TSVs (red and blue solid lines). The deduced thermal load is in reasonable agreement with typical process temperatures (~400°C), and the predicted via extrusion for the LG vias also compares closely with data reported in an independent study.[53] Using the elastic-plastic properties obtained from nanoindentation measurements for the SG and LG vias,[32] the via extrusion behavior was deduced by FEA simulation during thermal cycle (Figure 6b). The numerical results were consistent with the predictions by the analytical model, where the residual via extrusion after the thermal cycle was higher for the LG via than for the SG via, both subject to the same thermal load ΔT = 350°C. The effect of grain structure is taken into account in this model only through the average elastic-plastic properties of the Cu vias.

The effects of interfacial properties and via dimensions on via extrusion have been studied by numerical simulations using FEA models.[31,52] On the effect of interfacial properties, assuming a perfectly bonded interface between the Cu via and Si, the residual extrusion at room temperature was significantly reduced, by ~3x. On the other hand, using a cohesive model for the via/Si interface, the via extrusions at both room and maximum temperatures were found to be bound by two limits, frictionless sliding in the analytical model as the upper bound and a perfectly bonded interface (no sliding) as the lower bound. Hence, via extrusion can be suppressed by improving the interfacial adhesion to resist sliding. On the effect of via dimensions, the results show a general trend of decreasing extrusion with smaller via diameter and depth. This is in general agreement with recent experimental studies where average via extrusion was found to decrease with via dimensions.[13,33] However, it is not clear that TSV reliability would improve with a smaller via diameter since an open question about the extrusion statistics remains: how the probability of the largest extrusion, or the weakest link, in determining the TSV reliability would change with decreasing via dimensions.

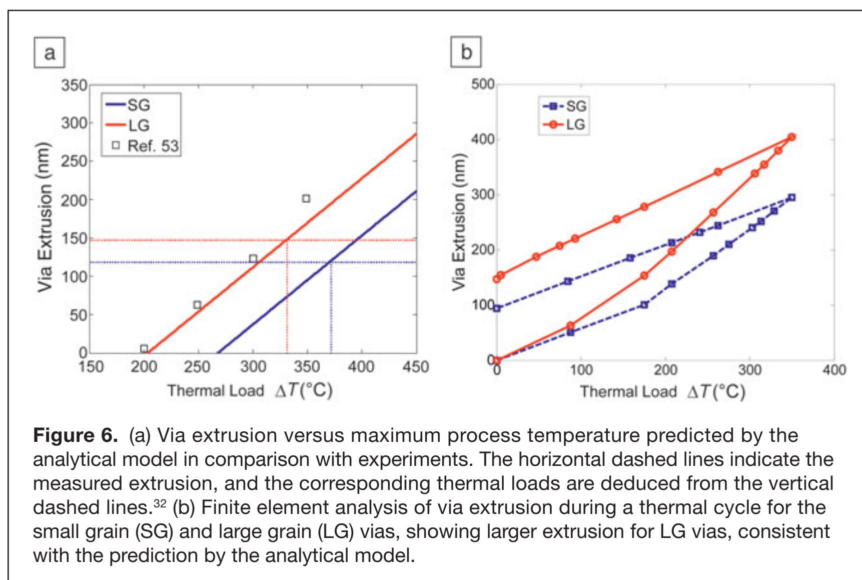

Figure 6. (a) Via extrusion versus maximum process temperature predicted by the analytical model in comparison with experiments. The horizontal dashed lines indicate the measured extrusion, and the corresponding thermal loads are deduced from the vertical dashed lines.[32] (b) Finite element analysis of via extrusion during a thermal cycle for the small grain (SG) and large grain (LG) vias, showing larger extrusion for LG vias, consistent with the prediction by the analytical model.

Keep-out zone

Within the keep-away zone,[54,55] or KOZ,[56–58] a significant level of TSV-induced stresses can be present, which would affect the device performance by degrading the carrier mobility if devices are placed there. Near-surface stresses in Si around the vias have been observed by micro-Raman spectroscopy.[21–25] Degradation of carrier mobility is induced by the piezoresistivity effect, which was analyzed by taking into account the anisotropic elastic properties of Si.[16,59]

The piezoresistivity effect was analyzed for a simple structural model consisting of a single TSV 10 μm in diameter and 200 μm in height surrounded by an infinite Si matrix subject to a thermal load, ΔT = –250°C. The calculated mobility changes are plotted in **Figure 7**a–b for the electric field and current density in the direction of [100] and [110], respectively. The dashed lines in the figures are the KOZ boundaries defined by 5% change in mobility, and they are highly directional. For the channels lined along [100], a sizable KOZ developed in the *n*-type silicon (Figure 7a), but no KOZ existed in the *p*-type (not shown). In contrast, for the channel lined along the [110] direction, the *p*-type silicon has a sizable KOZ (Figure 7b) but no KOZ for the *n*-type (not shown).

Further analyses were performed as a function of TSV diameter and Cu yield strength.[16] The KOZ was found to increase monotonically with TSV diameter. With respect to Cu yield strength, the KOZ initially increased with increasing yield strength and then remained constant with a further increase in yield strength. This is consistent with the synchrotron observation of localized yielding and plastic deformation at the via/Si interface near the top surface,[17] which can effectively relax the local

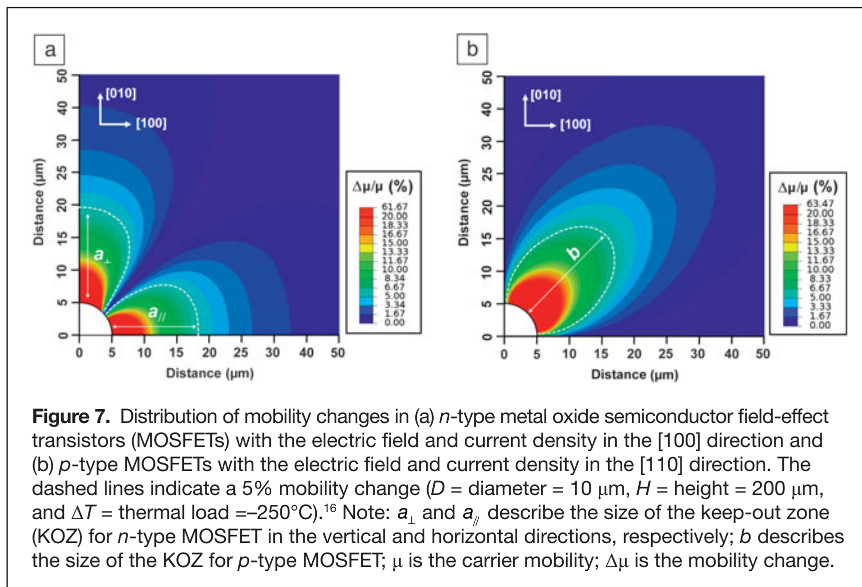

Figure 7. Distribution of mobility changes in (a) *n*-type metal oxide semiconductor field-effect transistors (MOSFETs) with the electric field and current density in the [100] direction and (b) *p*-type MOSFETs with the electric field and current density in the [110] direction. The dashed lines indicate a 5% mobility change (D = diameter = 10 μm, H = height = 200 μm, and ΔT = thermal load =–250°C).[16] Note: $a_{\perp}$ and $a_{//}$ describe the size of the keep-out zone (KOZ) for *n*-type MOSFET in the vertical and horizontal directions, respectively; b describes the size of the KOZ for *p*-type MOSFET; μ is the carrier mobility; Δμ is the mobility change.

stresses to reduce the mobility change. With increasing yielding strength, the TSV could remain elastic under a thermal load of –250°C, and thus the size and shape of the KOZ would not change. When the TSVs are placed closer together, the stresses in one via can interact with those of the neighbors, increasing the overall stresses in Si and the size of the KOZ. However, the effect is found to be negligible if the ratio of via pitch to diameter is greater than five.[16]

Various groups have performed electrical testing to determine the KOZ of devices for technology nodes ranging from 130 to 28 nm.[57,58,60–62] The results have been tabulated by Weerasekera et al.[60] and are shown in **Table I**. For TSVs with diameters ranging from 5 to 10 μm, the KOZ was 4 μm or less, and the change in saturation current, ΔI_{on}, was 4% and below–within the specified limit of device saturation current for 65 nm technology–for both *n*-type and *p*-type MOS devices.

The size of the KOZ from these electrical measurements turned out to be lower than that predicted by FEA for via diameters of 10 μm or below (Figure 7). The difference may be traced to the materials database used in the FEA and could be reduced if more accurate material properties were available.

On the processing side, most of the processing details can be incorporated into FEA to provide a better estimate of the KOZ and for processing optimization. Rabie et al. utilized the stacks consisting of a nitride, a pre-metal dielectric oxide, and a contact protection layer to achieve a "near-zero" KOZ.[63] Takeda and Aoki[64] evaluated TSVs with a 7 μm diameter and found a KOZ of about 2 μm based on their electrical failure criterion of a 1% change in the frequency of the ring oscillator. They attributed the reduction of KOZ to wafer thinning after bonding and hybrid wafer bonding in a via-last process, where via processing was done last after the processing of the BEOL wiring structures. Kino et al.[65] constructed a thinned chip on a substrate consisting of metal microbumps with an adhesive and used a capacitance-voltage method to measure the electron mobility. By switching from a high temperature cure to a low temperature cure adhesive, they were able to reduce the electron mobility change from 13.4% to 0.14%. Overall, considerable advances have been made recently by the industry to reduce the KOZ.

Summary and future outlook

The development of 3D integration has stimulated great interest in the study of thermal stresses and their impact on TSV reliability. Experimental techniques have been developed to measure the complex stress behavior of TSVs, particularly for stresses near the via surface. This was accompanied by the use of analytical solutions and numerical simulations to analyze the results from experiments. Together these studies have significantly advanced our understanding of the stress characteristics and reliability mechanisms of TSV structures, particularly when correlated with the microstructure of Cu TSVs. The microstructural evolution of Cu was found to be important in controlling the residual stress and local plastic deformation accumulated during thermal cycling, which can directly impact via extrusion and BEOL reliability. Results of such studies have led to guidelines and potential approaches for stress management to improve TSV reliability.

Table I. Maximum change in saturation current, I_{on}, for different technologies.[60]

Ref.	Technology (nm)	TSV D (μm)	KOZ (μm)	% $\|\Delta I_{on}/I_{on}\|$	
				NMOS	PMOS
Yang et al.[57]	130	5.2	1.1	0.0	0.0
Beyne[61]	65	5	1.7	0.6	4.0
Weerasekera et al.[60]	65	8	1.2	4.0	4.0
Cho et al.[58]	45	6	2	2.0	2.0
West et al.[62]	28	10	4	2.3	2.3

Note: D, diameter; KOZ, keep-out zone; NMOS, *n*-type metal oxide semiconductor field-effect transistors; PMOS, *p*-type metal oxide semiconductor field-effect transistors; ΔI_{on}, change in saturation current.

Looking ahead, the implementation of 3D integration is imminent, which will motivate further materials and processing optimization to improve the yield and reliability as the scaling of TSVs continues with further chip-level integration. As scaling increases the number of vias in 3D ICs, the statistics of via extrusion seem to emerge as

a significant issue, where the tail distribution of the largest extrusions would be important in determining BEOL reliability. Recent studies show that although the average via extrusion decreases with smaller via diameter, the portion of the largest extrusions would not substantially change. This suggests that via extrusion will remain an important reliability issue as TSV dimensions continue to decrease. The statistics and the mechanism of the largest via extrusions will have to be better understood together with their impact on the electrical and structural integrity of TSV structures for development of reliable 3D ICs.

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