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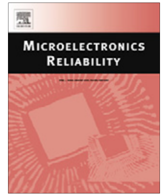

Measurement and analysis of thermal stresses in 3D integrated structures containing through-silicon-vias

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ABSTRACT

Three-dimensional (3-D) integration with through-silicon-vias (TSVs) has emerged as an effective approach to overcome the wiring limit beyond the 32 nm technology node. Due to the mismatch of thermal expansion between the via material and Si, thermal stresses ubiquitously exist in the integrated 3-D structures. The thermal stresses can be significant to raise serious reliability issues, such as TSV extrusion and mobility degradation of logic devices. To understand the characteristics of the thermal stresses in TSVs, experimental measurements and numerical analysis are presented in this work. A precision wafer curvature technique was used together with micro-Raman spectroscopy to form a complementary approach to characterize the deformation and stresses in the TSV structures. The microstructures of the Cu vias were analyzed to provide insights to the deformation mechanisms. Guided by the experimental observations, finite element analysis was performed to analyze the thermal stresses taking into account the elastic anisotropy of Si and the plasticity of Cu. It was found that plastic deformation is localized within the Cu vias near the via/Si interface and may play an important role in TSV extrusion. Finally, the effect of thermal stresses on carrier mobility was investigated to evaluate the keep-out zone (KOZ) for logic devices near the TSVs.

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1. Introduction

Through-silicon-via (TSV) is a key element for 3-D integration in providing vertical interconnects for chip-stacking structures. By using short vertical interconnects in 3-D integration to replace the long interconnects needed in 2-D integration, better electrical performance and lower power consumption can be achieved [1,2]. Cu is widely used as the via filling material because Cu is compatible with the back-end of line (BEOL) processes along with appropriate electrical and mechanical properties. However, the mismatch in the coefficients of thermal expansions (CTEs) between Cu and Si is relatively large, which can induce substantial thermal stresses in the TSV structures. The stresses may arise during fabrication, testing and operation of the TSV structures, leading to various reliability issues, such as crack growth, TSV extrusion, and degradation of device performance [3–5]. Therefore, characterizing the thermal stresses in the TSV structures is important for successful implementation of 3-D integration.

In this work, the thermal stresses in TSV structures are studied by experimental and numerical methods. First, the precision wafer curvature technique is used to determine the thermal stresses by measuring the curvature change of the TSV specimen during thermal cycling. The stress behavior is correlated to changes in the microstructures of the Cu vias subjected to thermal treatments which are analyzed by focused ion beam (FIB) and electron backscatter diffraction (EBSD) techniques. Along with the microstructure analysis, the mechanisms underlying the linear and nonlinear temperature–curvature behavior of the TSV specimen are discussed. As a global measurement, the curvature change reflects the overall effect of the thermal stresses. This is supplemented by measurement of the local stress distribution near the surface of the Si wafer around the Cu vias using micro-Raman spectroscopy. The stresses deduced from Raman spectroscopy are compared with the thermomechanical finite element analysis (FEA) and found in good agreement. Here the effect of Cu plasticity is a significant factor in controlling the thermal stresses and via extrusion and will be discussed. Finally, the stress analysis is extended to study the effect on carrier mobility and keep-out zone (KOZ) for logic devices near the TSVs, which is important for design and reliability of 3D integrated circuits.

2. Stress measurement and microstructure analysis

2.1. Precision wafer curvature technique

2.1.1. Measurement system and TSV specimen

The precision wafer curvature technique is an extension of the wafer curvature technique that has been used extensively for

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stress measurement in thin films and periodic line structures [6–8]. The precision wafer curvature measurement system is set up based on an optical lever with a capability to measure the curvature ($1/R$) to a precision of $6.5 \times 10^{-5}\ m^{-1}$. As shown schematically in Fig. 1a, the two incident laser beams are reflected by the specimen and the movement of the reflected laser spots is tracked by two position-sensitive photodetectors. The measurement system is designed with a heating stage inside a vacuum chamber. Therefore, the curvature change of the TSV specimen during thermal cycling can be measured *in situ* under a controlled atmosphere. More details of the system have been presented elsewhere [9].

The TSV specimen used in the present study contained periodic arrays of blind Cu vias, where the Cu is deposited by electroplating. The vias were 10 μm in diameter with a nominal depth of 55 μm. The silicon wafer was 700 μm thick and was of (001) type. The spacing between the TSVs was 40 μm along the [110] direction and 50 μm along the $[1\bar{1}0]$ direction (Fig. 1b). For the curvature measurement, the wafer was cut into 5 × 50 mm beams where the TSVs were located along the centerline of the specimen (Fig. 1c). There was a Ta barrier metal layer of 0.1 μm thick and an oxide barrier layer with a nominal thickness of 0.4 μm at the via/Si interface. On the surface of the wafer, there was an oxide layer of 0.8 μm thick. The surface oxide layer was mechanically removed for all measurements discussed in this work.

2.1.2. Thermal cycling experiment

The curvature measurements were conducted for several fully-filled TSV specimens subjected to thermal cycling. Due to the residual stress resulting from the fabrication process, an initial curvature was developed in the specimen. To determine the residual stress in the Cu vias, a reference specimen was used by etching off the Cu vias. The curvature of the reference specimen was measured over the same thermal cycle as the specimen with fully filled Cu vias, and the curvature difference between the two specimens is attributed to the average thermal stress in the Cu vias. As shown in Fig. 2a, the curvature decreases nonlinearly with increasing temperature during the first cycle, suggesting an average compressive stress in the Cu vias and inelastic deformation. During cooling, however, the curvature changes linearly with the temperature, suggesting predominantly linear elastic deformation. In particular, the curvature difference between the two specimens becomes zero at around 100 °C, suggesting a zero average stress in the Cu vias at this temperature. Below 100 °C, the curvature becomes positive, and the average stress in the Cu vias becomes tensile. The temperature of zero curvature (∼100 °C) is consistent with the annealing temperature during fabrication for the as-received TSV specimen and is taken as the reference temperature for the thermal stress analysis.

In the first measurement (Fig. 2a), sample A went through three thermal cycles to 200 °C at a heating rate of 2 °C/min. After the first thermal cycle, the curvature–temperature relation became nearly linear and was reversible up to 200 °C. The residual curvature at room temperature increased slightly after each cycle. In the second measurement (Fig. 2b), sample B was heated to 200 °C in the first two cycles, and then heated to 300 °C during the third cycle and annealed for 1 h prior to cooling, followed by an additional cycle to 300 °C. For the first two cycles, the curvature behavior of sample B is similar to sample A. However, when the temperature was increased beyond 200 °C during the third cycle, a nonlinear curvature–temperature behavior similar to the first cycle was observed from 200 °C to 300 °C. During annealing at 300 °C, the curvature decreased to almost zero. Evidently, the average stress in the Cu vias was relaxed considerably during annealing at 300 °C. Subsequently, during cooling and the last thermal cycle, the curvature–temperature behavior again became nearly linear and reversible up to 300 °C. Compared to sample A, the residual curvature of sample B after the four thermal cycles is much larger, suggesting a higher tensile stress in the vias for sample B. This is attributed to the annealing process that reset the reference temperature with zero curvature to 300 °C. Therefore, depending on the thermal history, different thermal load (ΔT) has to be used for the thermal stress analysis. For sample A (Fig. 2a), the reference temperature is 100 °C, and the thermal load $\Delta T_A = -70$ °C at the room temperature (∼30 °C). For sample B (Fig. 2b), the reference temperature is 300 °C, and the thermal load $\Delta T_B = -270$ °C after the thermal cycles. The reference temperatures determined here were used in finite element analyses in comparison with micro-Raman measurements, as discussed further in Section 2.4.

The measured curvature–temperature behavior can be related to the average effects of thermal stresses and deformation mechanisms of the TSV specimen. The negative curvature indicates an average compressive stress in the Cu vias, while the positive curvature implies tensile stress. The nonlinear curvature–temperature behavior observed during the heating process of the first cycle suggests an inelastic deformation mechanism, which was found to be related to the evolution of the Cu grain structures, as discussed in Section 2.2 along with microstructure analysis. On the other hand, the nearly linear curvature–temperature behavior in the subsequent thermal cycles indicates predominantly linear elastic behavior of the Cu vias, which is in sharp contrast with the thermomechanical behavior of Cu thin films as discussed in Section 3.1. In Section 2.3, the micro-Raman technique was used to measure the local stress distribution in Si near the TSVs with similar test structures subjected to the same thermal loads as in the curvature

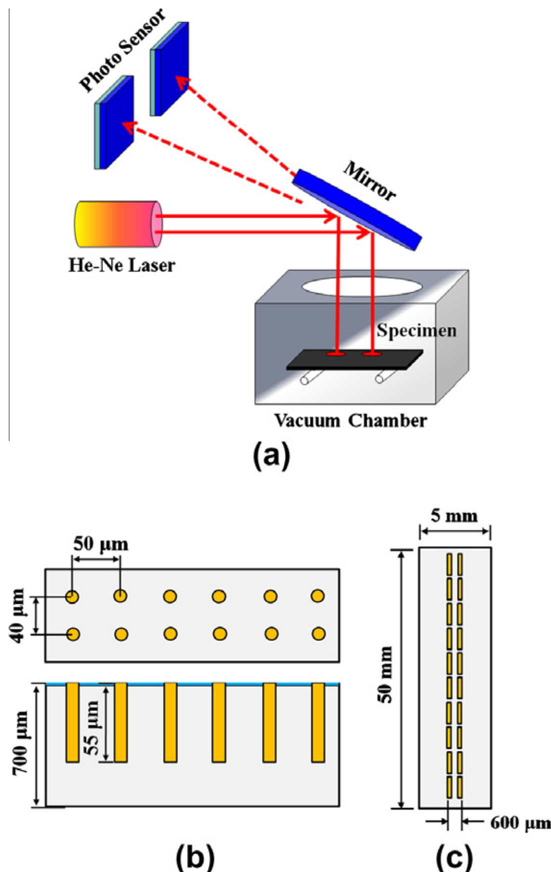


Fig. 1. (a) Illustration of the precision wafer curvature measurement system. (b) Illustration of the TSV specimen, top and side views with the dimensions. (c) Top view of the TSV specimen for the curvature measurements, with TSV arrays in many blocks along the center line.

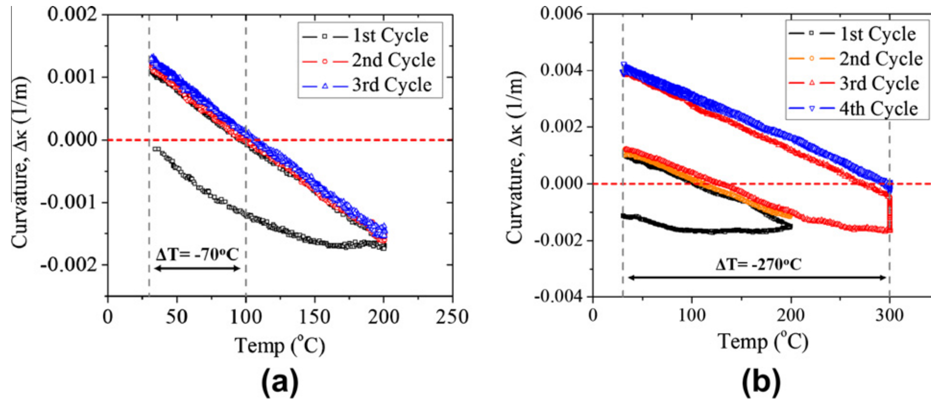


Fig. 2. Curvature measurements for (a) a TSV specimen subjected to thermal cycling to 200 °C; (b) a TSV specimen subjected to four thermal cycles with an annealing step at 300 °C for 1 h.

measurements. In this way, the results from the two measurements can be correlated to provide a more complete description of the stress characteristics in the TSV structures by combining the global and local effects.

2.2. Microstructure analysis

To further understand the deformation mechanism underlying the measured curvature–temperature behavior of the TSV specimens, microstructure evolution of the Cu vias subjected to different thermal histories was studied. A number of TSV specimens were each subjected to a single thermal cycle to different temperatures, and the measured curvatures are shown in Fig. 3. Despite the different highest temperatures ranging from 100 °C to 400 °C, similar behavior was observed for all specimens: a nonlinear curvature–temperature relation during heating followed by a nearly linear relation during cooling.

Using focused ion beam (FIB), the cross-sections of the TSV specimens were examined after completing the thermal cycling measurements. The contrast of the ion channeling images of the Cu vias in Fig. 4a shows that the average Cu grain sizes are larger after thermal cycles and increase as the highest temperature of thermal cycling increases, suggesting possible grain growth during the thermal cycles. This is confirmed by electron backscatter diffraction (EBSD) analysis of the grain structures. The EBSD grain mappings for the Cu vias are shown in Fig. 4b together with the average grain sizes measured and compared in Fig. 4c. Evidently, systematic grain growth has occurred in the Cu vias after each thermal cycle. The average grain size for the via in the as-received TSV specimen is 0.69 μm. After thermal cycling to 100, 200, 300, and 400 °C, the average grain sizes have grown by 18.4%, 26.8%, 46.8%, and 61.4%, to 0.81, 0.87, 1.00, and 1.11 μm, respectively.

With the EBSD technique, the grain orientation of the Cu vias is quantitatively measured. In Fig. 5a and b, the inverse pole figures of the grain orientations are plotted for the TSVs along directions normal to the TSV length (ND) and parallel to the TSV length (RD). Overall, there appears to be no preferred Cu grain orientation in all the specimens before and after thermal cycling. This observation is in agreement with studies reported by other groups [10,11]. The lack of preferred grain orientation indicates a statistically isotropic grain structure in the Cu vias, and thus the thermomechanical properties of the Cu can be treated as isotropic in the thermal stress analysis. In addition, the misorientation across grain boundaries obtained from the EBSD measurements is plotted in Fig. 6a and b. There exist a large number of twin boundaries with a characteristic misorientation angle of 60° across the grain boundaries for all the vias examined. The presence of twin boundaries may lead to relatively high yield strength of the Cu vias [12].

Based on the microstructure analysis, the curvature–temperature behavior of the fully-filled TSV specimen can be understood as the following. The nonlinear curvature–temperature relation during heating of the first cycle is mainly attributed to the nonlinear stress relaxation caused by grain growth. Similar curvature behavior due to grain growth has been observed for Cu thin films [13,14]. As grain growth can eliminate grain boundaries and reduce the excess volume, it is favored when the average stress in the Cu vias is compressive during heating [15]. The nearly linear curvature–temperature behavior during cooling and subsequent cycles suggests stabilized grain structures in the Cu vias. The grain structures would remain largely stabilized as long as the temperature doesn't exceed the highest temperature that the TSV specimen has experienced in any of the previous cycles. When the temperature was increased beyond the highest temperature in the previous cycles, the grain structures would evolve further with additional grain growth and stress relaxation. Furthermore, the annealing process in Fig. 2b shows continual stress relaxation at the high temperature. In general, grain growth is a kinetic process that depends on both temperature and stress [16].

2.3. Measurement by micro-Raman spectroscopy

For the TSV structure, the thermal stresses in Cu can in turn induce stresses in the Si matrix surrounding the TSVs where the stress distribution near the wafer surface is particularly important since most of the active devices are located near the surface. To measure the near surface stresses in Si, micro-Raman spectroscopy technique is used. Raman spectroscopy relies on the inelastic scattering (or Raman scattering) of Si, and the frequency shift of the Raman modes provides a measure of the stress in Si. The theory of Raman measurement and its application for TSV structures have been developed previously [17,18] and here we describe only the experiments performed in this study. Under the [001] backscattering configuration, only the longitudinal Raman mode can be detected. Assuming a biaxial stress state near the wafer surface, the following relation can be deduced from the secular equation for (001) Si [19],

$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega_3(cm^{-1}), \tag{1}$$

where $\sigma_r + \sigma_\theta$ is the sum of the in-plane normal stresses, and $\Delta\omega_3$ is the Raman frequency shift of the longitudinal Raman mode. With Eq. (1), the stress sum near the wafer surface can be determined from the measurement of $\Delta\omega_3$.

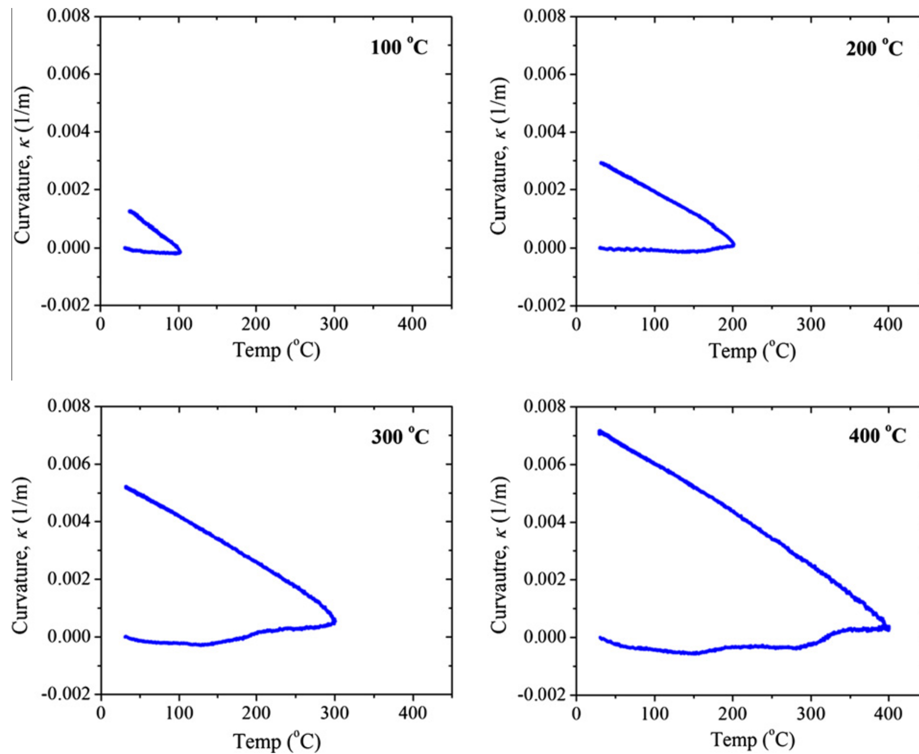


Fig. 3. Curvature–temperature measurements for TSV specimens subject to thermal cycles with the highest temperature at 100 °C, 200 °C, 300 °C, and 400 °C.

In this study, Raman measurements were carried out with a commercial micro-Raman Spectrometer equipped with a 442 nm Ar laser. Two TSV specimens were subjected to similar thermal treatment as those in the wafer curvature experiments (Fig. 2). Specimen C was heated to 200 °C and then immediately cooled down to room temperature (RT), and specimen D was heated to 300 °C and annealed for 1 h prior to cooling down. For both specimens, the Raman measurements were conducted at RT by scanning across two neighboring vias along the [1 1 0] direction. To deduce the frequency shift $\Delta\omega_3$, a reference Raman frequency ω_0 is required, which was determined by extending the measurement to areas far away from the TSVs where the stress is assumed to be zero [20]. With the calibrated reference frequency ω_0, the sum of the two principal stresses in Si is deduced from the measured Raman frequency using Eq. (1).

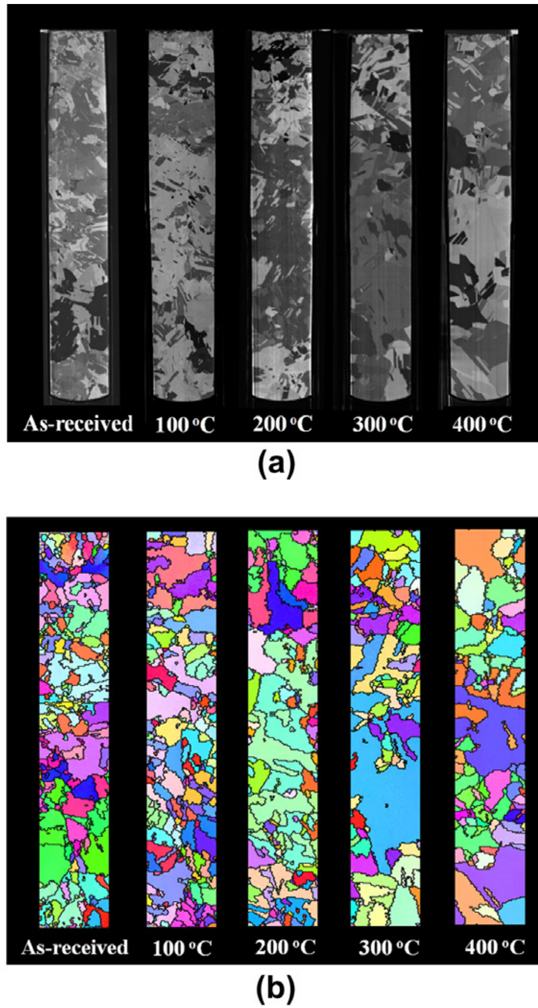
The measured Raman intensity and frequency shift obtained from specimen C are shown in Fig. 7, representing typical results obtained from Raman measurements. A sudden drop of the Raman intensity was observed near the Cu/Si interface. The distributions of the stress sums deduced from the Raman measurements are plotted in Fig. 8a and b. Clearly, a sub-micron resolution was achieved in the measurement, but the results provided only the sum of the two individual stress components in Si. Further understanding of the stress characteristics in the TSV structure requires detailed stress analysis to delineate the stress components and correlate the micro-Raman measurements with the thermal cycling experiments. This is discussed in the next section.

2.4. Stress analysis

Finite element analysis was performed to correlate the global stress behavior of the TSV structure measured by the wafer curvature technique and the local stress in Si measured by the micron-Raman technique. A three-dimensional finite element model was constructed using the commercial package, ABAQUS (v6.10). A quarter of the via with symmetric boundary conditions in the [1 1 0] and $[1\bar{1}0]$ directions was modeled to simulate the periodic TSV array used in the Raman measurement. At the TSV/Si interface, the oxide barrier layer with a nominal thickness of 0.4 μm was included in the model, while the thin Ta barrier layer was neglected. The anisotropy of Si was taken into consideration by using the anisotropic elastic constants for Si [21], and Cu is treated as isotropic based on the microstructure analysis by EBSD. The following material properties were used for Cu and SiO_2: Young's modulus, E_{Cu} = 110 GPa and E_{oxide} = 70 GPa; Poisson's ratio, ν_{Cu} = 0.35 and ν_{oxide} = 0.16. The CTEs are α_{Cu} = 17 ppm/°C, α_{Si} = 2.3 ppm/°C and α_{oxide} = 0.55 ppm/°C. The effect of Cu plasticity is discussed in Section 3.

Since the Raman signal penetrates up to 0.2 μm from the wafer surface [20], the stress components are extracted from 0.2 μm below the wafer surface. The contours of the stress sum at 0.2 μm below the wafer surface obtained by FEA are shown in Fig. 9a for $\Delta T = -270$ °C, where the stress distribution exhibits a fourfold symmetry, reflecting the cubic symmetry of Si. The stress variation is slightly different in the [1 1 0] and $[1\bar{1}0]$ directions due to the different pitch distances in those directions. The stress sum in Si becomes positive, except for the regions very close to the via as a result of the interaction between neighboring vias in the periodic array. The stress anisotropy is shown in Fig. 9b by plotting the stress sum along directions rotated by an angle of θ from the [1 1 0] direction. The results indicate that the near-surface stress as measured by Raman spectroscopy depend on the direction of Raman scanning and is enhanced by the interaction between the neighboring vias. A relatively strong Raman signal is expected for scanning along the [1 1 0] direction (θ = 0°), where the stress sum reaches a positive peak of ~90 MPa at 10 μm away from the Si/Cu interface.

Next, the sums of the in-plane stresses obtained by FEA for specimens C and D are calculated and compared with the Raman measurements. The thermal loads for the two specimens were



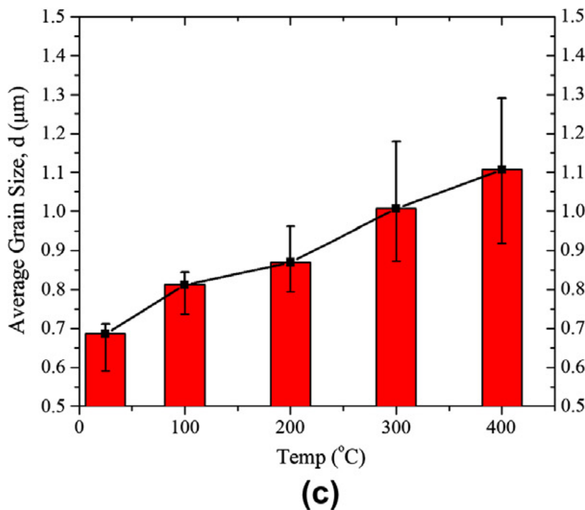


Fig. 4. (a) Focused ion beam images of TSVs after different thermal loads. (b) Grain mapping by EBSD. (c) Average grain sizes.

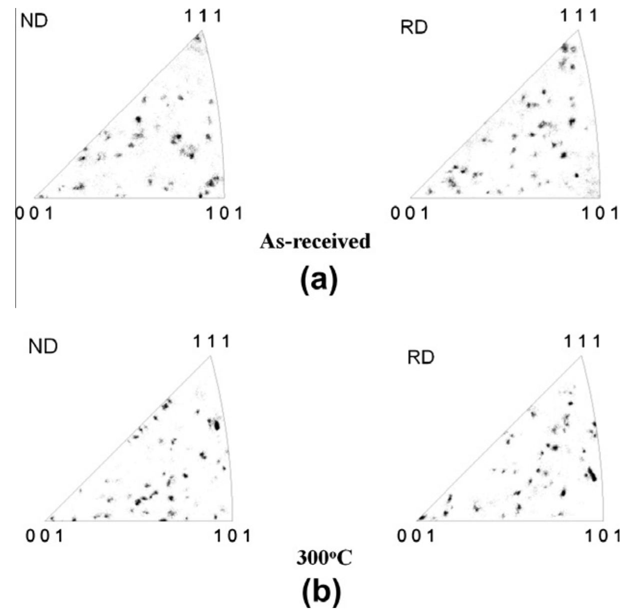


Fig. 5. Inverse pole figures of (a) as-received TSV and (b) TSV after thermal cycling to 300 °C. Two measurement directions were defined: ND (normal to the TSV axis) and RD (parallel to the TSV axis).

chosen to be the same as specimens A and B in the curvature measurements (Fig. 2) to facilitate the correlation of the results from the two techniques. Based on the curvature measurements, the reference temperature for specimen C is taken to be 100 °C, and that for specimen D is 300 °C, corresponding to thermal loads of $\Delta T_C = -70$ °C and $\Delta T_D = -270$ °C relative to the room temperature of 30 °C. As shown in Fig. 8, the FEA results are in reasonable agreements with the Raman measurements. Moving away from the Cu/Si interface, the sum of the stresses first increases sharply, and then gradually decreases. Between the two adjacent vias, the stress depends on the pitch distance as a result of the stress interaction. The measurement for specimen D (Fig. 8b) shows a higher stress level in Si than for specimen C, as a result of the higher negative thermal load for specimen D ($|\Delta T_D| > |\Delta T_C|$). Therefore, the stresses in Si around the TSVs depend on the thermal processes of the specimen.

3. Discussion

3.1. Comparison of stress behavior with thin film structures

The curvature–temperature behavior observed for the TSV specimen is very different from that of Cu thin films. Fig. 10a and b compare curvature measurements for a TSV specimen and a 0.6 μm electroplated Cu thin film specimen. Both specimens were first heated to 200 °C in two thermal cycles, and then heated to 350 °C in two subsequent thermal cycles. The curvature–temperature data for the thin film specimen exhibited the typical hysteresis loops due to plastic deformation of the Cu film [7]. In contrast, the TSV specimen showed distinctly different curvature behavior. During the first heating cycle, the curvature was nonlinear due to stress relaxation as discussed in Section 2.2. Subsequently, during cooling and the second cycle, the curvature showed a nearly linear behavior. The curvature remained linear in the third heating cycle until the temperature exceeded 200 °C. Heating beyond 200 °C led to additional stress relaxation, and the curvature became nonlinear in the third cycle from 200 °C to 350 °C. Finally, the curvature behavior became linear again during cooling of the third cycle, followed by a linear behavior during heating and cooling of the fourth cycle. Unlike the thin film specimen, no appreciable hysteresis loop was observed for the TSV specimen. We note that a nonlinear stress relaxation occurred for the thin film specimen during heating of the first and third cycles, similar to the TSV specimen. However, during the second and fourth cycles, the thin film specimen showed clearly a hysteresis loop.

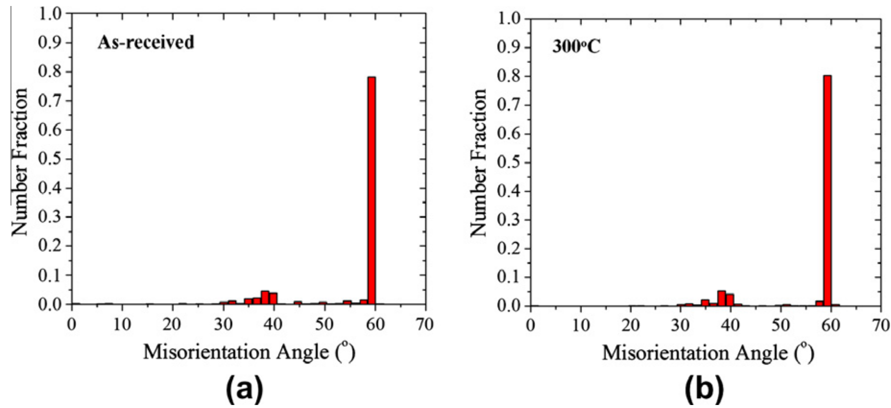


Fig. 6. Grain misorientation angles obtained by EBSD for (a) as-received TSV and (b) TSV after thermal cycling to 300 °C.

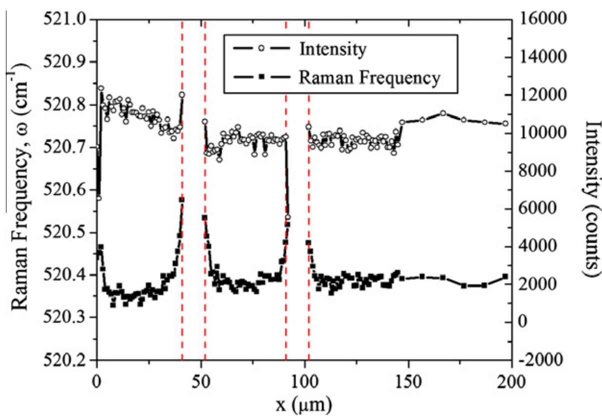


Fig. 7. Raman intensity (open symbols) and frequency (filled symbols) of a TSV specimen. Dashed lines indicate the Cu/Si interfaces.

The different curvature behaviors observed in the two specimens can be attributed to the different amounts of plastic deformation due to the different stress states and geometry. For the thin film specimen, the stress in the Cu film is typically biaxial and uniform. The stress in the Cu TSVs on the other hand is generally triaxial and non-uniform. The biaxial stress in the Cu film results in a relatively high von-Mises stress, which is the effective shear stress driving plastic deformation. In contrast, the effective shear stress in the Cu TSVs is relatively low. As shown in Fig. 10a and b, the FEA models of the two structures yield drastically different stress distributions under the same thermal load ($\Delta T = -270$ °C). In particular, the von-Mises stress in the Cu film is much higher than the Cu via. Take the yield strength of Cu to be 300 MPa, plastic deformation would be expected over the entire volume of the Cu film. In the Cu via, however, the von Mises stress is non-uniform and reaches the yield strength only in a small region near the via/Si interface and the wafer surface (Fig. 10a). Consequently, plastic deformation in the Cu via is expected to be highly localized within a small volume. Moreover, the volume fraction of Cu is relatively low in the TSV specimen compared to the thin film specimen. Therefore, the total volume of Cu that underwent plastic deformation was much smaller in the TSV specimen than in the thin film specimen. The localized plastic deformation has negligible effect on the overall curvature of the specimen, and thus no hysteresis was observed during the thermal cycling. For the first and third cycles, the nonlinear curvature–temperature behavior during heating is mainly due to grain growth-induced stress relaxation, for both the TSV and thin film specimens.

3.2. Effect of Cu plasticity on via extrusion

After thermal cycling, via extrusion was observed in the TSV specimen (Fig. 11a). A previous study has suggested that via extrusion could be caused by interfacial delamination [22]. However, in the present study, no evidence of interfacial delamination was observed. Instead, via extrusion appears to have occurred as a result of localized plastic deformation near the via/Si interface during thermal cycling [23]. An elastic–plastic FEA model is constructed to investigate the effect of Cu plasticity on via extrusion. In general, the plastic deformation in the Cu TSVs depends on the thermal load and the yield strength of Cu. For the present study, the yield strength

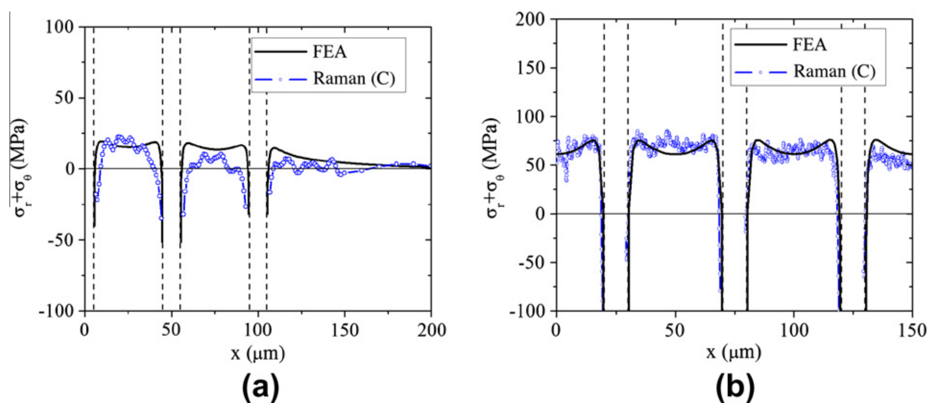


Fig. 8. Comparison of the near-surface stress distribution between Raman measurements and FEA: (a) Specimen C; (b) Specimen D.

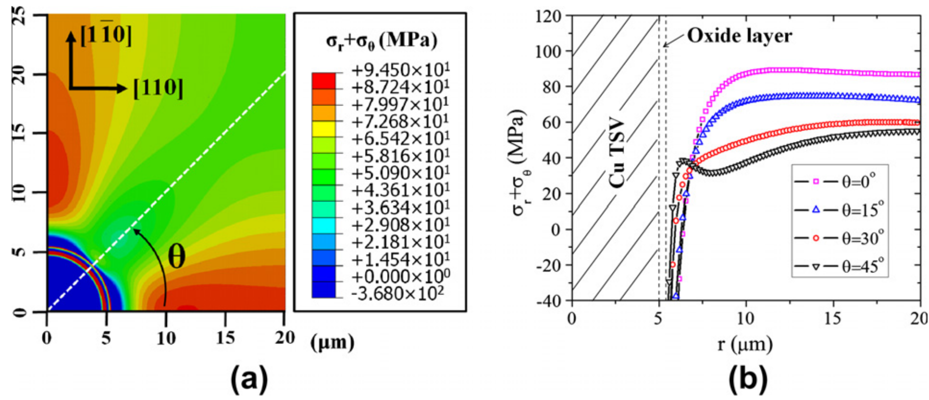


Fig. 9. (a) Contour of the stress sum ($\sigma_r + \sigma_\theta$) near the (001) Si wafer surface ($z = 0.2\ \mu$m) around a Cu TSV. (b) Directional dependence of the stress distribution ($\Delta T = -270\ ^\circ$C).

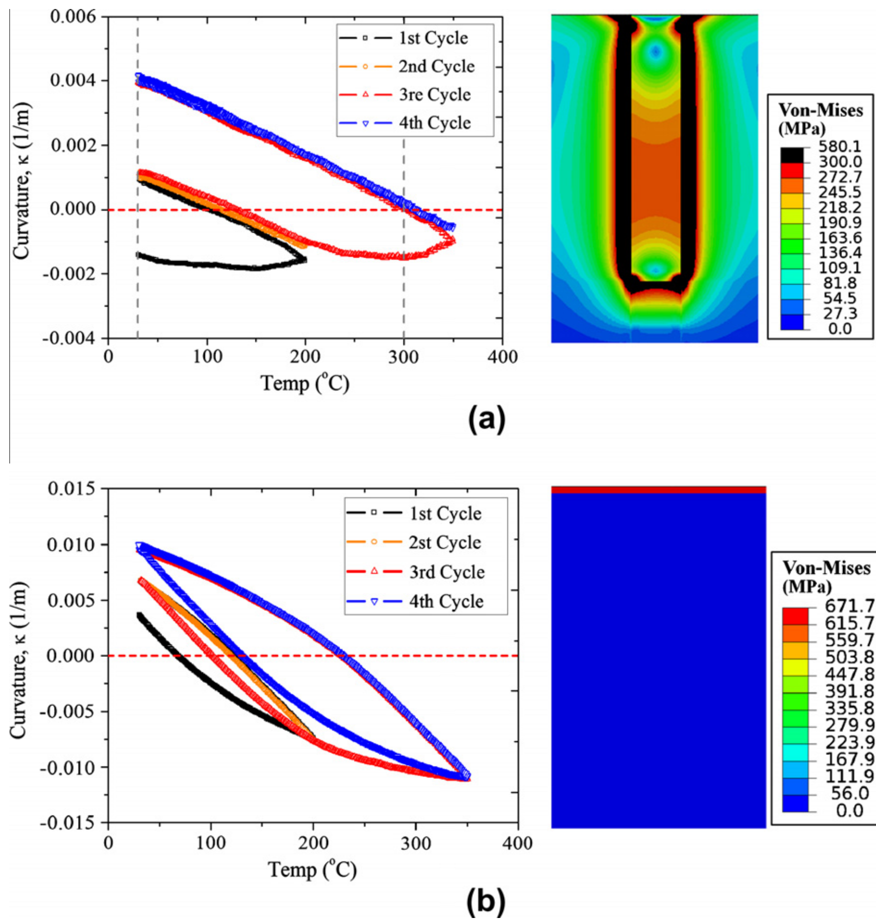


Fig. 10. Comparion between the measured curvature–temperature behaviors for (a) Cu TSV and (b) Cu thin film structures, along with the von Mises stresses obtained from finite element analysis ($\Delta T = -270\ ^\circ$C).

of Cu is assumed to be 300 MPa and a thermal load of $\Delta T = 270\ ^\circ$C is applied. In Fig. 11b, the deformed shape by the FEA model clearly shows extrusion of the via, similar to what was observed in our experiments. As discussed in Section 3.1, plastic deformation in the Cu via is highly localized, as shown in Fig. 11c, where the equivalent plastic strain is non-zero only in a small region near the top of the via. The plastic yielding of Cu near the interface effectively relaxes the constraint of the surrounding materials and allows the via extrusion without interfacial delamination. Moreover, the local plasticity in Cu could also enhance the total fracture energy for interfacial delamination [24] and thus help prevent delamination. The localized plasticity found in this analysis provides an interesting and distinctive mechanism for via extrusion. This mechanism could be of basic importance for improving the reliability of the Cu TSV structures.

In addition to Cu plasticity, the grain growth observed in this study could be another important deformation mechanism in the Cu vias. Similar grain growth phenomenon has been extensively studied for electroplated Cu films [14,25]. The grain structure evolution plays an important role in determining the Cu interconnect

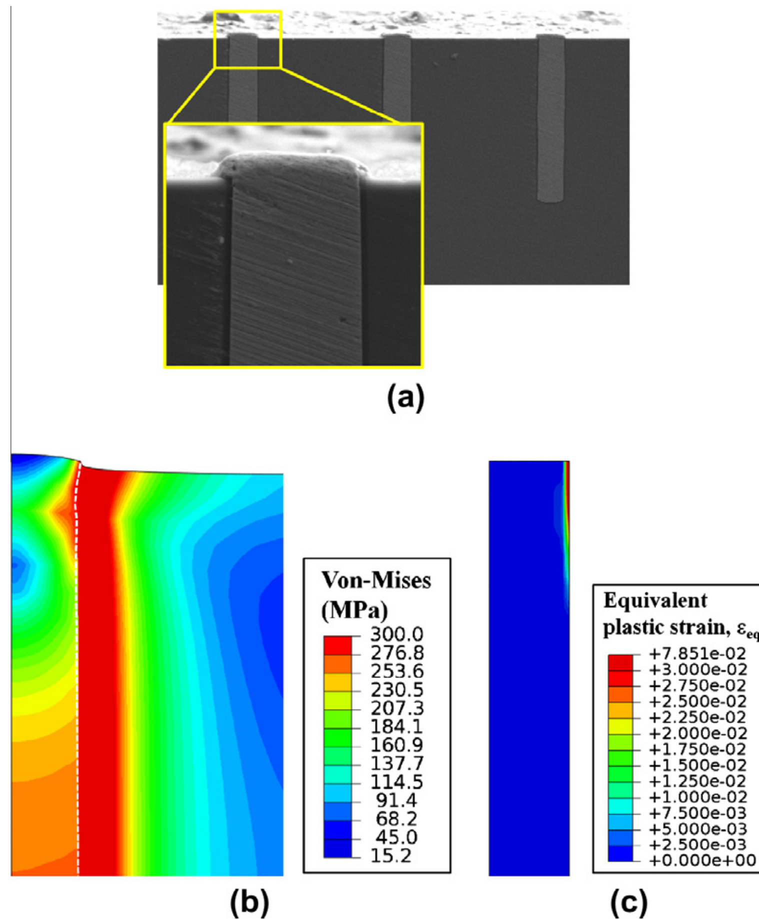


Fig. 11. (a) SEM image of TSV extrusion observed after thermal cycling. (b) Stress distribution and deformation of TSV by an elastic–plastic FEA model. (c) Equivalent plastic strain in the TSV by FEA (yield strength = 300 MPa, ΔT = 270 °C).

reliability, such as electromigration and stress voiding [26–28]. The effects of grain growth on the TSV structures have not been fully understood. It is known that grain growth could lower the yield strength of Cu according to the Hall–Petch relation [29]. Thus, with higher process temperatures, more grain growth would lead to more plastic deformation in the Cu via, and thus more via extrusion. Therefore, in the fabrication of TSV structures, it is important to stabilize the Cu grain structures before subsequent thermal processing in order to minimize via extrusion. Based on the wafer curvature measurements in the thermal cycling experiments, the linear curvature behavior following the heating cycle indicates that the grain structure in the Cu vias can indeed be stabilized. This suggests that the annealing process can be optimized to prevent via extrusion, for example, by exposing the TSV structure to a maximum grain-stabilizing temperature T_m (e.g., ∼300–350 °C), followed by a one-time chemical–mechanical planarization (CMP) process to remove the extruded Cu. With the grain structure stabilized, via extrusion can be eliminated in subsequent fabrication processes as long as the temperature does not exceed T_m.

3.3. Keep-out zone (KOZ)

The thermal stresses induced around the TSVs can degrade the performance of devices near the wafer surface due to stress-induced carrier mobility change in Si. It has been reported that the thermal stresses induced by TSVs can cause up to 30% shift in the saturation drain current (I_{DSAT}) of nearby transistors [30]. This effect has to be taken into account in the consideration of the keep-out zone (KOZ) for devices near the TSVs [31,32]. Stress induced mobility change has become an increasingly important reliability issue and design parameter for 3-D integration with TSVs.

The stresses affect the carrier mobility through the piezoresistivity effect of Si. For the [1 0 0] channel direction in a Si (1 0 0) wafer, the mobility change ($\Delta\mu$) can be related to stresses through the piezoresistance coefficient (π_{ij}) by the following relation [33],

$$\Delta\mu/\mu = |\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})| \quad (2)$$

Table 1 lists the piezoresistance coefficients for n- and p-type Si. When the transistors are aligned along other directions such as [1 1 0], both the stresses and piezoresistance coefficients have to be transformed to the new direction to calculate the mobility change. The detailed approach has been described elsewhere [32].

We use FEA to calculate the stresses for an isolated TSV structure subjected to thermal cycling to 350 °C, a typical temperature for TSV processing. As shown in Fig. 10a, the curvature measurement suggested that the reference temperature is about 300 °C for the TSV structure subjected to similar thermal processes. The corresponding thermal load is thus ΔT = −270 °C when the TSV is

Table 1
Piezoresistance coefficients for n- and p-Type Si (in units of 10^{-11} Pa^{-1}).

	π_{11}	π_{12}	π_{44}
n-Type Si	−102.2	53.7	−13.6
p-Type Si	6.6	−1.1	138.1

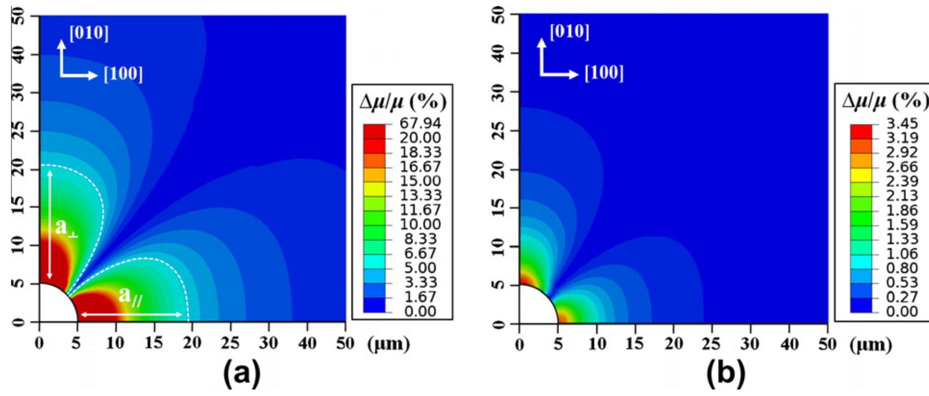


Fig. 12. Mobility change for (a) n-type and (b) p-type Si with [100] channel direction for $\Delta T = -270$ °C.

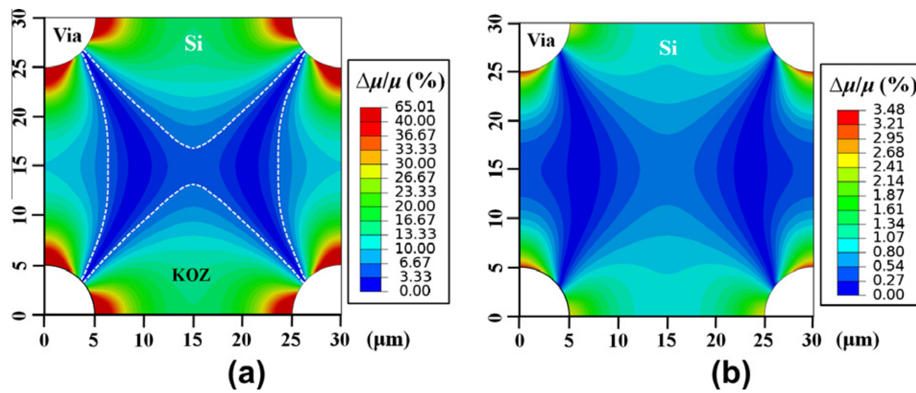


Fig. 13. Effect of stress interaction on KOZ for (a) n-type and (b) p-type Si with [100] channel direction for $\Delta T = -270$ °C ($p/D = 3$).

cooled down to the room temperature (∼30 °C). The stress components are calculated on the Si surface, with which the mobility change is calculated by Eq. (2). The contours of mobility change for n-type and p-type Si devices are shown in Fig. 12, assuming the [100] channel direction. Since both the elastic properties and the piezoresistance of Si are anisotropic, the mobility change depends on the location of the device in an anisotropic manner. For n-type Si (Fig. 12a), the maximum mobility change has reached 67%. Defining the KOZ based on the minimum mobility change of 5%, the boundary of the KOZ can be determined, shown as the dashed lines in Fig. 12a. The extent of the KOZ for the n-type Si is slightly different in the [010] and [100] directions. Therefore, two characteristic distances, $a_{\perp}$ and $a_{//}$, are used to represent the size of KOZ. In contrast, for p-type Si, the maximum mobility change is below 5% (Fig. 12b). Thus, no KOZ is defined for the p-type Si. In a separate study [32], it was found that the trend is reversed for the [110] channel direction, i.e., no KOZ for n-type Si whereas a KOZ is defined for p-type Si.

For TSV arrays, the pitch distance (p) between the TSVs can be small enough to generate stress interactions between the neighboring vias. The effect of stress interaction on KOZ was studied by FEA modeling of a TSV array with different pitch distances. It was found that the effect of stress interaction becomes significant when the pitch to diameter ratio (p/D) is less than 5 [32]. Fig. 13 shows the mobility change and KOZ for $p/D = 3$, for both n-type and p-type of Si with [100] channel direction. For n-type Si, the KOZs of the neighboring vias overlap and merge (Fig. 13a). For p-type Si, the maximum mobility change near the TSV has increased slightly compared to the isolated TSV (Fig. 13a), but no KOZ is defined by the 5% minimum mobility change.

4. Summary

In this paper, the thermal stresses in the TSV structures are studied using experimental methods and numerical analysis. The thermal stresses of TSV specimens were measured first using the precision wafer curvature technique in thermal cycling experiments. Following this measurement, the microstructure of the Cu vias was analyzed. Next, micro-Raman spectroscopy was used to measure the local stress distribution in Si near the TSVs. The results of Raman measurements were correlated with the wafer curvature measurements along with finite element analysis to understand the thermomechanical behavior of the TSV structures during thermal cycling. It was found that plastic deformation is highly localized in the Cu vias, which led to a nearly linear curvature behavior except for the first heating cycle. On the other hand, the local plastic deformation could be sufficient to cause via extrusion. Finally, the stress analysis was extended to study the keep-out zone (KOZ) near the TSVs, which is an important design and reliability issue for 3D integrated circuits.

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