Thermomechanical Reliability Challenges for 3D Interconnects

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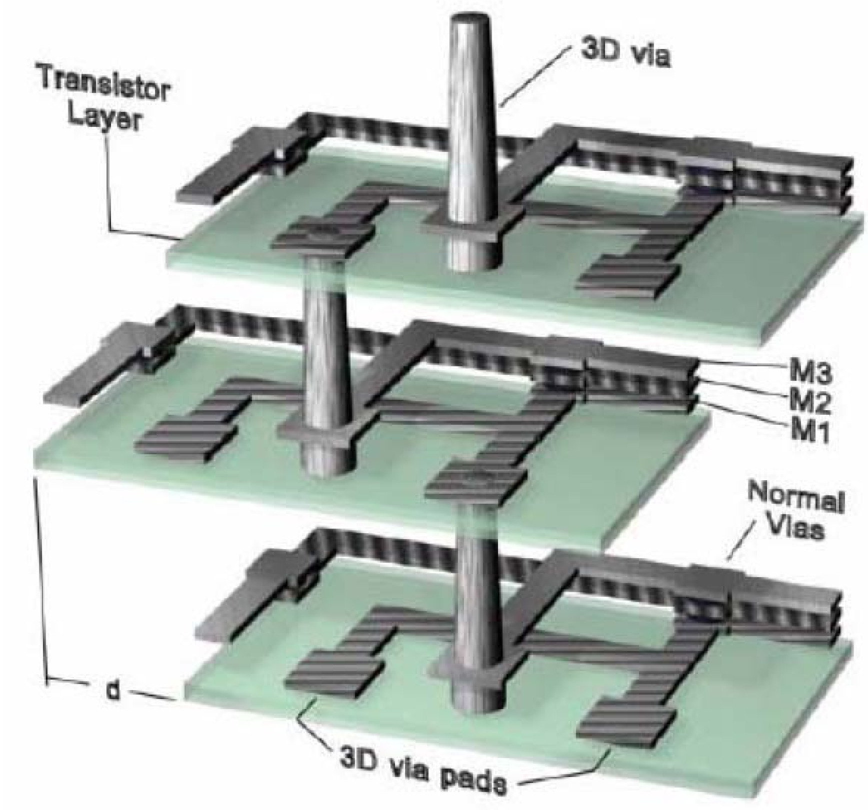
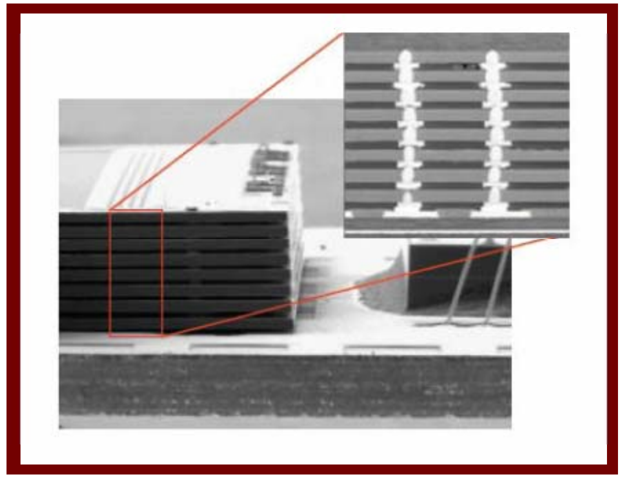
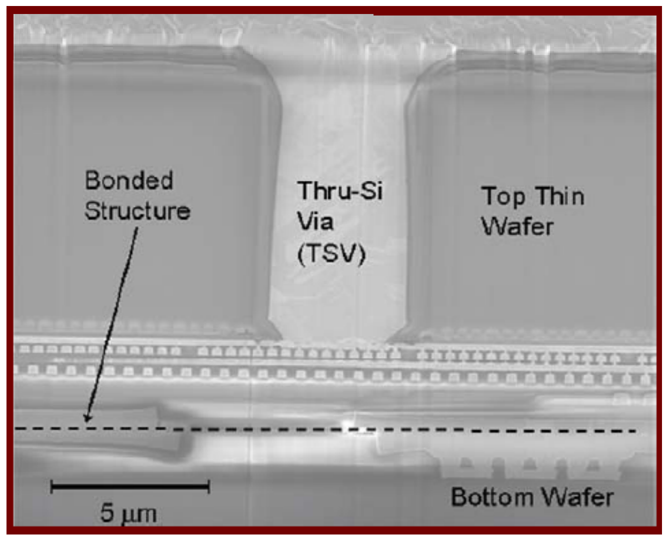
Wafer Level 3D Integration





Memory stacks (Samsung)



Intel 300 mm multicore processors

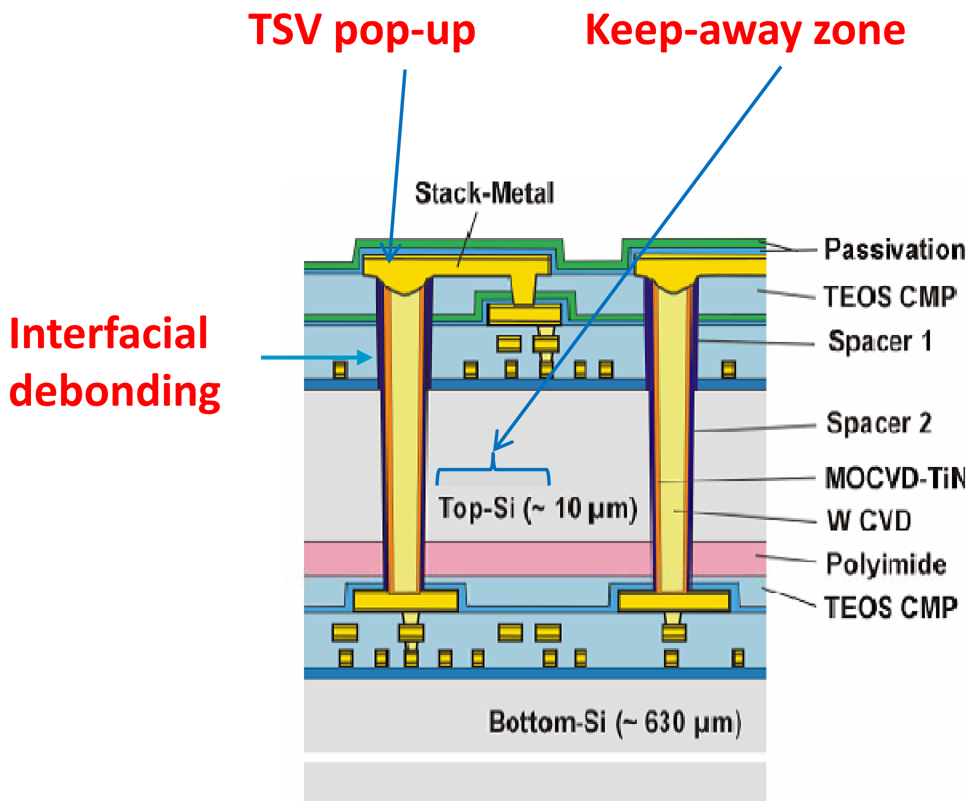
Mechanical effects:

- Through silicon vias (TSVs)
- Wafer thinning
- Wafer (die) bonding

Philip Garrou, Microelectronic Consultants of NC

TSV Mechanical Reliability

- **Stress around TSVs:**
  - ***Keep-away zone*** for FEOL
  - Cracking of silicon
- **Stress at the interfaces:**
  - **Debonding, TSV pop-up**
- **Stress inside TSVs:**
  - Plastic deformation
  - Stress-induced voiding
  - Stress migration

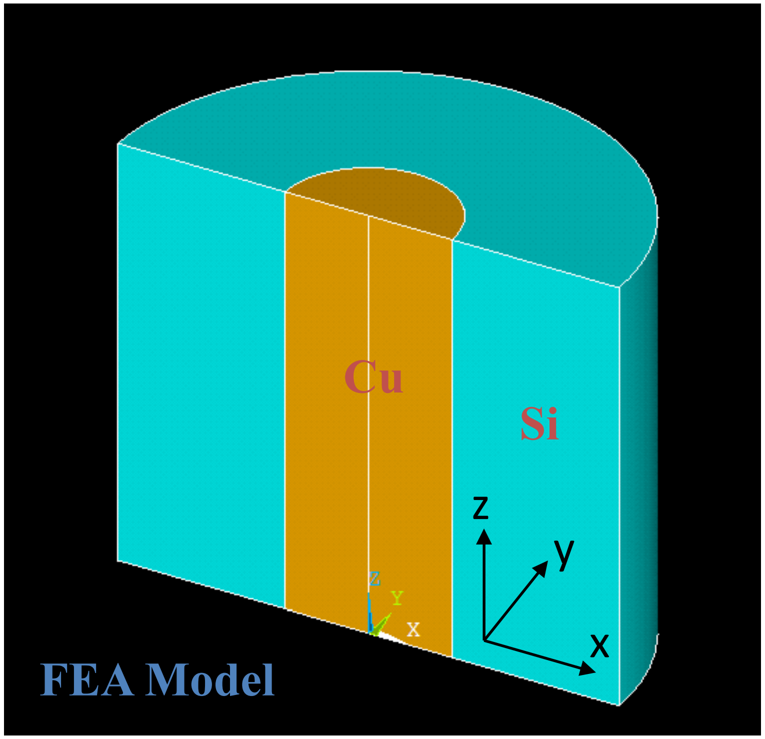


- **Sources of stress:**
  - Process-induced stress
  - Thermal stress – BEOL process
  - Packaging induced stress

TSV stress and reliability depends on both materials processing and structural design.

Stress and Reliability Analysis of TSV

- **Analytical solutions**
  - 2D approximation
  - Near-surface stress distribution by method of superposition
- **Finite element analysis**
  - Effect of liners/barrier layers
  - Effect of wafer thickness
  - Effect of elastic mismatch
  - Effect of nail head
- **Fracture analysis**
  - Calculation of ERR
  - Cohesive crack simulations



Process Induced Stress Simulation

TEOS/barrier layer deposition 400~430ºC

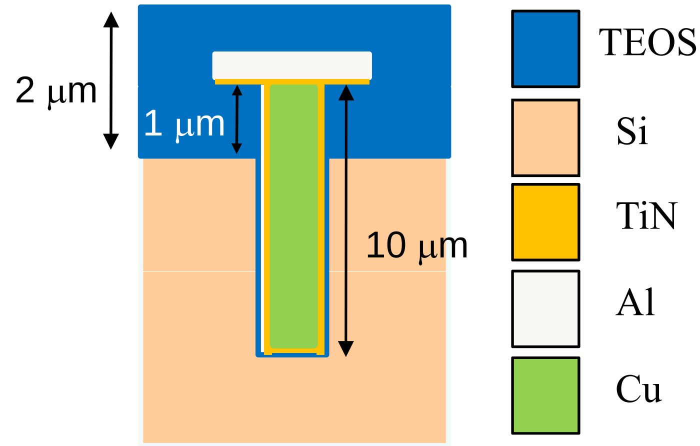
Cu electroplating @ 30ºC Annealing @ 200ºC

Cooling down to 30ºC Cu CMP

Capping layer deposition 150ºC

CVD of TEOS @ 400ºC

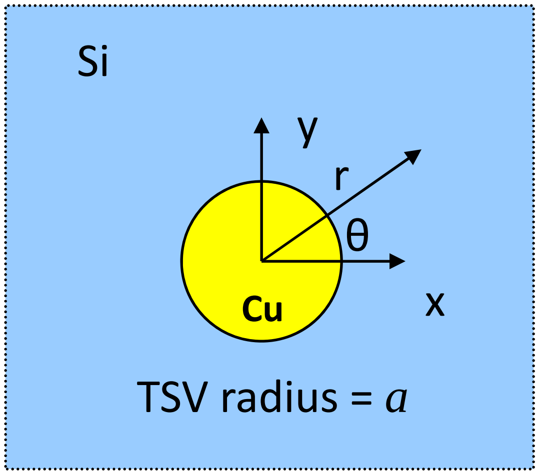
Cooling down to 25ºC

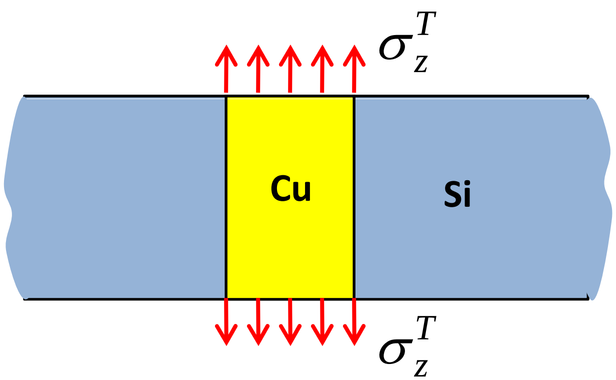


TSV diameter: ~2 μm

Critical steps for **interfacial delamination and silicon cracking**

Thermal Stress: 2D Approximate Solution





Thermal Strain:

$$\varepsilon_T = (\alpha_{Cu} - \alpha_{Si})\Delta T$$

Uniform thermal stress in Cu via (triaxial):

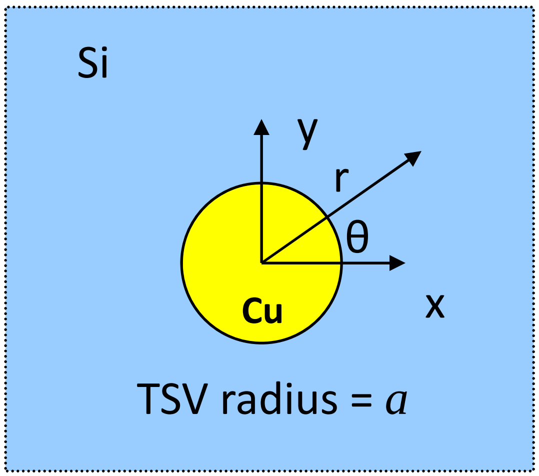
$$\sigma_r = \sigma_\theta = \frac{-E\varepsilon_T}{2(1-\nu)}, \qquad \sigma_z = \frac{-E\varepsilon_T}{1-\nu}$$

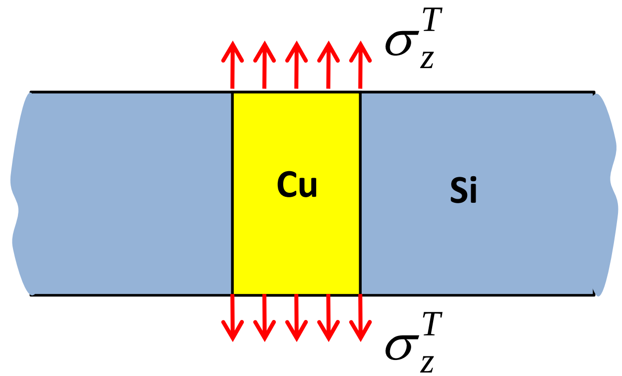
Stress distribution in Si (biaxial):

$$\sigma_r = -\sigma_\theta = \frac{-E\varepsilon_T}{2(1-\nu)}\frac{a^2}{r^2}, \qquad \sigma_z = 0$$

- The magnitude of the stresses in the via is independent of the via size.
- The stresses in Si decay with the distance (r), with the decay length proportional to the via size (a).

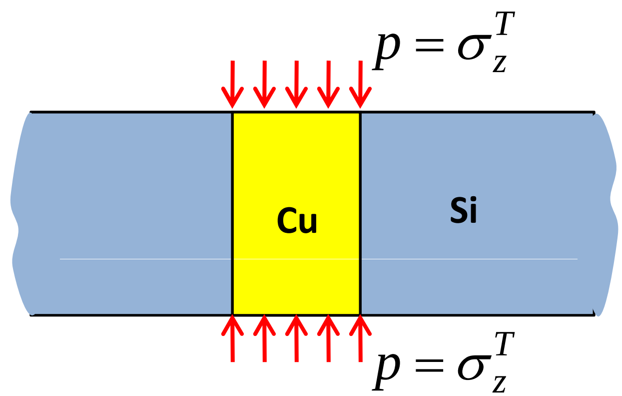
Method of Superposition





Problem A:

uniform thermal stress in Cu

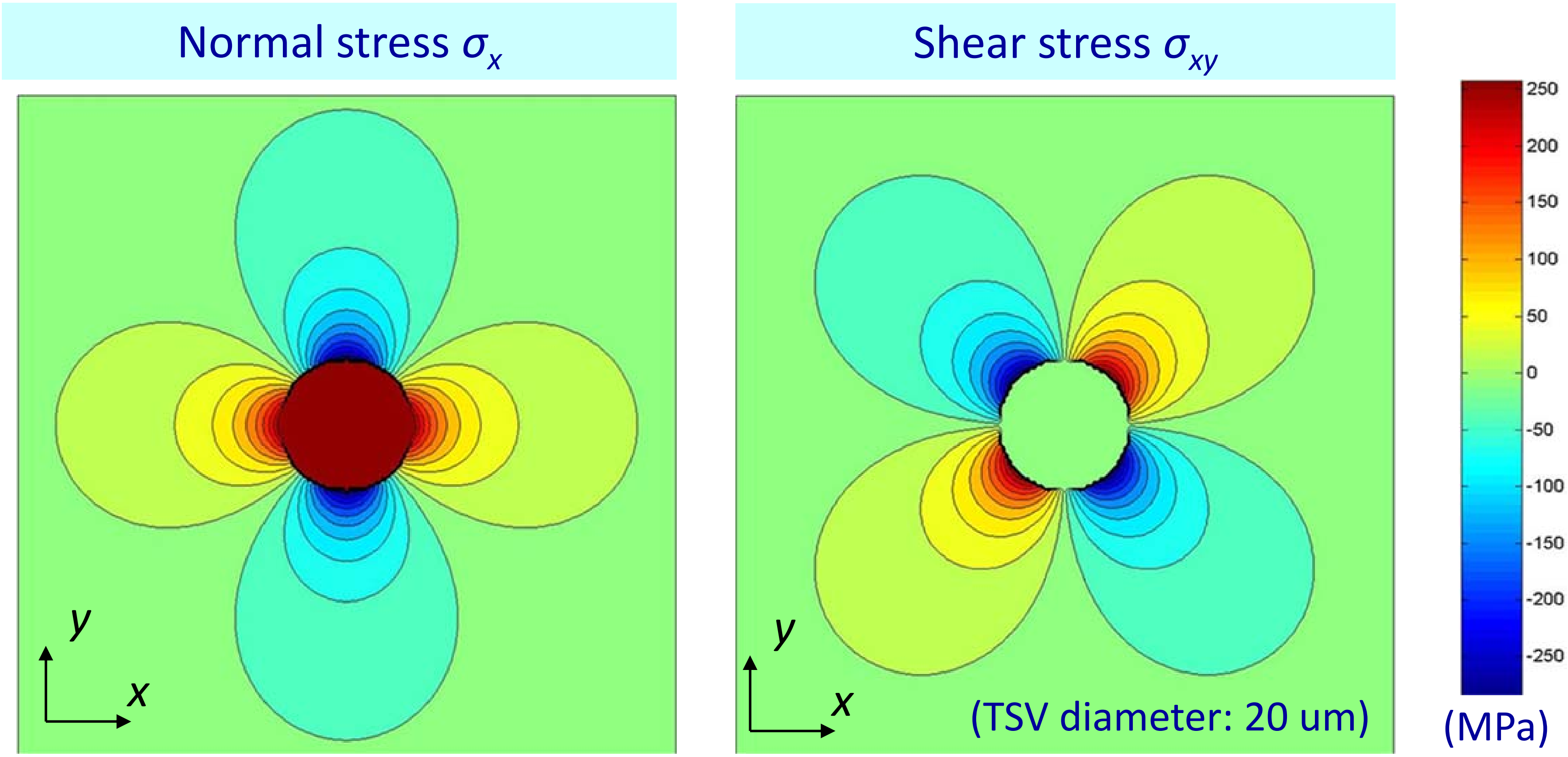


Problem B:

3D Stress redistribution near surface

- For a high aspect-ratio TSV, the stress field away from the surfaces can be obtained from a 2D plane-strain solution (Problem A).
- The stress field near surface is 3D in general, which can be determined by superimposing an opposite surface loading (Problem B) onto the 2D field (Problem A) to satisfy the boundary conditions at the surface.

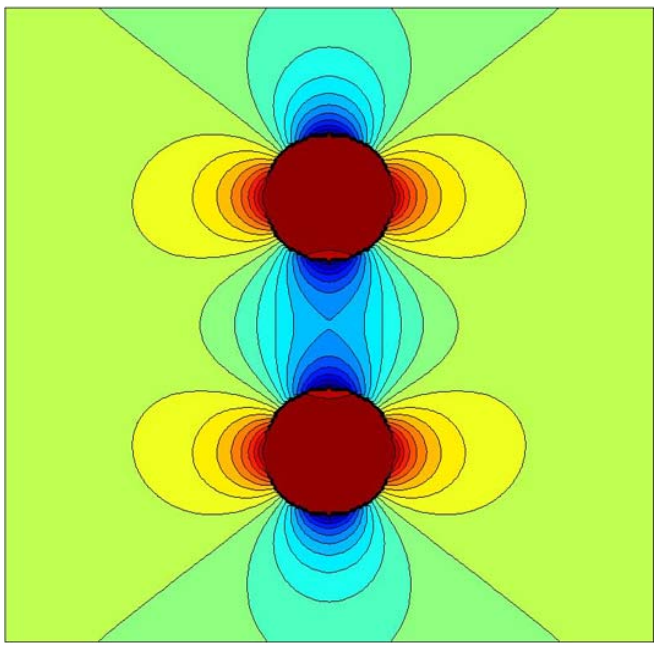
2D Stress Field of Single Via



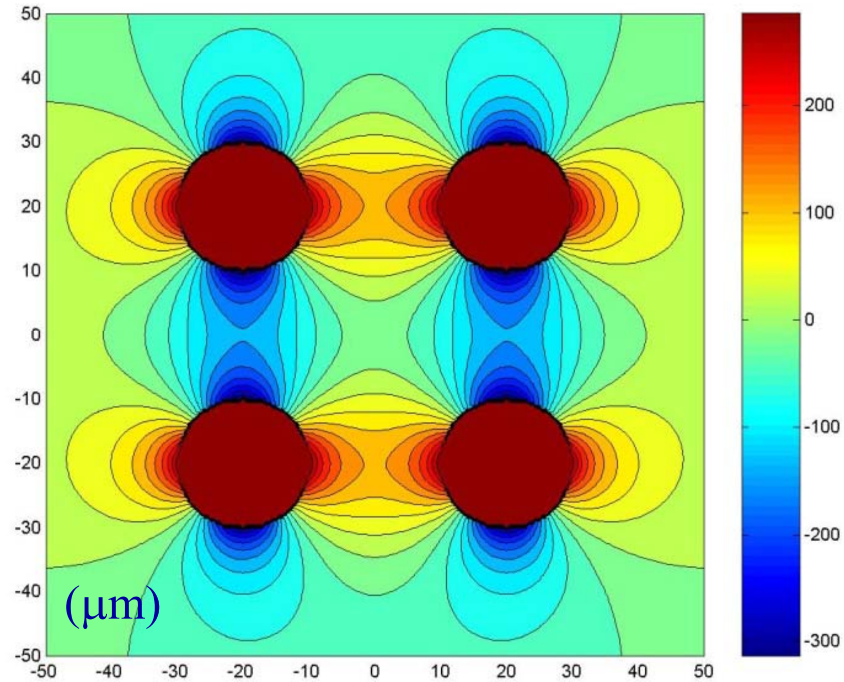
- Assume stress free at high temperature (reference)
- Cooling from the reference temperature ($\Delta T = -175^oC$) leads to tensile stresses in the via.
- Around the via, the stress is tensile in the radial direction and compressive in the circumferential direction, both concentrated near the via.

Proximity Effect on Keep-away Zone

Normal Stress σ_x

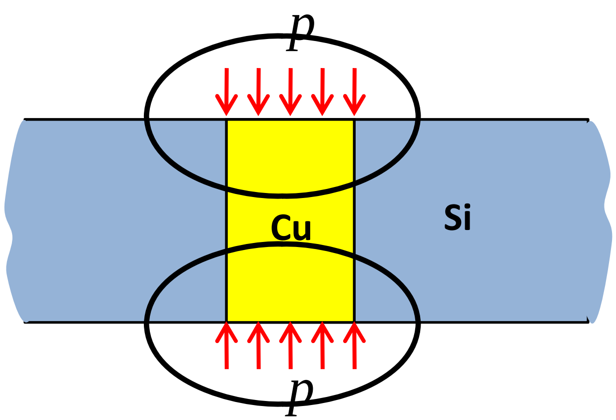


Normal Stress σ_x (MPa)



- Proximity of TSVs increases the area with high thermal stress and affect the keep-away zone.

3D Stress Field near Surface (Problem B)



Uniform surface pressure over a circular area

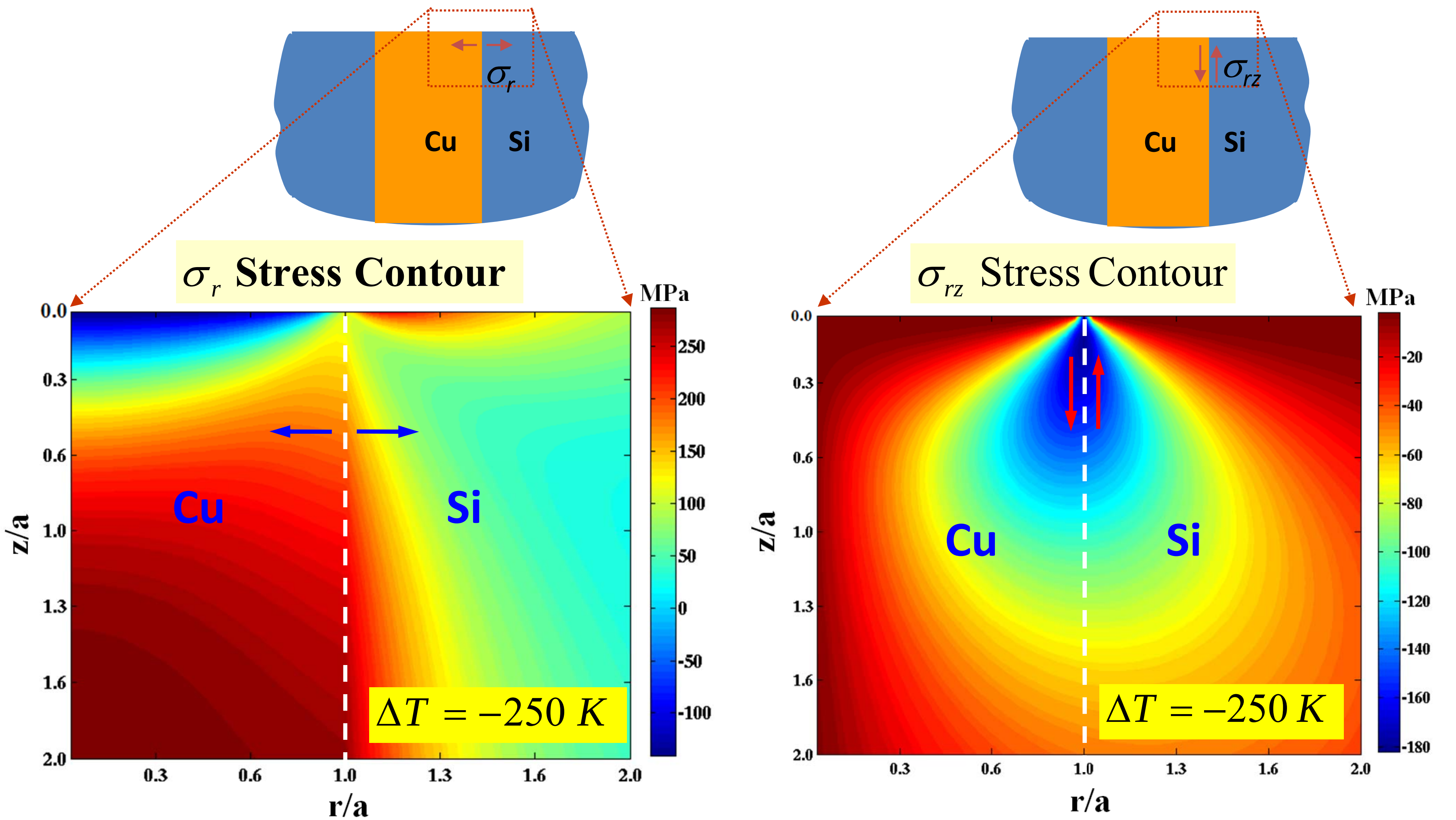
$$p = \sigma_z^T = \frac{E\varepsilon_T}{1-\nu}$$

- Stress decays with the distance from the surface.
- Triaxial stress in the via center (r = 0).
- Radial and circumferential stresses on the surface (z = 0).
- Shear stress at the interface.

$$\sigma_z(r=0) = \frac{E\varepsilon_T}{1-\nu}\left[\frac{z^3}{(a^2+z^2)^{3/2}} - 1\right] = \frac{E\varepsilon_T}{1-\nu} f\left(\frac{z}{a}\right)$$

$$\sigma_r(r=0) = \sigma_\theta(r=0) = \frac{E\varepsilon_T}{2(1-\nu)}\left[-2\nu + \frac{(1+2\nu)z}{\sqrt{a^2+z^2}} + \frac{a^2 z}{(a^2+z^2)^{3/2}}\right]$$

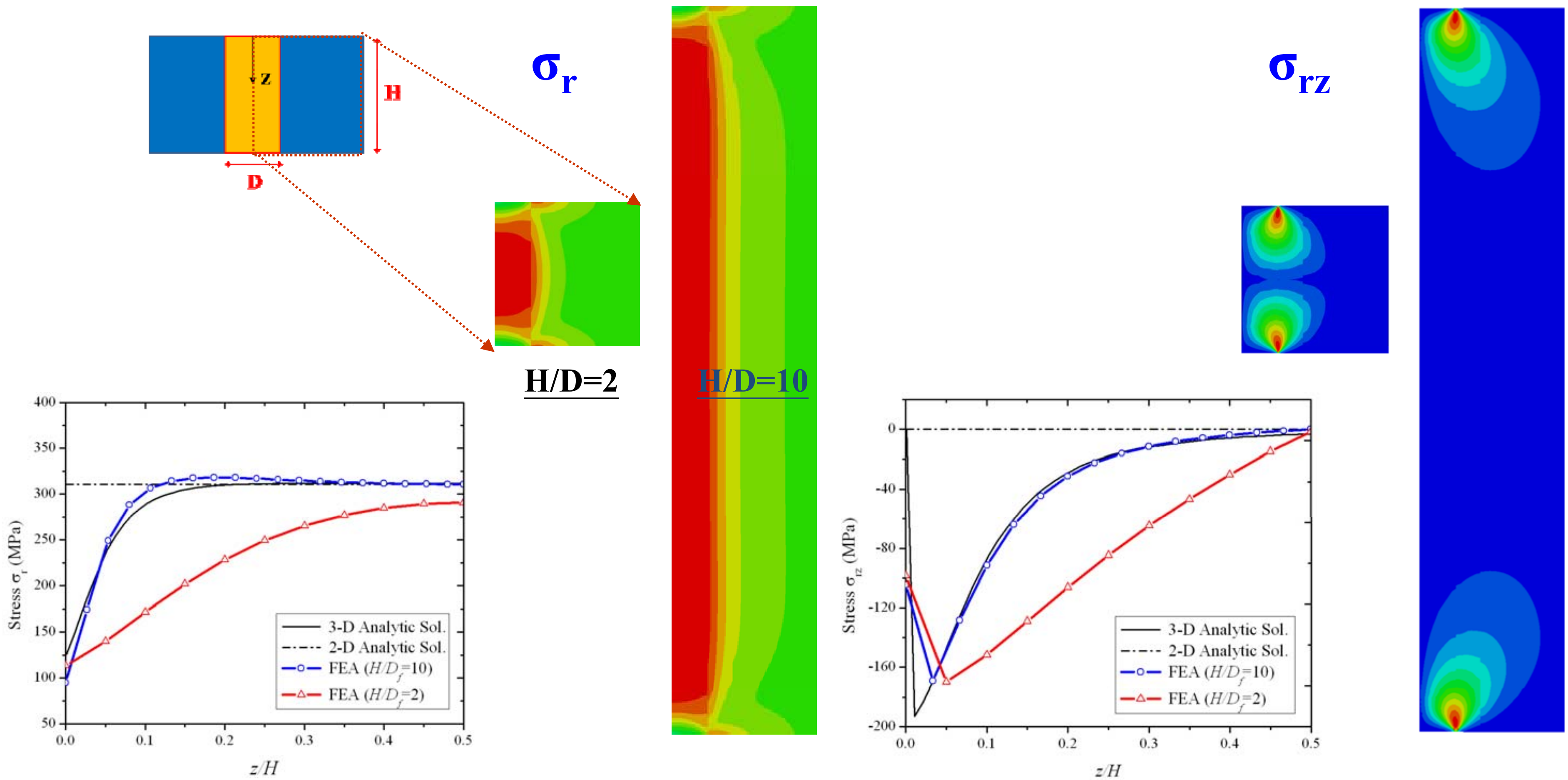
Stresses near Wafer Surface



Positive opening stress along Cu/Si interface

Concentration of the shear stress at the surface/interface junction

FEA: Effect of Wafer Thickness



- At the Cu/Si interface, the opening stress (σ_r) decreases but the shear stress (σ_{rz}) increases as the aspect ratio H/D decreases.

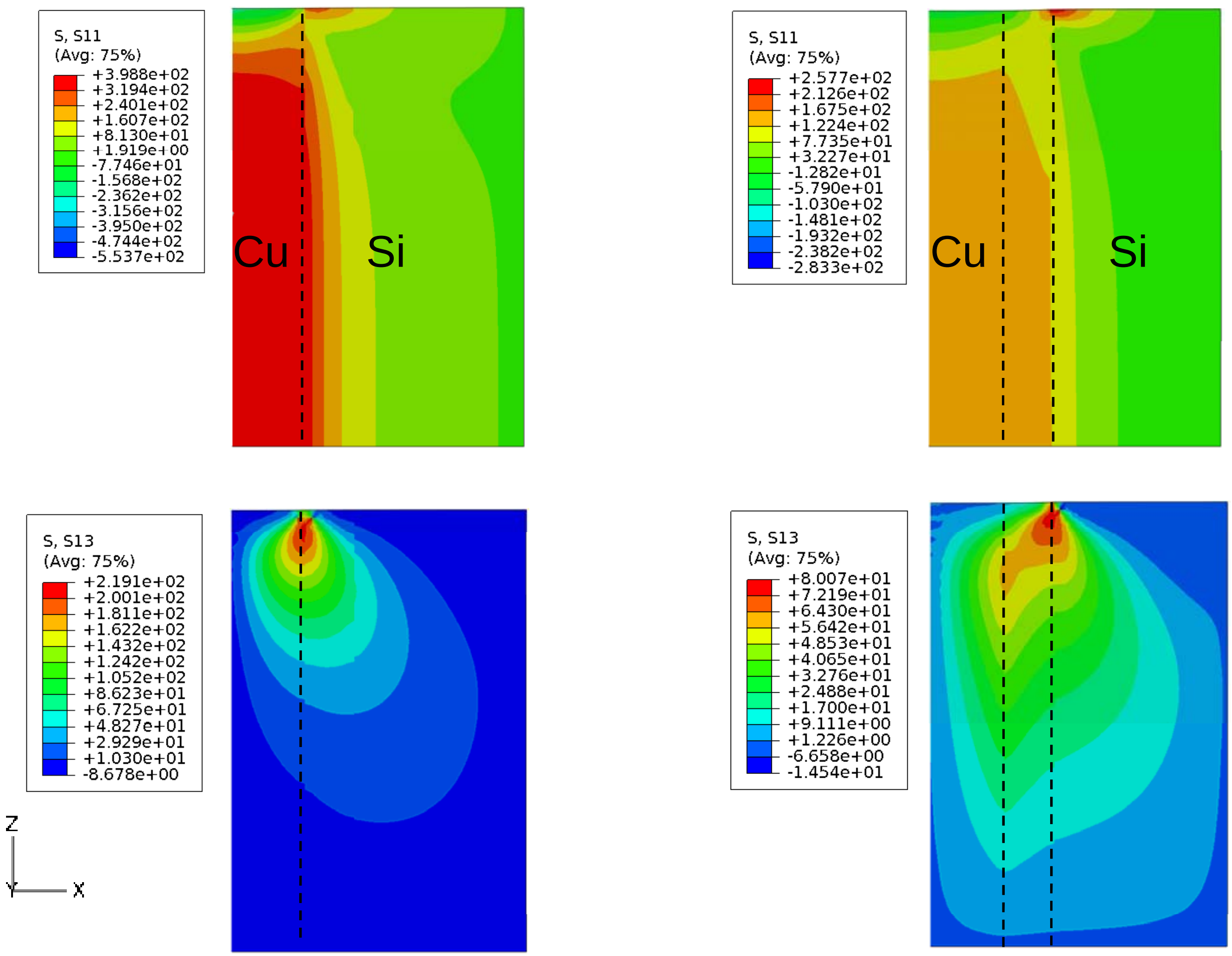
Effect of Liner Interlayer

σ_r

opening stress

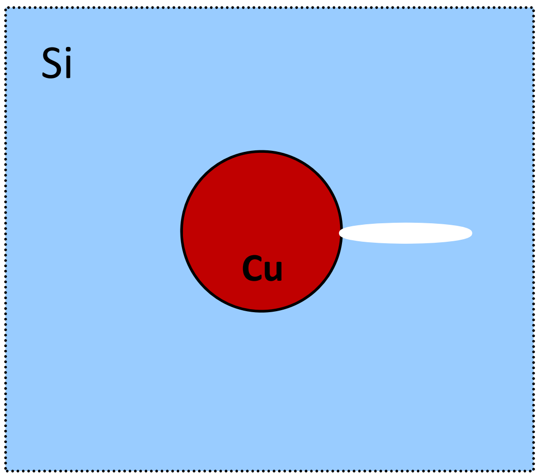
σ_{rz}

shear stress

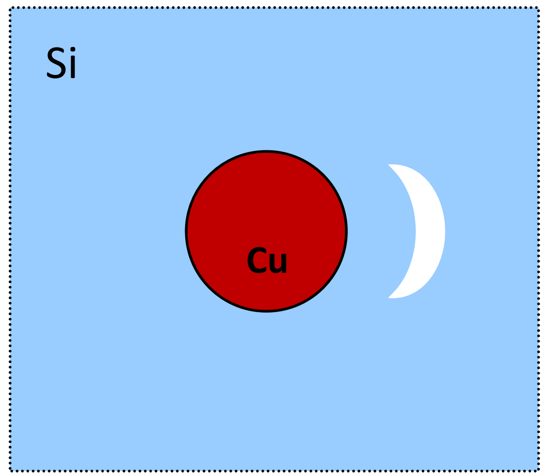


Without liner **With liner**

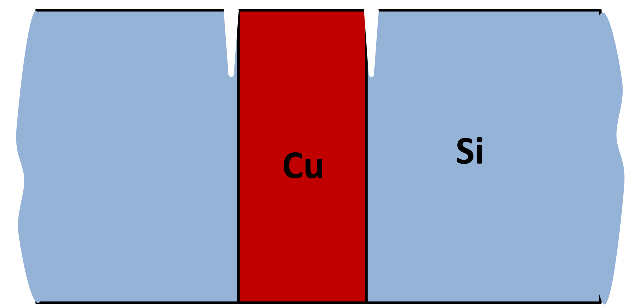
Potential Fracture Modes of TSVs



R-crack



C-crack



Interfacial crack

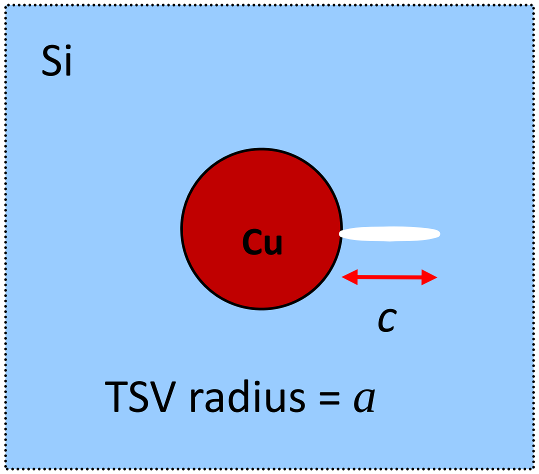
- R-crack may grow in Si during heating ($\Delta T > 0$) when the circumferential stress is tensile ($\sigma_\theta > 0$).
- C-crack may grows in Si during cooling ($\Delta T < 0$) when the radial stress is tensile ($\sigma_r > 0$).
- Interfacial crack can grow during both heating and cooling.

Concepts of Fracture Mechanics

- **Energy release rate** (ERR or ***G***): thermodynamic driving force for crack growth, the elastic strain energy released per unit area of the crack; calculated by FEA or other methods.
- **Fracture toughness** (Γ): material resistance against cracking, an intrinsic property of the material or interface; measured by experiments.
- *An simple comparison between G and Γ predicts crack growth or not.*

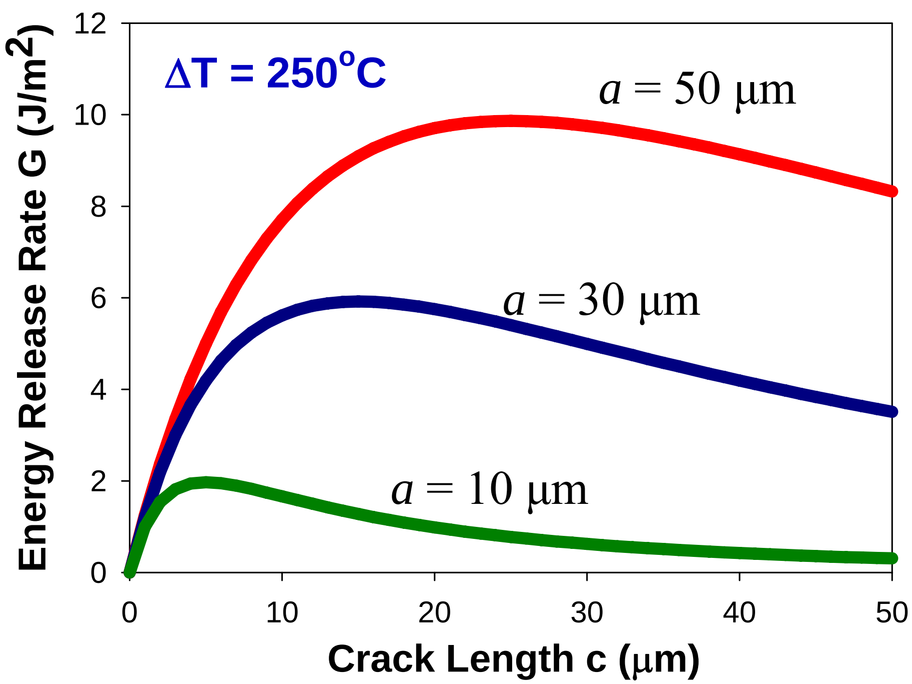
- **Cohesive zone modeling**: use a nonlinear traction-separation relationship to describe the interactions across the interface, including crack nucleation and growth.

TSV-induced R-crack in Si



Energy release rate:

$$G(c) = \frac{\pi E(\Delta\alpha\Delta T)^2}{8(1-\nu)^2}\frac{c}{(1+c/a)^3}$$

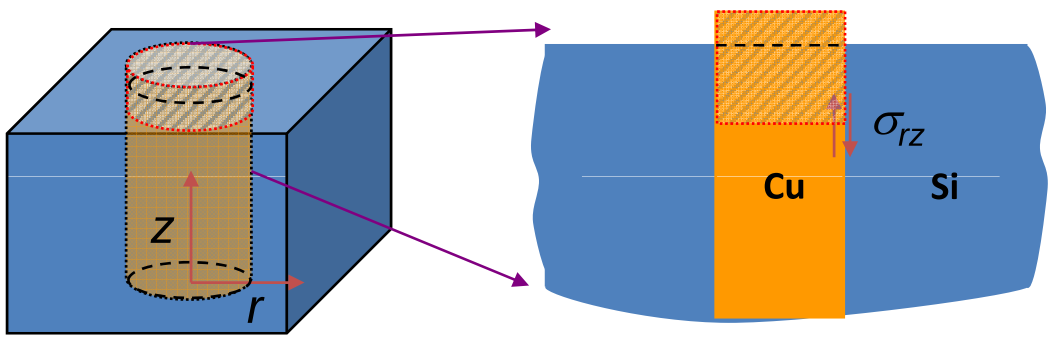


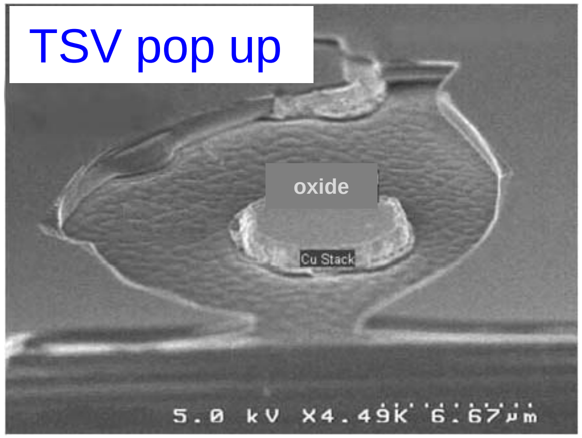
- The energy release rate for a R-crack increases as the via diameter increases.
- The maximum energy release rate occurs at the crack length $c = 0.5a$:

$$G_{max}(a) = \frac{\pi(\Delta\alpha\Delta T)^2}{54(1-\nu)^2}Ea$$

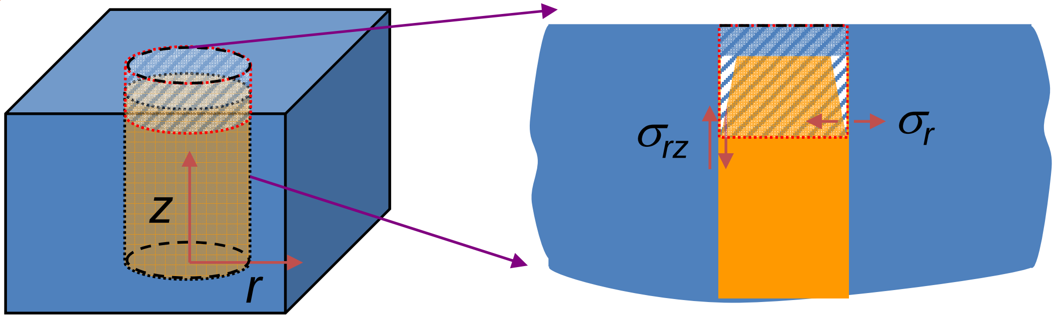
TSV Interfacial Delamination

- **Heating cycle ($\Delta T > 0$): Interfacial crack driven by shear stress (σ_{rz}); Mode II fracture**

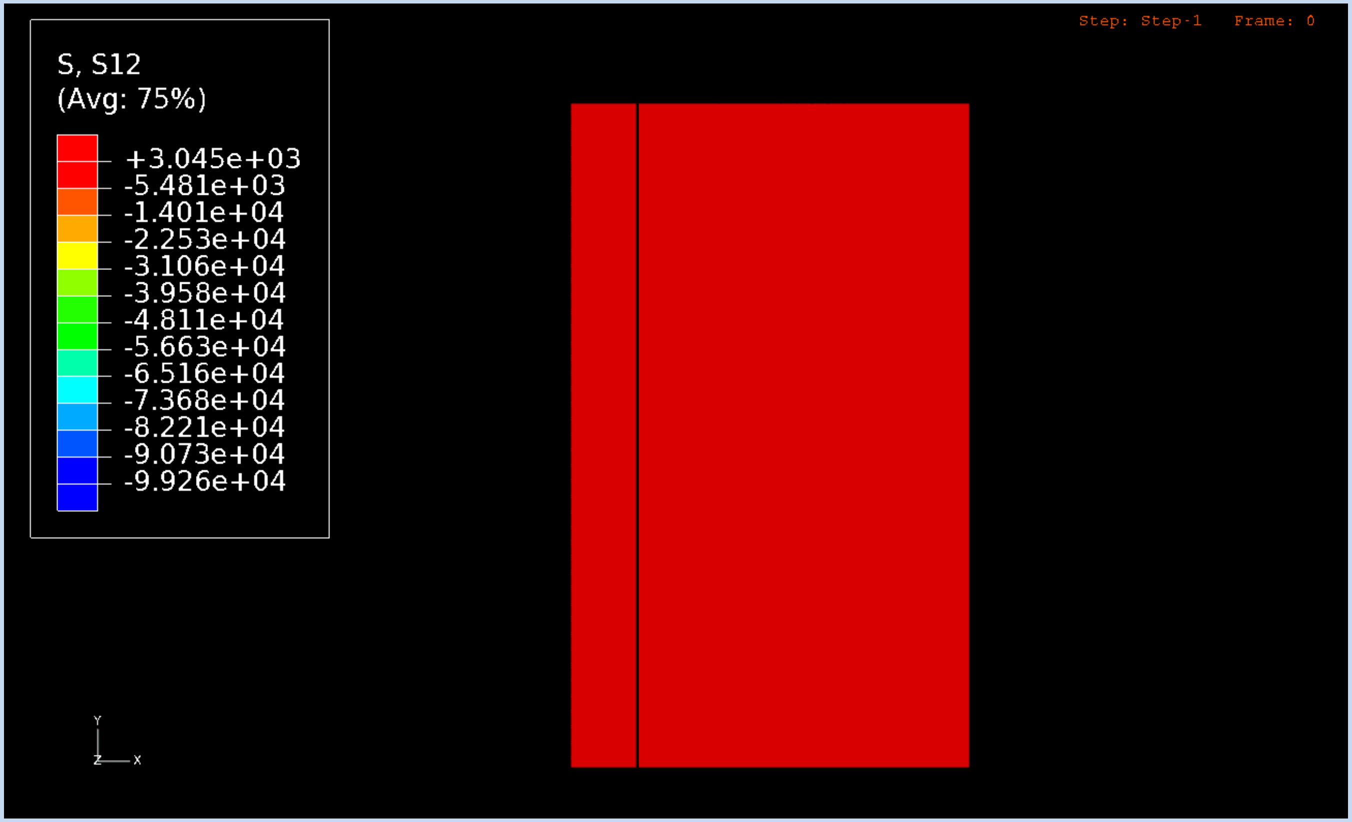


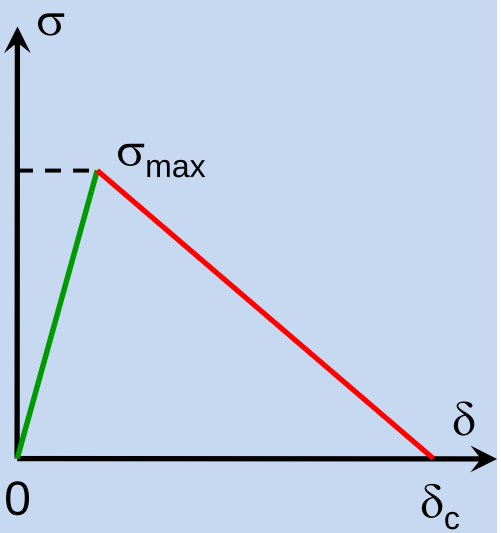


- **Cooling cycle ($\Delta T < 0$): Crack driven by both shear stress (σ_{rz}) and radial stress ($\sigma_r > 0$); mixed mode fracture (Mode I + Mode II)**



Via pop-up upon heating

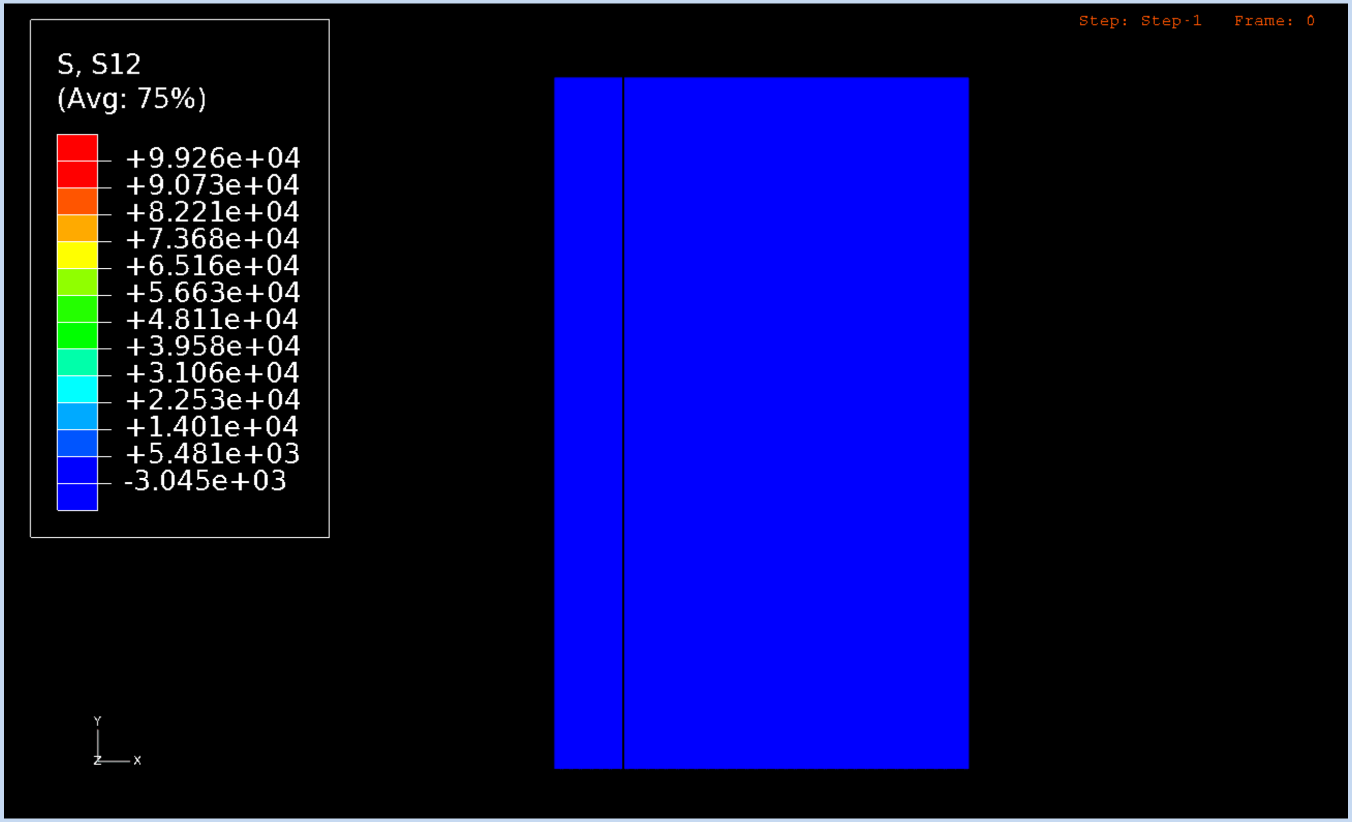




$\Gamma = \sigma_{max}\delta_c/2$

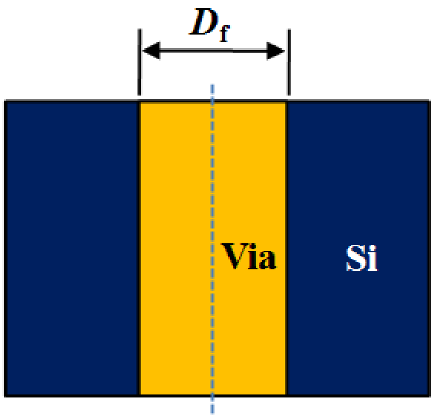
- Cu TSV subjected to heating up to +400K
- Cohesive interface elements are used to simulate crack initiation and growth
- The simulation results depend on input of interfacial properties (strength and toughness)

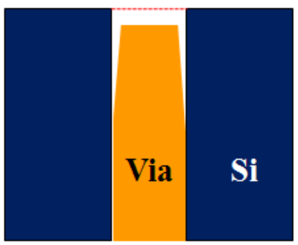
Interfacial Delamination during Cooling



- Cu TSV subjected to cooling up to -400K
- Cohesive interface elements are used to simulate crack initiation and growth

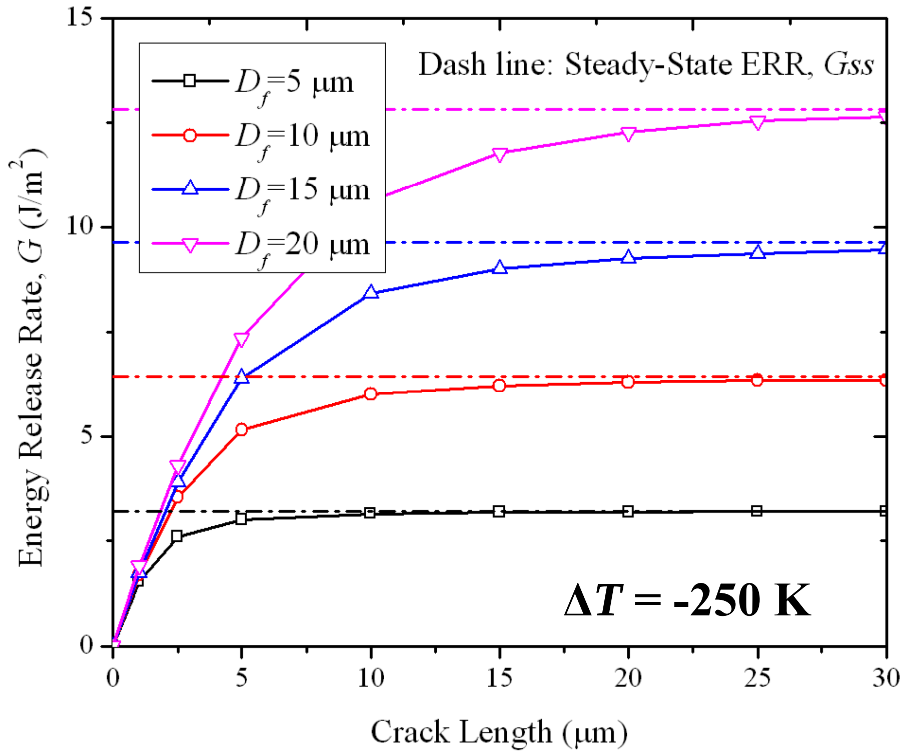
Energy Release Rate (ERR)

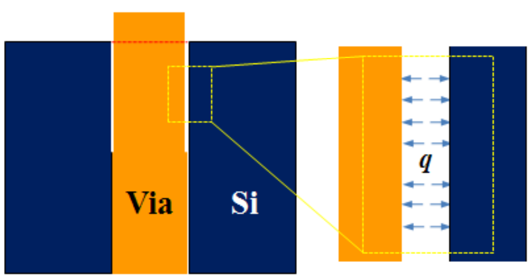




ΔT< 0 : Mode I+II

$$G_{cooling}^{SS} \approx \frac{E(\Delta\alpha\Delta T)^2 D_f}{4(1-\nu)}$$



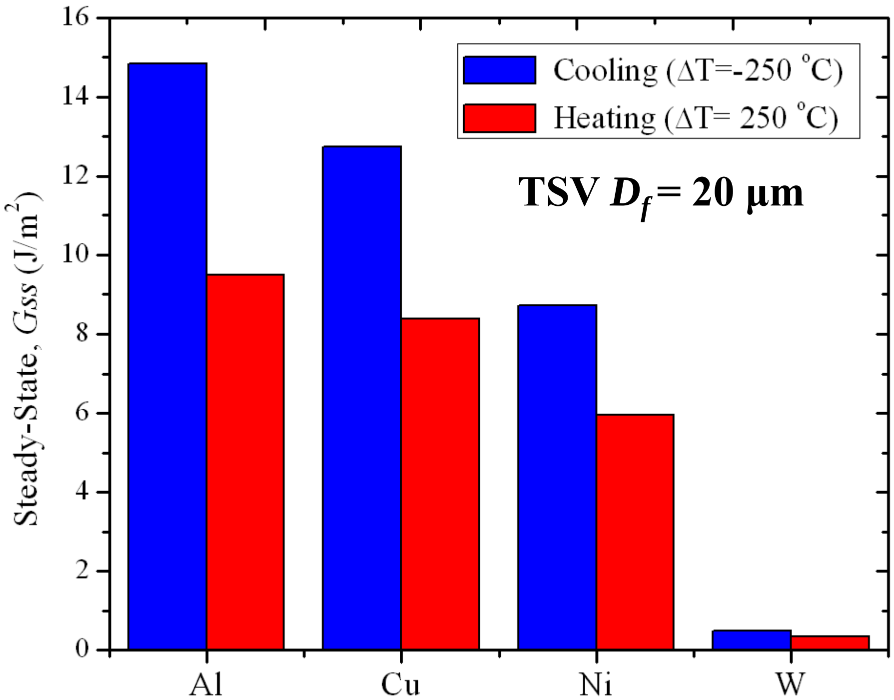


ΔT > 0: Mode II

$$G_{heating}^{SS} \approx \frac{1+\nu}{8(1-\nu)} E(\Delta\alpha\Delta T)^2 D_f$$

- The steady-state ERR sets an upper bound for the crack driving force, which may be used for conservative design.

Effect of TSV Metals

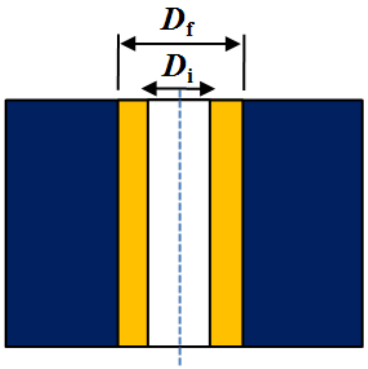


Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's Ratio
Al	20	70	0.35
Cu	17	110	0.35
Ni	13	207	0.31
W	4.4	400	0.28
Si	2.3	130	0.28

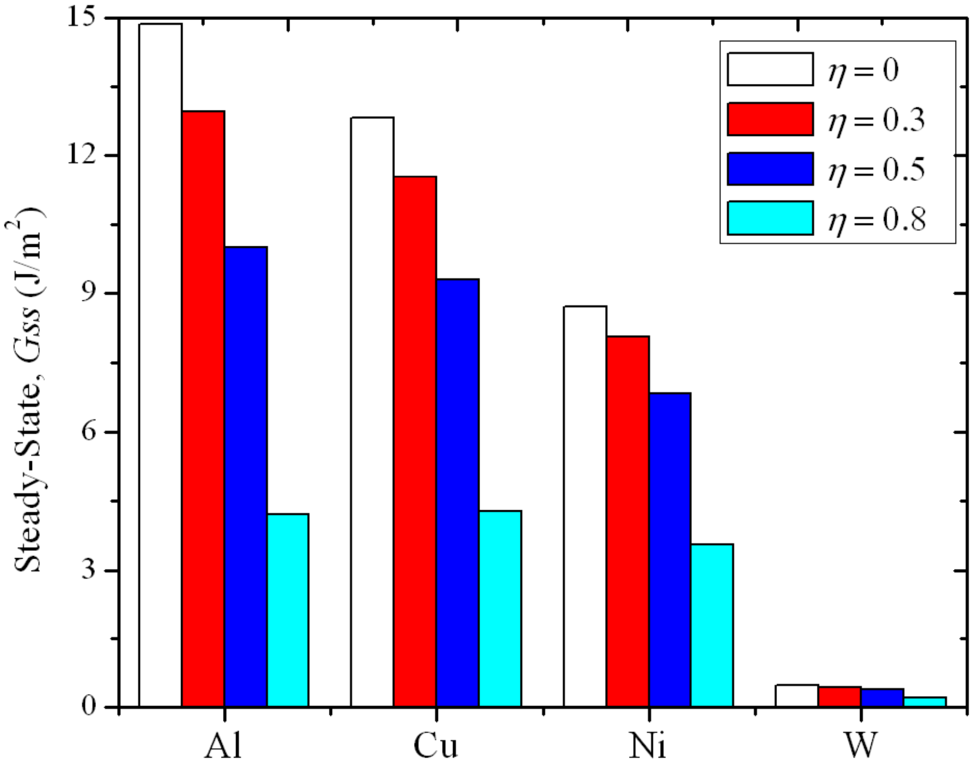
$$G_{SS} = \frac{E_{Si}\left(\Delta\alpha\Delta T\right)^2 D_f}{4} f\left(\frac{E_{TSV}}{E_{Si}}, \nu_{TSV}, \nu_{Si}\right)$$

- The effect of thermal mismatch dominates the effect of elastic mismatch.

Annular TSV



Diameter ratio: $\eta = \dfrac{D_i}{D_f}$

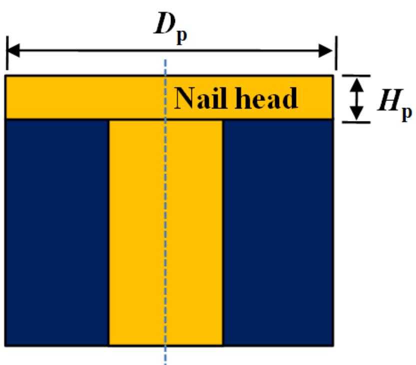


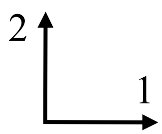
Steady-State ERR for interfacial delamination:

$$G_{SS} = \frac{E_{Si}\left(\Delta\alpha\Delta T\right)^2 D_f}{4} f\left(\eta, \frac{E_{TSV}}{E_{Si}}, \nu_{TSV}, \nu_{Si}\right) \approx \frac{E\left(\Delta\alpha\Delta T\right)^2 D_f}{4(1-\nu)}\left(1-\eta^2\right)$$

TSV with Nail Head

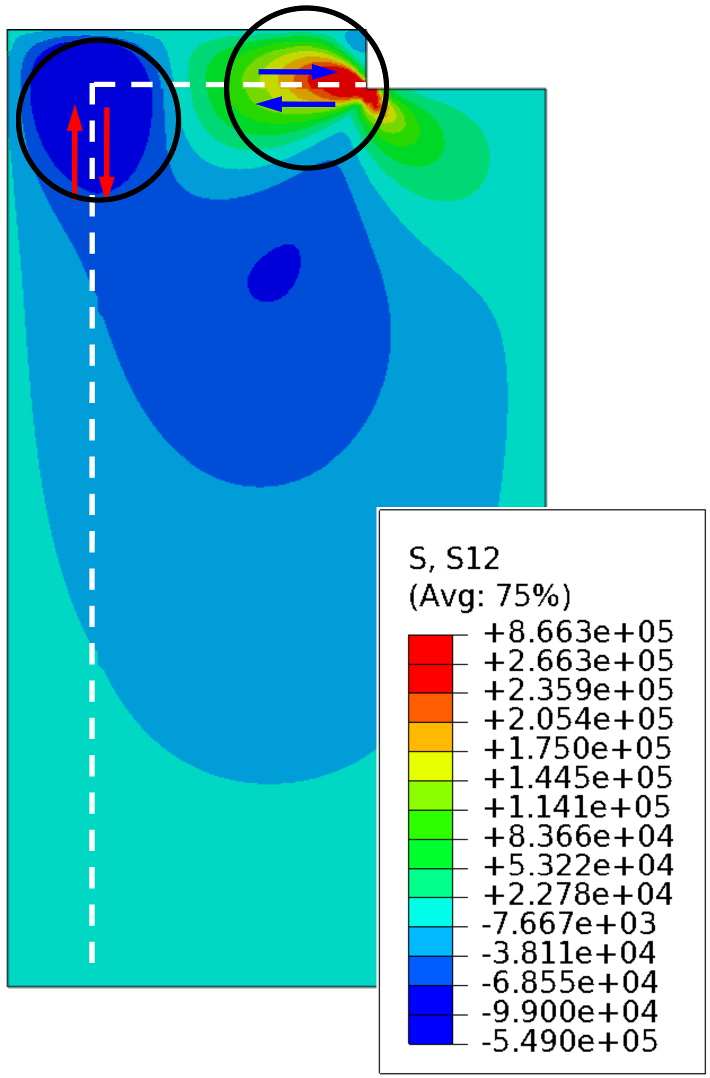
- Shear stress at both interfaces
- Opening stress at the NH/Si interface (heating)

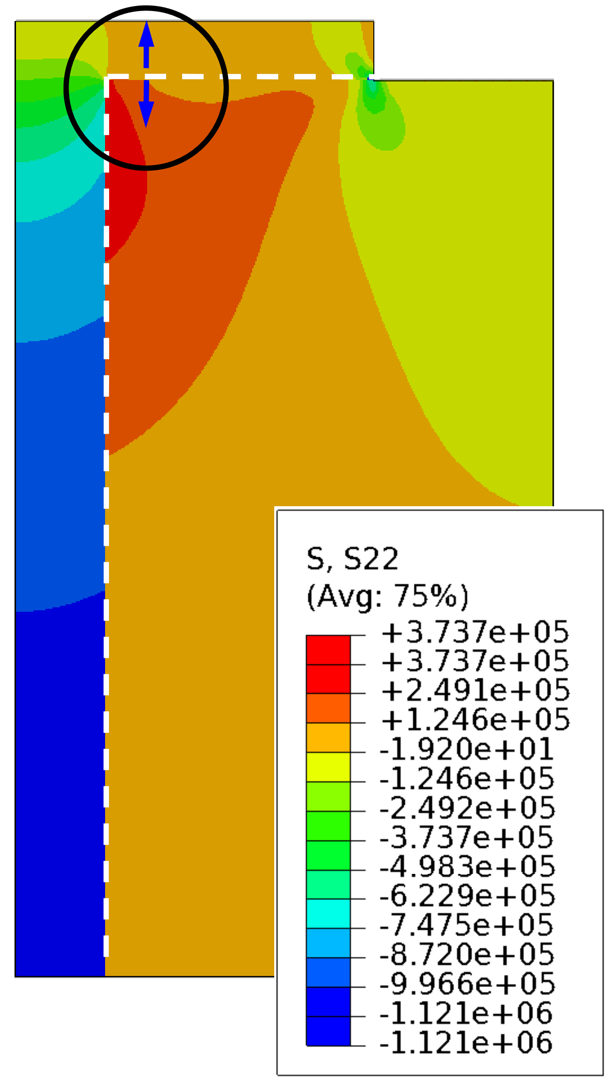




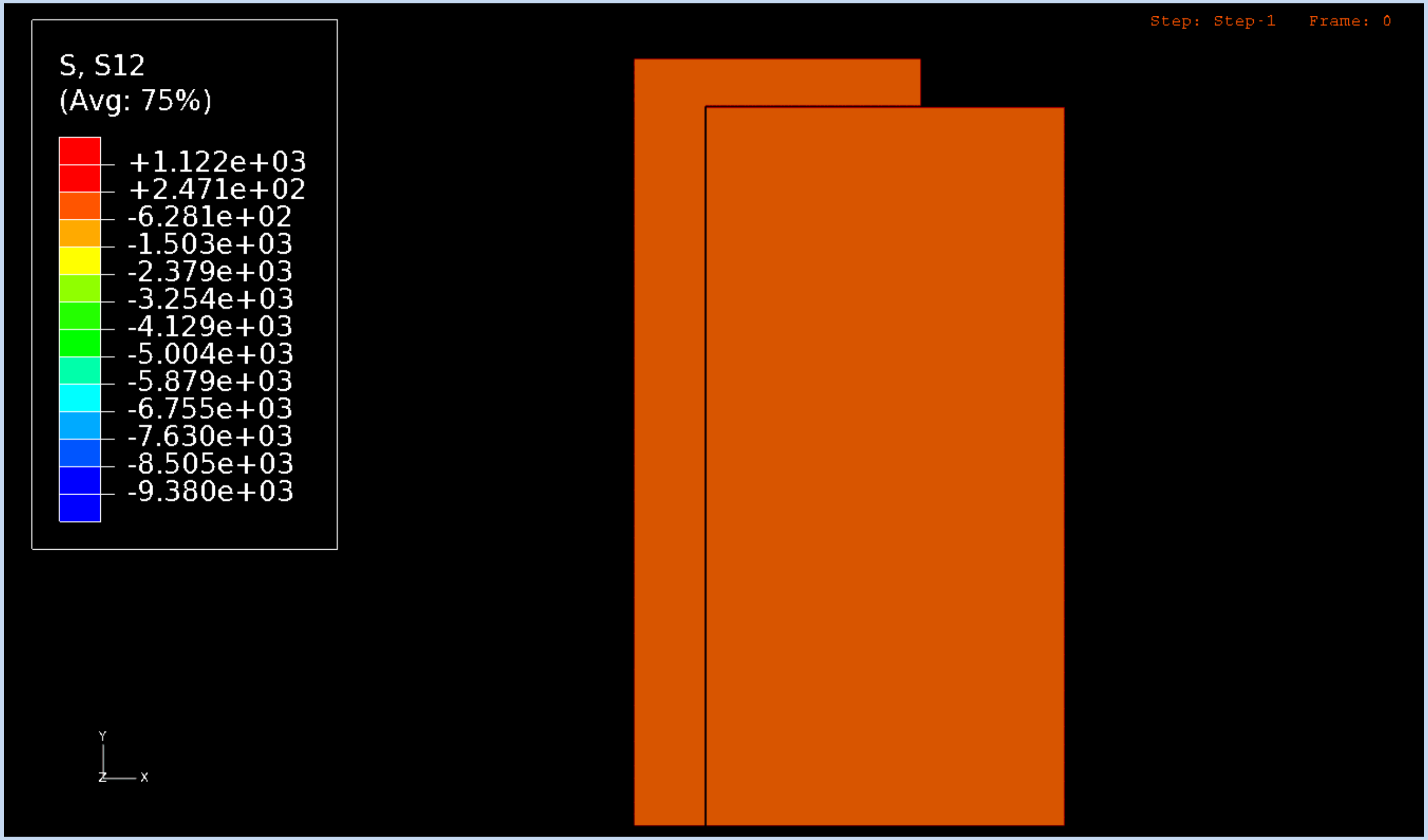
$$D_f = 6\mu m$$

$$\Delta T = 400\,K$$



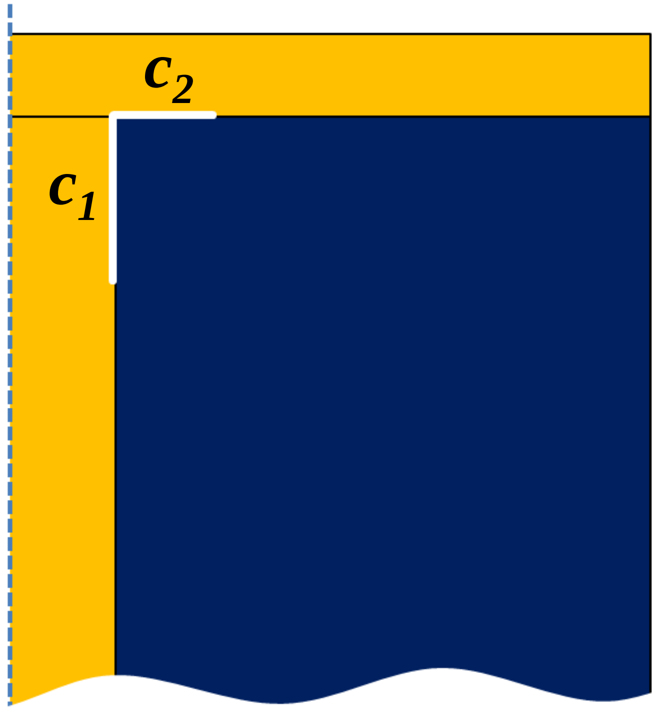


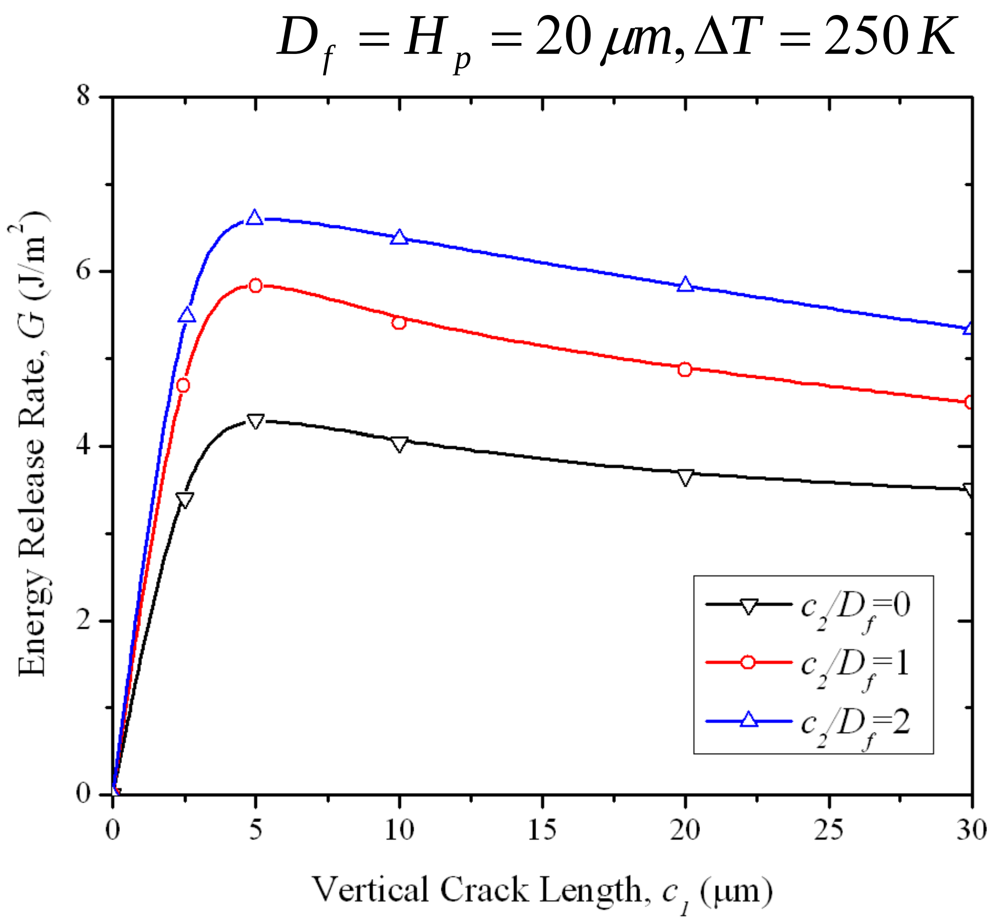
TSV pop-up with nail head



- Cu TSV/NH subjected to heating up to +400K
- Cohesive interface elements are used to for both via/Si and NH/Si interfaces

Energy Release Rate





- Delamination typically initiates from the corner (site of stress concentration) and grows simultaneously along both interfaces.

Summary

- Thermal expansion mismatch induces stresses in TSV and surround materials. TSV geometry and material combination can generate complex 3D stress fields that affects the determination of keep-away zone.
- Interfacial delamination of TSV can occur under both heating and cooling while r-crack in Si could occur under heating. In both cases, the crack driving force increases with the TSV diameter and scales with the square of thermal loading.
- The reliability of TSV structure can be improved by optimizing the materials and geometry to reduce the crack driving force.
- Cohesive zone modeling could be useful in the study of crack nucleation and growth, for which experimental measurements of the interfacial properties (toughness and strength) are needed.